



COM Express™ PCOM-B702GT User's Guide R0.4

Revision History

Rev.	Note	Date
R0.1	Preliminary	Jan.2017
R0.2	Add CH5 Signal Descriptions and Pin out Tables	Nov.2021
R0.3	SKU updated & revised model name to B702GT	Dec. 2023
R0.4	Revise Chapter 9	Jan. 2024

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1 Introduction

PCOM-B702GT a COM Express® Type 7, Compact form factor (95mm x 95mm) module developed by Portwell, Inc. It is empowered by Intel® Atom-C3000 refresh processor aiming at Networking and IOT application. The module implements Atom® C3000 Refresh series processors. It offers connectivity interface such as 4x 10GbE KR, 1xPCIe Gen 3.0 x8, 2x USB 3.0, 4x USB 2.0, and 2x SATA III I/O expansion, it also supports Intel® QuickAssist Technology (Intel® QAT), NC-SI, and extended temperature (-40°C to 80°C) by selected SKUs

2 Block Diagram

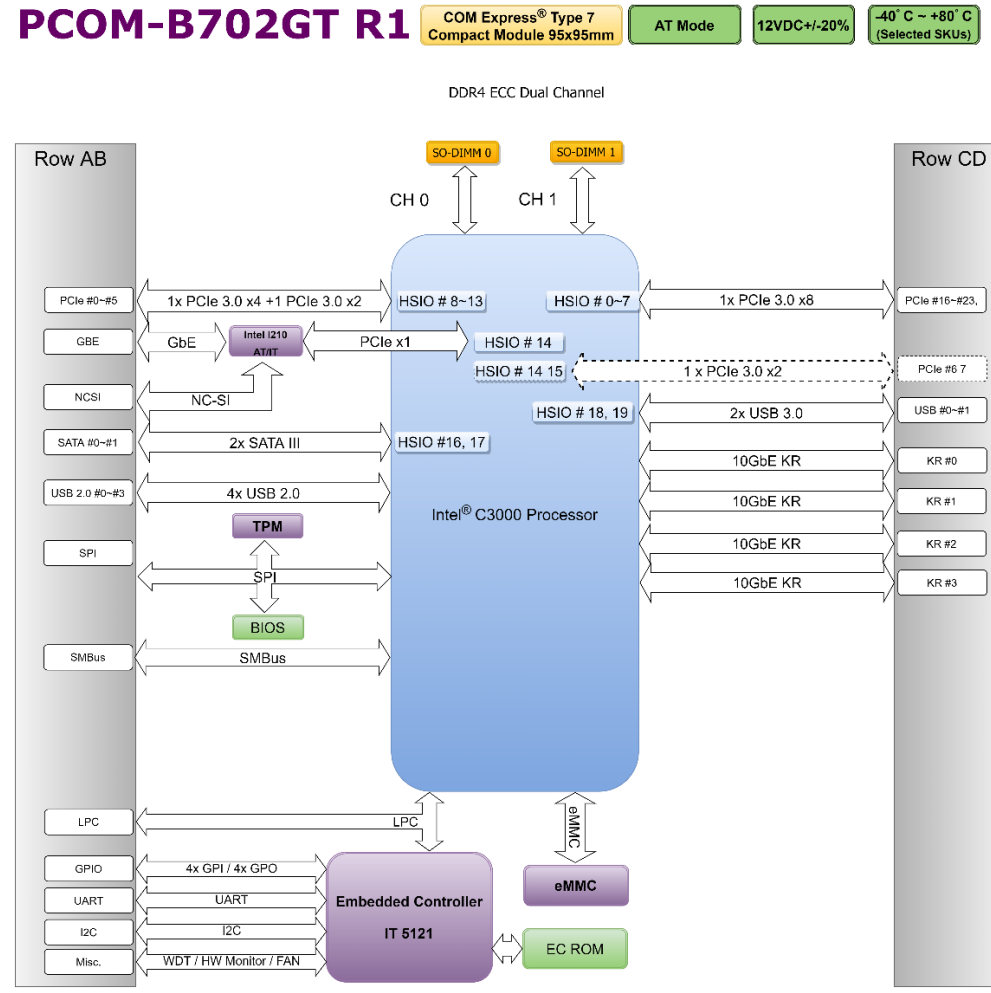


Figure 1 Block Diagram

3 Specifications

Product	➤ PCOM-B702GT
Form Factor	➤ COM Express™ standard pin out Type 7 Rev. 3.0 (Basic 95 x 95mm).
Processor	➤ Intel®Atom-Processor-C3558R ➤ Intel®Atom-Processor-C3708 ➤ Intel®Atom-Processor-C3508 ➤ Intel®Atom-Processor-C3308
BIOS	➤ AMI Aptio5 BIOS
Memory	➤ SODIMM DDR4 ➤ Support ECC ➤ Up to 128GB 2400MHz
Ethernet	➤ Intel® I210IT ➤ 4 x 10G KR(By Selected SKU)
Security	➤ TPM 2.0
I/O	➤ 1 PCI Express x8 (PEG) up to Gen3 (8.0 GT/s) configuration x4, x8, x16 ➤ 4 x USB2.0 (480 Mbps) & 2 x USB3.0 (5 Gbps) ➤ 2 x SATA3.0 (6 Gbps) ➤ GPIO / I2C / 2 Serial Ports / SMBus
Hardware Monitors	➤ IT5121 Embedded Controller, Voltage, Fan and Temperature
Power Management	➤ ACPI 5.0a
Environment	➤ Operating Temperature 0 ~ 60 ° C & -40 ~ 85 ° C (By Selected SKUS) ➤ Storage Temperature 0 ~ 60 ° C ➤ Relative Humidity 5%~95%

Table 1 Specification

3.1 PCOM-B702GT Processor List

PCOM-B702GT Processor List

PCOM-B702GT Series	PCOM-B702GT	PCOM-B702GT	PCOM-B702GT	PCOM-B702GT
Ordering P/N	AB1-3R78	AB1-3R79	AB1-3J40	AB1-3H45
Processor Number	C3558R	C3708	C3508	C3308
Cache	8 MB	16 MB	8 MB	4 MB
Instruction Set	64-bit	64-bit	64-bit	64-bit
# of Cores	4	8	4	2
# of Threads	4	8	4	2
Processor Base Frequency	2.4 GHz	1.7 GHz	1.6 GHz	1.6 GHz
Turbo Boost Frequency	N/A	N/A	N/A	2.1 GHz
TDP	17 W	17 W	11.5 W	9.5 W

Table 2 PCOM-B702GT Processor List

3.2 Supported Operating Systems

The PCOM-B702GT supports the following operating systems.

Windows	Windows server 2012 r2,2016
Linux Yocto	Kernel version: 5.8
Red Hat	7.3, 7.4 version
Ubuntu(Canonical)	16.04, 18.04
CentOS	7.3
WR Linux	WRL8, WRL 9 , LTS 17,LTS 18, LTS 19
SUSE	12 SP3

3.3 Windows OS driver

Please download the drivers from Portwell download center website

Download Center	https://www.portwell.com.tw/support-center/download-center/	Standard release for launched product
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3.4 Electrical Characteristics

Input Voltage	+12VDC (Nominal)
RTC Battery	
Power on Mode	AT Mode

Table 3 Electrical Characteristics

Figure 33-1. ACPI Cold Boot Sequence

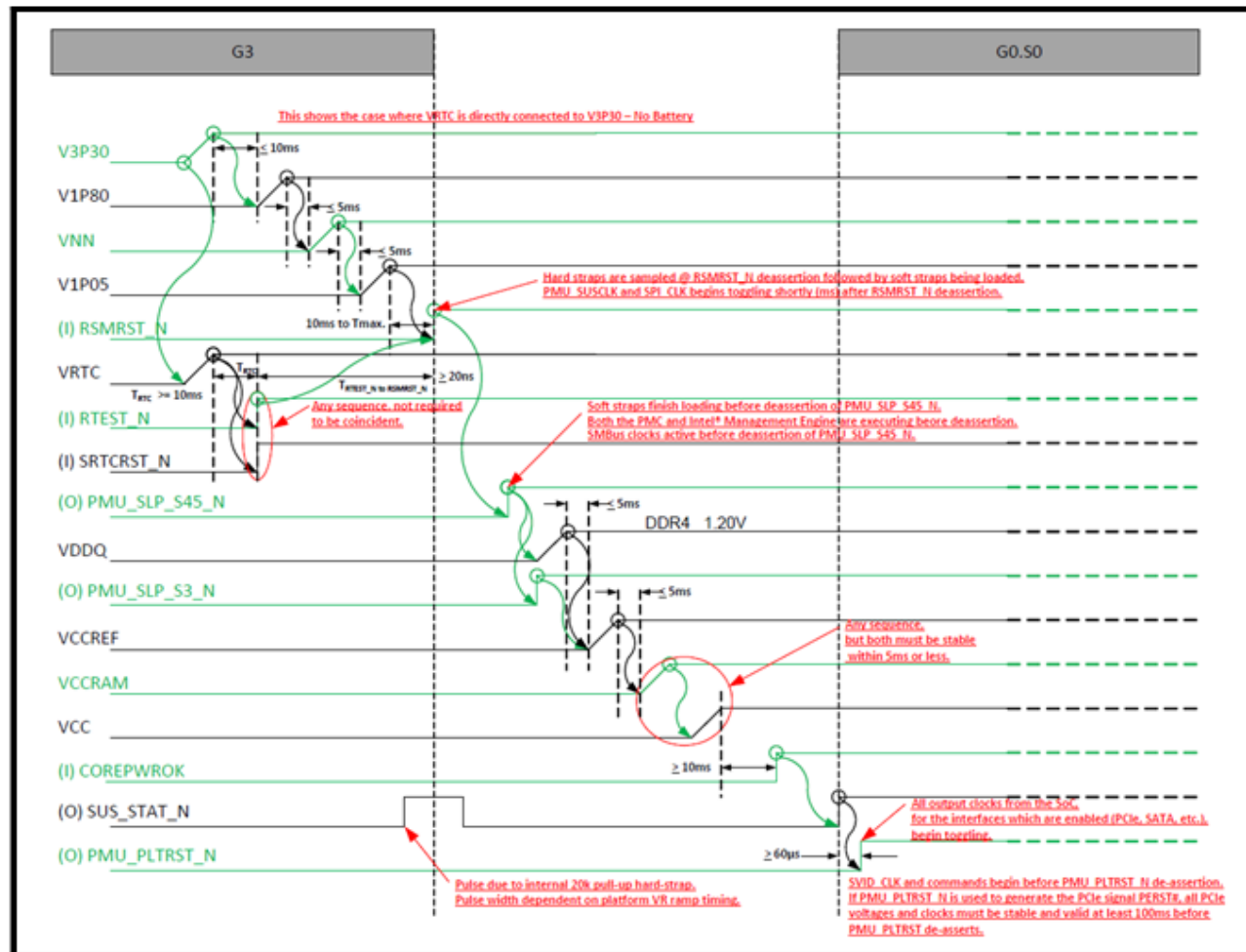


Figure 2 Power on Sequence

Figure 33-3. ACPI Shutdown Sequence

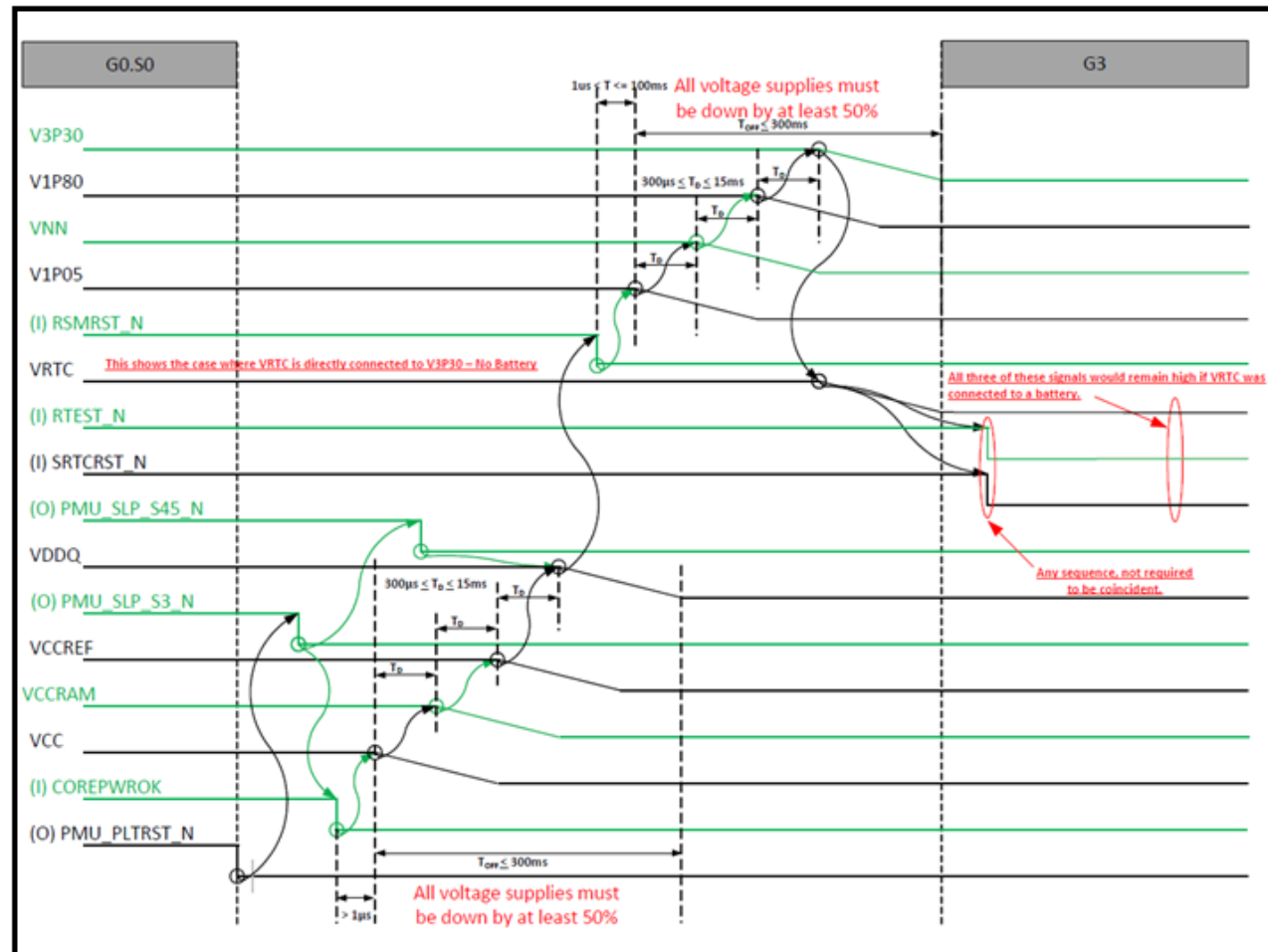


Figure 3 Shutdown Sequence

3.5 Power Consumption

Series	PCOM-B702GT			
Processor	C3558R	C3708	C3508	C3308
<u>Power Consumption</u>				
S0 Idle	0.56A	0.58A	0.55A	0.46A
100% workload without turbo mode	0.81A	1.03A	0.93A	0.66A
Peak Current	0.74A	0.75A	0.68A	0.61A

Table 4 Power Consumption

3.6 Mechanical Dimensions

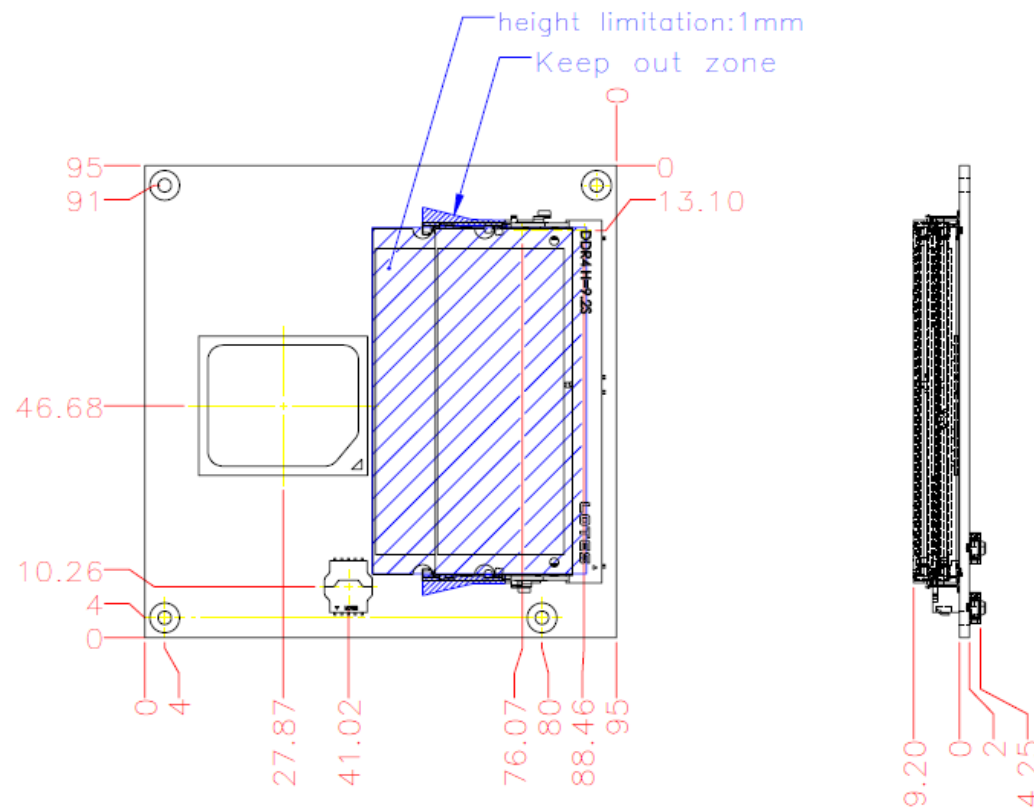


Figure 4 Mechanical Dimensions - Top

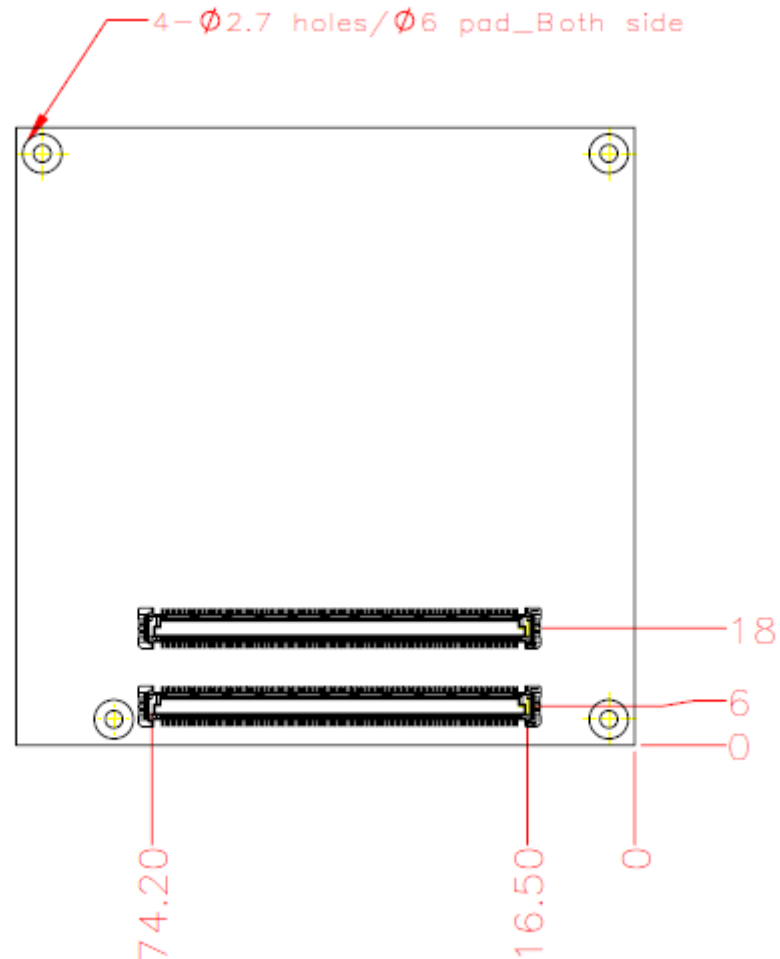
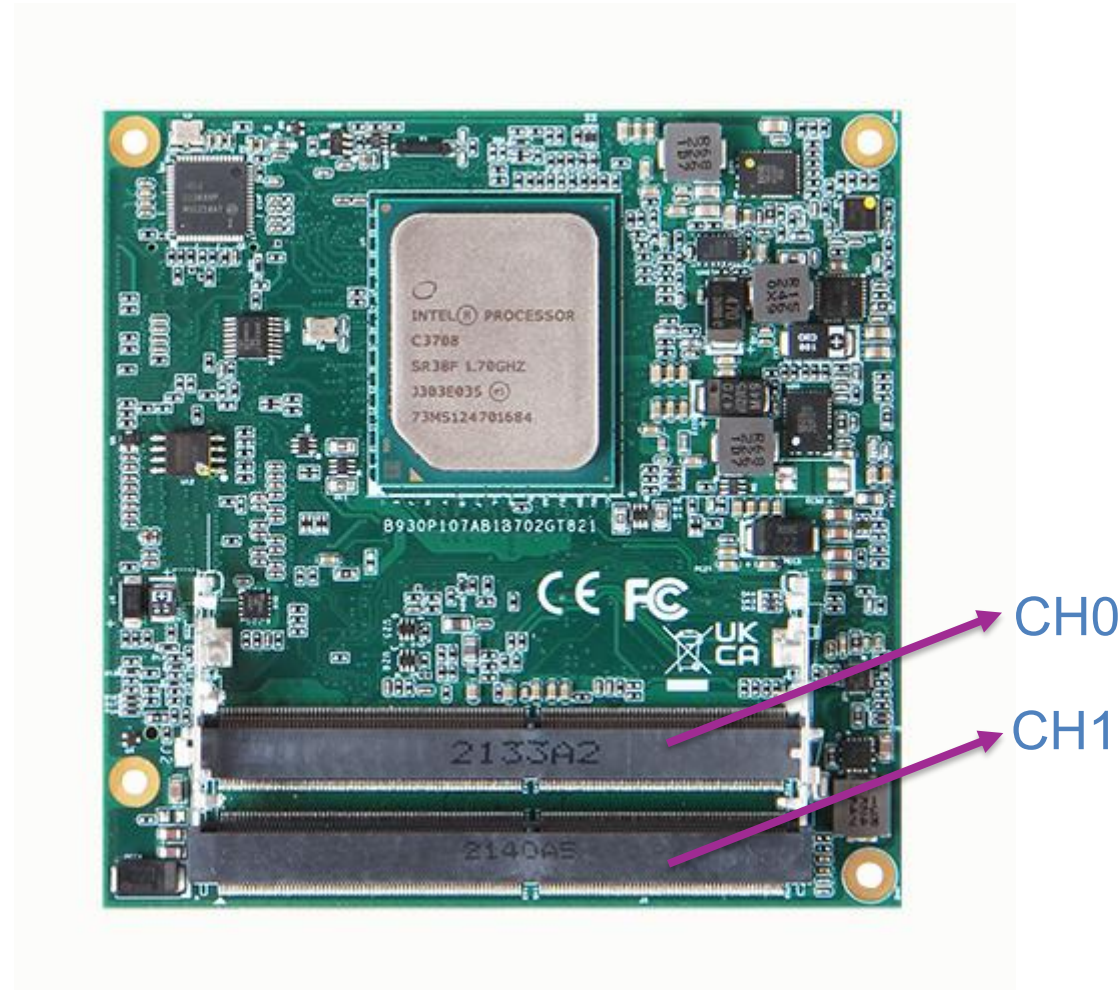


Figure 5 Mechanical Dimensions - Bottom

3.7 2x SODIMM Socket Design

PCOM-B702GT has designed additional Memory SODIMM socket, which supports up to DDR4 128GB capacity. There are 2 SODIMM socket of channel 0 & channel 1 (C3308 only support CH0)



3.8 Environmental Specifications

Storage Temperature	-40°C ~85°C
Operation Temperature	0°C ~60°C, Extended : -40°C ~+85°C (By Selected SKUS)
Storage Humidity	0%~95%
Operation Humidity	0%~95%

Table 5 Environmental Specifications

3.9 Ordering Guide

Module

Model	Ordering P/N	Status
PCOM-B702GT-C3558R	AB1-3R87	Available
PCOM-B702GT-C3708	AB1-3R79	Available
PCOM-B702GT-C3508	AB1-3J40	Available
PCOM-B702GT-C3308	AB1-3H45	Available

Table 6 Ordering Guide - PCOM-B702GT

Accessory

Accessory	Ordering P/N	Status
PCOM-B702GT Heat Spreader	B830C140	Available
PCOM-B702GT Heatsink	B830A920	Available
PCOM-B702GT Cooler (for SKU 3708)	B9972230	Available
Evaluation Carrier PCOM-C701	AB1-3J61Z	Available

Table 7 Ordering Guide - Accessory

3.10 Packaging

Package	Appearance	Size
Anti-Static bubble bag		180x135mm
White Paper Box		210x151x40mm
Shipping Box (10 pcs White paper box)		595x300x195mm

Table 8 Packaging Information

4 Thermal Solution

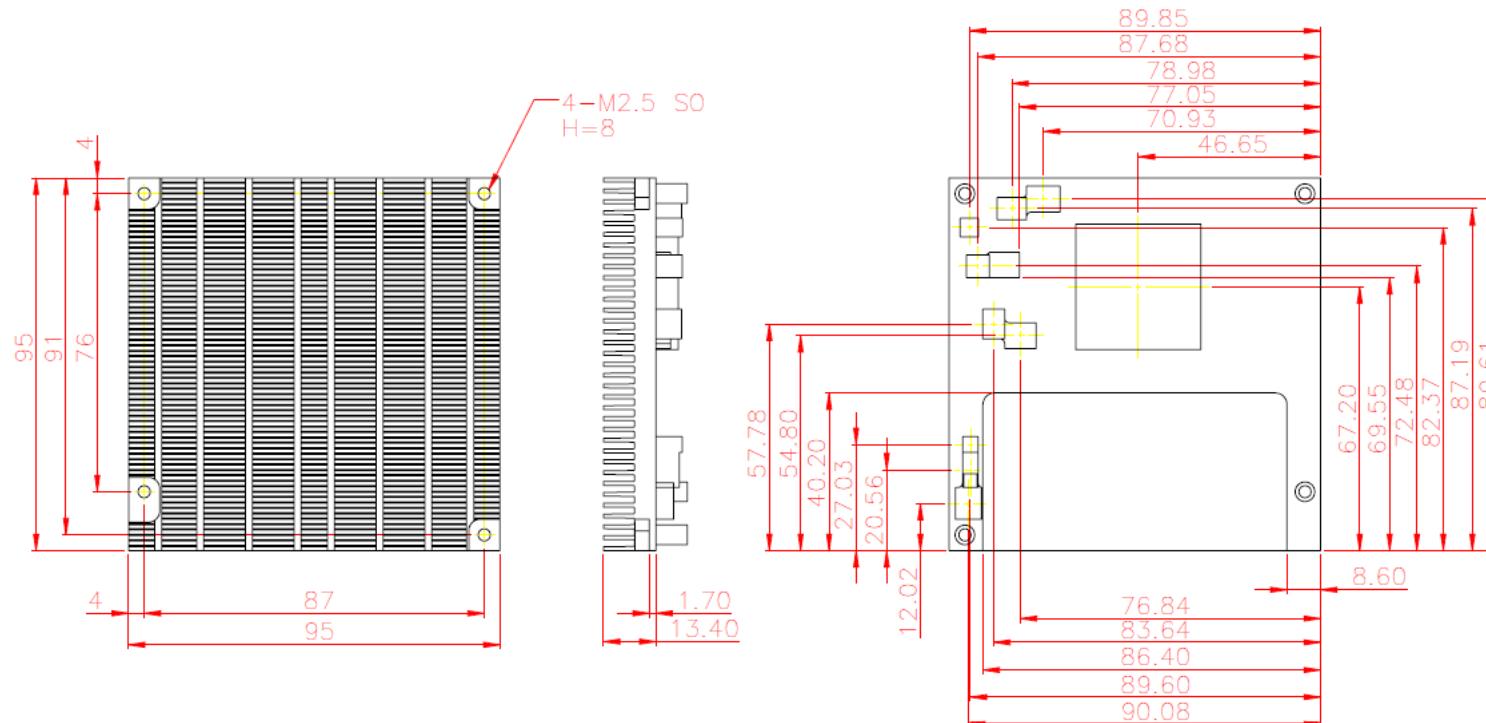


Figure 6 Heat Sink

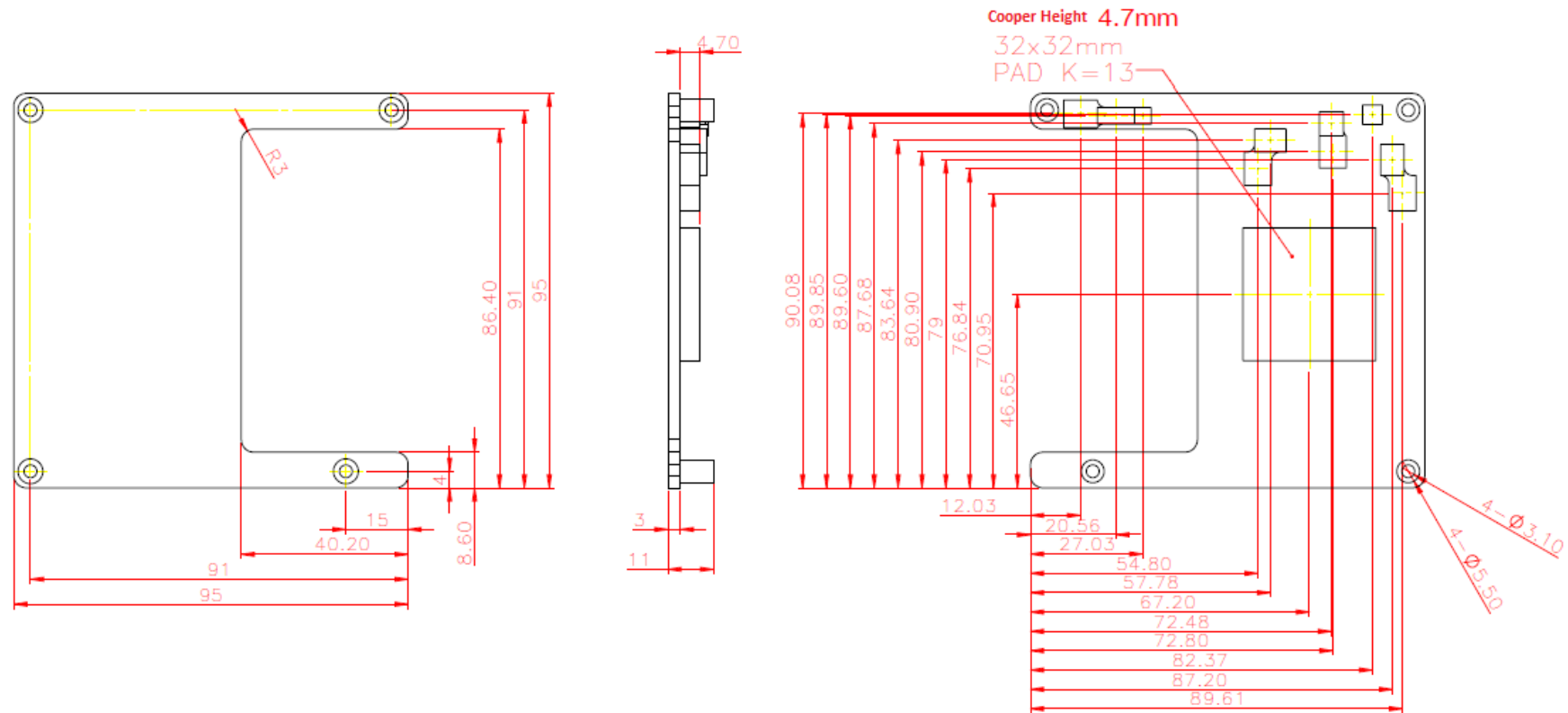


Figure 7 Heat Spreader

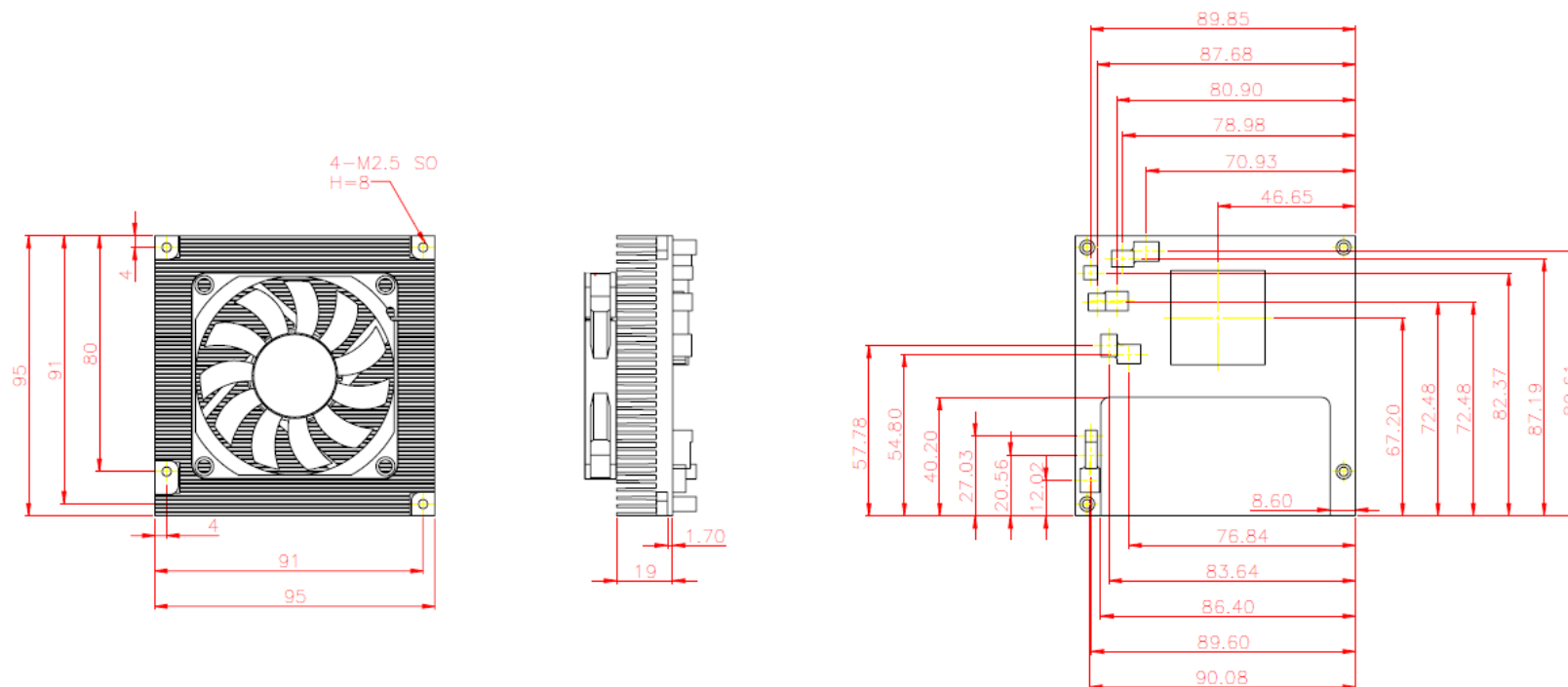


Figure 8 Cooler (only for C3708 SKU)

5 Signal Descriptions and Pin out Tables

Signal Tables Terminology Descriptions

I	Input to the Module
O	Output from the Module
I/O	Bi-direction input / output signal
OD	Open Drain output
CMOS	Logic input or output. Input thresholds and output levels shall be 80% of supply rail for high side and 20% of the relevant supply rail for low side.
PCIE	PCI Express compatible differential signal. Please refer to the PCI Express Specification for details. PCIE transmit pins (Module outputs) shall be AC coupled on the Module. PCIE receive pins (Module inputs) shall be DC coupled on the COM Express® Module and shall be assumed to be AC coupled off Module, close to the signal source. If the target PCI Express device resides on the Carrier Board, the Module PCIE receive lanes (target PCIE device transmit lanes) shall be AC coupled near the device on the Carrier Board. If the Carrier Board implements a PCIE slot, then these signals shall be AC coupled on the add-in card, not on the Carrier Board.
SATA	SATA compatible differential signal. Please refer to the SATA Specification for details. All COM Express® SATA signals shall be AC coupled on the Module.
LVDS	Low Voltage Differential Signal – 330mV nominal; 450mV maximum differential signal.
Analog	Inputs and Outputs used for LAN, and VGA are analog signals.
PU	Pull-up resistor on PCOM-B702GT
PD	Pull-down resistor on PCOM-B702GT

Table 9 Signal Tables Terminology Descriptions

#Note : Reserved / Not connected pins are highlighted as **gray** color.

Pin	Signal	Description	I/O	Type	Power / Tolerance	PU / PD	Note
A1	GND	GND(FIXED)	-	-	-	-	-
A2	L1_MDIN3	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs	I/O	Analog	3.3V max Suspend	-	-
A3	L1_MDIP3	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs	I/O	Analog	3.3V max Suspend	-	-
A4	L1_100#	Gigabit Ethernet Controller 0 100 Mbit / sec link indicator, active low.	OD	CMOS	3.3V Suspend / 3.3V	-	-
A5	L1_1000#	Gigabit Ethernet Controller 0 1000 Mbit / sec link indicator, active low.	OD	CMOS	3.3V Suspend / 3.3V	-	-
A6	L1_MDIN2	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs	I/O	Analog	3.3V max Suspend	-	-
A7	L1_MDIP2	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs	I/O	Analog	3.3V max Suspend	-	-
A8	L1_LINK#	Gigabit Ethernet Controller 0 link indicator, active low.	OD	CMOS	3.3V Suspend / 3.3V	PU 10k ohm to 3VSB	-

A9	L1_MDIN1	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs	I/O	Analog	3.3V max Suspend	-	-
A10	L1_MDIP1	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs	I/O	Analog	3.3V max Suspend	-	-
A11	GND	GND(FIXED)	-	-	-	-	-
A12	L1_MDIN0	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs	I/O	Analog	3.3V max Suspend	-	-
A13	L1_MDIP0	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs	I/O	Analog	3.3V max Suspend	-	-
A14	GBE_CTREF_CN	Reference voltage for Carrier Board Ethernet channel 0 magnetics center tap.	-	-	GND min 3.3V max	Placeholder 0 ohm to V_1P5_L2	-
A15	SLP_S3_CN	Indicates system is in Suspend to RAM state. Active low output. An inverted copy of SUS_S3# on the Carrier Board may be used to enable the non-standby power on a typical ATX supply.	O	CMOS	3.3V Suspend / 3.3V	PD 470 ohm	-
A16	SATA0_PCIE16_TXP	Serial ATA or SAS Channel 0 transmit differential pair.	O	SATA	AC coupled on Module	-	-
A17	SATA0_PCIE16_TXN	Serial ATA or SAS Channel 0 transmit differential pair.	O	SATA	AC coupled on Module	-	-

A18	SLP_S4_CN	Indicates system is in Suspend to Disk state. Active low output.	O	CMOS	3.3V Suspend / 3.3V	PD 470 ohm -	Through 0 ohm to kbc_slp_S45_N
A19	SATA0_PCIE16_RXP	Serial ATA or SAS Channel 0 receive differential pair.	I	SATA	AC coupled on Module	-	-
A20	SATA0_PCIE16_RXN	Serial ATA or SAS Channel 0 receive differential pair.	I	SATA	AC coupled on Module	-	-
A21	GND	GND(FIXED)	-	-	-	-	-
A22	PCIE_TX15+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A23	PCIE_TX15-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A24	SLP_S5_CN	Indicates system is in Soft Off state.	O	CMOS	3.3V Suspend / 3.3V	PD 470 ohm	Through 0 ohm to kbc_slp_S45_N
A25	PCIE_TX14+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A26	PCIE_TX14-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A27	BATLOW_N	Indicates that external battery is low. This port provides a battery-low signal to the Module for orderly transitioning to power saving or power cut-off ACPI modes.	I	CMOS	3.3V Suspend / 3.3V	PU 1K ohm to 3VSB	-

A28	SATA_LED_N	SATA activity indicator, active low.	I/O	CMOS	3.3V / 3.3V	PU 4.7K ohm to 3VSB	-
A29	RSVD	Reserved Pin	-	-	-	-	-
A30	RSVD	Reserved Pin	-	-	-	-	-
A31	GND	GND(FIXED)	-	-	-	-	-
A32	RSVD	Reserved Pin	-	-	-	-	-
A33	RSVD	Reserved Pin	-	-	-	-	-
A34	BIOS_DIS0#	Selection straps to determine the BIOS boot device. The Carrier should only float these or pull them low. Shared pin with ESPI_SAFS	I	CMOS	NA	PU 10K ohm to 3.3V	-
A35	THERMTRIP_N_CN	Active low output indicating that the CPU has entered thermal shutdown	O	CMOS	3.3V / 3.3V	PU 10K ohm to 3VSB	-
A36	PCIE_TX13+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A37	PCIE_TX13-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A38	GND	GND	-	-	-	-	-
A39	PCIE_TX12+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A40	PCIE_TX12-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A41	GND	GND(FIXED)	-	-	-	-	-

A42	SOC_USB2_DN2	USB differential pairs, channels 2. All USB ports except USB7, if implemented, shall be host ports.	I/O	USB	3.3V Suspend / 3.3V	-	-
A43	SOC_USB2_DP2	USB differential pairs, channels 2. All USB ports except USB7, if implemented, shall be host ports.	I/O	USB	3.3V Suspend / 3.3V	-	-
A44	USB_OC2_3#	USB over-current sense, USB channels 2 and 3. A pull-up for this line shall be present on the Module. Do not pull this line high on the Carrier Board	I	CMOS	3.3V Suspend / 3.3V	Go through diode then PU 10K ohm	-
A45	SOC_USB2_DN0	USB differential pairs, channels 0. All USB ports except USB7, if implemented, shall be host ports.	I/O	USB	3.3V Suspend / 3.3V	-	-
A46	SOC_USB2_DP0	USB differential pairs, channels 0. All USB ports except USB7, if implemented, shall be host ports.	I/O	USB	3.3V Suspend / 3.3V	-	-
A47	+V3P3_RTC	Real-time clock circuit-power input. Nominally +3.0V.	-	PWR	-	-	-
A48	RSVD	Reserved Pin	-	-	-	-	-
A49	GBE0_SDP	Gigabit Ethernet Controller 0 Software-Definable Pins. Can also be used for IEEE1588 support such as a 1pps signal. See section 4.3.4 for details.	I/O	CMOS	3.3V Suspend / 3.3V		-

A50	SOC_LPC_SERIRQ	LPC serial interrupt / Shared pin with ESPI_CS1#	I/O	CMOS	3.3V / 3.3V	PU 10K ohm to 3.3V	-
A51	GND	GND(FIXED)	-	-	-	-	-
A52	PCIE_TX_DP13	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A53	PCIE_TX_DN13	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A54	GPIO	General purpose input pins. Pulled high internally on the Module.	I	CMOS	3.3V / 3.3V	PU 10k ohm to 3.3V	-
A55	PCIE_TX_DP12	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A56	PCIE_TX_DN12	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A57	GND	GND	-	-	-	-	-
A58	PCIE_TX_DP11	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A59	PCIE_TX_DN11	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A60	GND	GND(FIXED)	-	-	-	-	-
A61	PCIE_TX_DP10	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A62	PCIE_TX_DN10	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-

A63	GPI1	General purpose input pins. Pulled high internally on the Module.	I	CMOS	3.3V / 3.3V	PU 10k ohm to 3.3V	-
A64	PCIE_TX_DP9	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A65	PCIE_TX_DN9	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A66	GND	GND	-	-	-	-	-
A67	GPI2	General purpose input pins. Pulled high internally on the Module.	I	CMOS	3.3V / 3.3V	PU 10k ohm to 3.3V	-
A68	PCIE_TX_DP8	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A69	PCIE_TX_DN8	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A70	GND	GND(FIXED)	-	-	-	-	-
A71	PCIE_TX8+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A72	PCIE_TX8-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A73	GND	GND	-	-	-	-	-
A74	PCIE_TX9+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A75	PCIE_TX9-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A76	GND	GND	-	-	-	-	-

A77	PCIE_TX10+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A78	PCIE_TX10-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A79	GND	GND	-	-	-	-	-
A80	GND	GND(FIXED)	-	-	-	-	-
A81	PCIE_TX11+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A82	PCIE_TX11-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A83	GND	GND	-	-	-	-	-
A84	NCSI_TX_EN_CN	NCSI Transmit Enable (PD 10K on Carrier when NC-SI is not used on Carrier)	I	-	3.3V Suspend / 3.3V		-
A85	GPI3	General purpose input pins. Pulled high internally on the Module.	I	CMOS	3.3V / 3.3V	PU 10k ohm to 3.3V	-
A86	RSVD	Reserved Pin	-	-	-	-	-
A87	RSVD	Reserved Pin	-	-	-	-	-
A88	CLK3_PCIE_P_CN	Reference clock output for all PCI Express and PCI Express Graphics lanes.	O	PCIE	PCIE	-	-
A89	CLK3_PCIE_N_CN	Reference clock output for all PCI Express and PCI Express Graphics lanes.	O	PCIE	PCIE	-	-
A90	GND	GND(FIXED)	-	-	-	-	-

A91	SPI_PWR_CN	Power supply for Carrier Board SPI – sourced from Module – nominally 3.3V. The Module shall provide a minimum of 100mA on SPI_POWER. Carriers shall use less than 100mA of SPI_POWER. SPI_POWER shall only be used to power SPI devices on the Carrier	O	-	3.3V Suspend / 3.3V	-	-
A92	SPI_MISO_CN	Data in to Module from Carrier SPI	I	CMOS	3.3V Suspend / 3.3V	-	-
A93	GPO0	General purpose output pins. Upon a hardware reset, these outputs should be low.	O	CMOS	3.3V / 3.3V	-	-
A94	SPI_CLK_CN	Clock from Module to Carrier SPI	O	CMOS	3.3V Suspend / 3.3V	-	-
A95	SPI_MOSI_CN	Data out from Module to Carrier SPI	O	CMOS	3.3V Suspend / 3.3V	-	-
A96	TPM_PP	Trusted Platform Module (TPM) Physical Presence pin. Active high. TPM chip has an internal pull down. This signal is used to indicate Physical Presence to the TPM.	I	CMOS	3.3V / 3.3V	-	-
A97	TYPE10_CN	Dual use pin. Indicates to the Carrier Board that a Type 10 module is installed. Indicates to	-	-	-	Place test point	

		the Carrier that a Rev 1.0/2.0 module is installed					
A98	SER0_TX	General purpose serial port transmitter	O	CMOS	3.3V / 12V	Placeholder PD 4.7K	-
A99	SER0_RX	General purpose serial port receiver	I	CMOS	3.3V / 12V	Go through diode PU 47K to 3.3V	-
A100	GND	GND(FIXED)	-	-	-	-	-
A101	SER1_TX	General purpose serial port transmitter / CAN_TX	O	CMOS	3.3V / 12V	Placeholder PD 4.7K	-
A102	SER1_RX	General purpose serial port receiver / CAN_RX	I	CMOS	3.3V / 12V	Go through diode PU 47K to 3.3V	-
A103	LID#_CN	LID button. Low active signal used by the ACPI operating system for a LID switch.	I	CMOS	3.3V Suspend / 12V	Go through diode PU 47K to 3VSB	-
A104	+V12_A	Primary power input: +12V nominal.	-	PWR	+12V	-	-
A105	+V12_A	Primary power input: +12V nominal.	-	PWR	+12V	-	-
A106	+V12_A	Primary power input: +12V nominal.	-	PWR	+12V	-	-
A107	+V12_A	Primary power input: +12V nominal.	-	PWR	+12V	-	-

A108	+V12_A	Primary power input: +12V nominal.	-	PWR	+12V	-	-
A109	+V12_A	Primary power input: +12V nominal.	-	PWR	+12V	-	-
A110	GND	GND(FIXED)	-	-	-	-	-
B1	GND	GND(FIXED)	-	-	-	-	-
B2	L1_LINK#/ACT#	Gigabit Ethernet Controller 1 activity indicator, active low.	OD	CMOS	3.3V Suspend / 3.3V	-	-
B3	SOC_LPC_FRAME_N	LPC frame indicates the start of an LPC cycle / Shared pin with ESPI_CS0#	O	CMOS	3.3V / 3.3V	PU 8.2k ohm to 3.3V	-
B4	SOC_LPC_AD0	LPC multiplexed address, command and data bus / Shared pin with ESPI IO	I/O	CMOS	3.3V / 3.3V	-	-
B5	SOC_LPC_AD1	LPC multiplexed address, command and data bus / Shared pin with ESPI IO	I/O	CMOS	3.3V / 3.3V	-	-
B6	SOC_LPC_AD2	LPC multiplexed address, command and data bus / Shared pin with ESPI IO	I/O	CMOS	3.3V / 3.3V	-	-
B7	SOC_LPC_AD3	LPC multiplexed address, command and data bus / Shared pin with ESPI IO	I/O	CMOS	3.3V / 3.3V	-	-
B8	LPC_DRQ0# / ESPI_ALERT0#	LPC serial DMA request / Shared pin with ESPI_ALERT	I	CMOS	3.3V / 3.3V	-	-
B9	LPC_DRQ1# / ESPI_ALERT1#	LPC serial DMA request / Shared pin with ESPI_ALERT	I	CMOS	3.3V / 3.3V	-	-

B10	LPC_CLK1_CE	LPC clock output - 33MHz nominal / Shared pin with ESPI_Clock	O	CMOS	3.3V / 3.3V	-	-
B11	GND	GND(FIXED)	-	-	-	-	-
B12	PWRBTN#_D	Power button to bring system out of S5 (soft off), active on falling edge.	I	CMOS	3.3V Suspend / 3.3V	PU 10k ohm to 3VSB	-
B13	SMB_CLK_CN	System Management Bus bidirectional clock line.	I/O	CMOS	3.3V Suspend / 3.3V	Placeholder 0 ohm	-
B14	SMB_DATA_CN	System Management Bus bidirectional data line.	I/O	CMOS	3.3V Suspend / 3.3V	Placeholder 0 ohm	-
B15	SMB_ALRT_N_CN	System Management Bus Alert – active low input can be used to generate an SMI# (System Management Interrupt) or to wake the system.	I	CMOS	3.3V Suspend / 3.3V	Go through 0 ohm	-
B16	SATA1_PCIE17_TXP	Serial ATA or SAS Channel 1 transmit differential pair.	O	SATA	AC coupled on Module	-	-
B17	SATA1_PCIE17_TXN	Serial ATA or SAS Channel 1 transmit differential pair.	O	SATA	AC coupled on Module	-	-
B18	SUS_STAT_N_CN	Indicates imminent suspend operation; used to notify LPC devices / Shared pin with ESPI_RESET	O	CMOS	3.3V Suspend / 3.3V	-	-
B19	SATA1_PCIE17_RXP	Serial ATA or SAS Channel 1 receive differential pair.	I	SATA	AC coupled on Module	-	-

B20	SATA1_PCIE17_RXN	Serial ATA or SAS Channel 1 receive differential pair.	I	SATA	AC coupled on Module	-	-
B21	GND	GND(FIXED)	-	-	-	-	-
B22	PCIE_RX15+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B23	PCIE_RX15-	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B24	CB_PWROK	Power OK from main power supply. A high value indicates that the power is good. This signal can be used to hold off Module startup to allow carrier based FPGAs or other configurable devices time to be programmed.	I	CMOS	3.3V / 3.3V	-	-
B25	PCIE_RX14+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B26	PCIE_RX14-	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B27	WDTO#	Output indicating that a watchdog time-out event has occurred.	O	CMOS	3.3V / 3.3V	-	-
B28	SMB_LAN_CLK_CN	Reserved Pin	-	-	-	Placeholder 0 ohm -	-
B29	SMB_LAN_DAT_CN	Reserved Pin	-	-	-	Placeholder 0 ohm -	-
B30	SMB_LAN_ALT_CN	Reserved Pin	-	-	-	Placeholder 0 ohm -	-
B31	GND	GND(FIXED)	-	-	-	-	-

B32	SPKR_CN	Output for audio enunciator	O	CMOS	3.3V / 3.3V	NC	-
B33	I2C_CLK_CN	General purpose I2C port clock output	I/O	CMOS	3.3V Suspend / 3.3V	Placeholder PU 10k ohm to 3.3V	-
B34	I2C_DAT_CN	General purpose I2C port data I/O line	I/O	CMOS	3.3V Suspend / 3.3V	Placeholder PU 10k ohm to 3.3V	-
B35	PM_THRM_N	Input from off-Module temp sensor indicating an over-temp situation	I	CMOS	3.3V / 3.3V		-
B36	PCIE_RX13+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B37	PCIE_RX13-	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B38	GND	GND	-	-	-	-	-
B39	PCIE_RX12+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B40	PCIE_RX12-	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B41	GND	GND(FIXED)	-	-	-	-	-
B42	SOC_USB2_DN3	USB differential pairs, channels 3. All USB ports except USB7, if implemented, shall be host ports.	I/O	USB	3.3V Suspend / 3.3V	-	-

B43	SOC_USB2_DP3	USB differential pairs, channels 3. All USB ports except USB7, if implemented, shall be host ports.	I/O	USB	3.3V Suspend / 3.3V	-	-
B44	USB_OC0_1#	USB over-current sense, USB channels 0 and 1. A pull-up for this line shall be present on the Module. Do not pull this line high on the Carrier Board	I	CMOS	3.3V Suspend / 3.3V	Go through diode then PU 10K ohm	-
B45	SOC_USB2_DN1	USB differential pairs, channels 1. All USB ports except USB7, if implemented, shall be host ports.	I/O	USB	3.3V Suspend / 3.3V	-	-
B46	SOC_USB2_DP1	USB differential pairs, channels 1. All USB ports except USB7, if implemented, shall be host ports.	I/O	USB	3.3V Suspend / 3.3V	-	-
B47	ESPI_EN	This signal is used by the Carrier to indicate the operating mode of the LPC/eSPI bus. If pulled down by the Carrier LPC mode is selected. If pulled up or left floating, eSPI is selected if available. This signal is pulled up on the Module. This signal is a "don't care" for Modules that do not support eSPI	I	CMOS	NA	-	-
B48	USB0_HOST_PRSENT	Module USB client may detect the presence of a USB host on USB0.	I	CMOS	3.3V Suspend/ 3.3V	-	-

		A high value indicates that a host is present.					
B49	RSTBTN#_D	Reset button input. Active low request for module to reset and reboot. May be falling edge sensitive. For situations when SYS_RESET# is not able to reestablish control of the system, PWR_OK or a power cycle may be used	I	CMOS	3.3V Suspend / 3.3V	PU 4.7k ohm to 3VSB	-
B50	CBRST_CN	Reset output from Module to Carrier Board. Active low. Issued by Module chipset and may result from a low SYS_RESET#input, a low PWR_OKinput, a VCC_12Vpower input that falls below the minimum specification, a watchdog timeout, or maybe initiated by the Module software.	O	CMOS	3.3V Suspend / 3.3V		-
B51	GND	GND(FIXED)	-	-	-	-	-
B52	PCIE_RX_DP13	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B53	PCIE_RX_DN13	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-

B54	GPO1	General purpose output pins. Upon a hardware reset, these outputs should be low.	O	CMOS	3.3V / 3.3V	-	-
B55	PCIE_RX_DP12	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B56	PCIE_RX_DN12	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B57	GPO2	General purpose output pins. Upon a hardware reset, these outputs should be low.	O	CMOS	3.3V / 3.3V	-	-
B58	PCIE_RX_DP11	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B59	PCIE_RX_DN11	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B60	GND	GND(FIXED)	-	-	-	-	-
B61	PCIE_RX_DP10	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B62	PCIE_RX_DN10	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B63	GPO3	General purpose output pins. Upon a hardware reset, these outputs should be low.	O	CMOS	3.3V / 3.3V	-	-
B64	PCIE_RX_DP9	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B65	PCIE_RX_DN9	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-

B66	WAKE0#_CN	PCI Express wake up signal.	I	CMOS	3.3V Suspend / 3.3V	PU 1k ohm to 3VSB	-
B67	WAKE1#_CN	General purpose wake up signal. Maybe used to implement wake-up on PS2 keyboard or mouse activity	I	CMOS	3.3V Suspend / 3.3V	PU 1k ohm to 3VSB	-
B68	PCIE_RX_DP8	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B69	PCIE_RX_DN8	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B70	GND	GND(FIXED)	-	-	-	-	-
B71	PCIE_RX8+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B72	PCIE_RX8-	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B73	GND	GND	-	-	-	-	-
B74	PCIE_RX9+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B75	PCIE_RX9-	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B76	GND	GND	-	-	-	-	-
B77	PCIE_RX10+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B78	PCIE_RX10-	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B79	COME_B79	GND	-	-	-	-	-

B80	GND	GND(FIXED)	-	-	-	-	-
B81	PCIE_RX11+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B82	PCIE_RX11-	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B83	GND	GND	-	-	-	-	-
B84	+5VSB	Standby power input: +5.0V nominal.	-	PWR	+5.0V	-	-
B85	+5VSB	Standby power input: +5.0V nominal.	-	PWR	+5.0V	-	-
B86	+5VSB	Standby power input: +5.0V nominal.	-	PWR	+5.0V	-	-
B87	+5VSB	Standby power input: +5.0V nominal.	-	PWR	+5.0V	-	-
B88	BIOS_DIS1#	Selection straps to determine the BIOS boot device. The Carrier should only float these or pull them low / Shared pin with ESPI_BBS	I	CMOS	NA	PU 10k ohm to 3VSB	-
B89	NCSI_RX_ER_CN	NC-SI Receive error	O	-	3.3V Suspend / 3.3V	NC	-
B90	GND	GND(FIXED)	-	-	-	-	-
B91	NCSI_CLK_IN	NC-SI Clock reference for receive, transmit, and control interface. (PD 10K on Carrier when NC-SI is not used on Carrier)	I	-	3.3V Suspend / 3.3V	-	-

B92	NCSI_RXD_1	NC-SI Receive Data (from NC to BMC).	O	-	3.3V Suspend / 3.3V	Placeholder PU 10K to 3VSB	-
B93	NCSI_RXD_0	NC-SI Receive Data (from NC to BMC).	O	-	3.3V Suspend / 3.3V	Placeholder PU 10K to 3VSB	-
B94	NCSI_CRS_DV	NC-SI Carrier Sense/Receive Data Valid to MC, indicating that the transmitted data from NC to BMC is valid.	O	-	3.3V Suspend / 3.3V	Placeholder PD 10K	-
B95	NCSI_TXD_1_CN	NC-SI Transmit Data (from BMC to NC). (PD 10K on Carrier when NC-SI is not used on Carrier)	I	-	3.3V Suspend / 3.3V	PD 10K	-
B96	NCSI_TXD_0_CN	NC-SI Transmit Data (from BMC to NC). (PD 10K on Carrier when NC-SI is not used on Carrier)	I	-	3.3V Suspend / 3.3V	PD 10K	-
B97	SPI_CS_CN	Chip select for Carrier Board SPI - maybe sourced from chipset SPI0 or SPI1	O	CMOS	3.3V Suspend / 3.3V	-	-
B98	NCSI_ARB_IN_CN	NC-SI hardware arbitration input.	I	-	3.3V Suspend / 3.3V	PU 10k ohm to 3VSB	-
B99	NCSI_ARB_OUT	NC-SI hardware arbitration output.	O	-	3.3V Suspend / 3.3V		-
B100	GND	GND(FIXED)	-	-	-	-	-

B101	FAN_PWMOUT_CN	Fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the fan's RPM	O	CMOS	3.3V / 12V	Go through diode then PU 10K ohm	-
B102	FAN_TACHIN_CN	Fan tachometer input for a fan with a two pulse output.	I	CMOS	3.3V / 12V	Go through diode then PU 47K ohm	-
B103	SLEEP#_CN	Sleep button. Low active signal used by the ACPI operating system to bring the system to sleep state or to wake it up again.	I	CMOS	3.3V Suspend / 12V	Go through diode then PU 10K ohm	-
B104	+V12_A	Primary power input: +12V nominal.	-	PWR	+12V	-	-
B105	+V12_A	Primary power input: +12V nominal.	-	PWR	+12V	-	-
B106	+V12_A	Primary power input: +12V nominal.	-	PWR	+12V	-	-
B107	+V12_A	Primary power input: +12V nominal.	-	PWR	+12V	-	-
B108	+V12_A	Primary power input: +12V nominal.	-	PWR	+12V	-	-
B109	+V12_A	Primary power input: +12V nominal.	-	PWR	+12V	-	-
B110	GND	GND(FIXED)	-	-	-	-	-
C1	GND	GND(FIXED)	-	-	-	-	-
C2	GND	GND	-	-	-	-	-

C3	USB3_PCIE18_RXN0	Additional transmit signal differential pairs for the SuperSpeed USB data path.	I	PCIE	AC coupled off Module	-	-
C4	USB3_PCIE18_RXP0	Additional transmit signal differential pairs for the SuperSpeed USB data path.	I	PCIE	AC coupled off Module	-	-
C5	GND	GND	-	-	-	-	-
C6	USB3_PCIE19_RXN1	Additional transmit signal differential pairs for the SuperSpeed USB data path.	I	PCIE	AC coupled off Module	-	-
C7	USB3_PCIE19_RXP1	Additional transmit signal differential pairs for the SuperSpeed USB data path.	I	PCIE	AC coupled off Module	-	-
C8	GND	GND	-	-	-	-	-
C9	USB3_PCIE18_RXN2	Additional transmit signal differential pairs for the SuperSpeed USB data path.	I	PCIE	AC coupled off Module	-	-
C10	USB3_PCIE18_RXP2	Additional transmit signal differential pairs for the SuperSpeed USB data path.	I	PCIE	AC coupled off Module	-	-
C11	GND					-	-
C12	USB3_PCIE19_RXN3	Additional transmit signal differential pairs for the SuperSpeed USB data path.	I	PCIE	AC coupled off Module	-	-
C13	USB3_PCIE19_RXP3	Additional transmit signal differential pairs for the SuperSpeed USB data path.	I	PCIE	AC coupled off Module	-	-

C14	GND	GND	-	-	-	-	-
C15	10PHY_MDC3_CN	MDIO Mode: Management Data I/O interface mode clock signal for serial data transfers between the MAC and an external PHY.	O	-	3.3V Suspend / 3.3V	Placeholder 0 ohm to LAN_MDC	-
		I2C Mode: I2C clock signal, of the 2-wire management interface used for serial data transfers between the MAC and an external PHY.	I/O OD	-	3.3V Suspend / 3.3V	-	-
C16	10PHY_MDC2_CN	MDIO Mode: Management Data I/O interface mode clock signal for serial data transfers between the MAC and an external PHY.	O	-	3.3V Suspend / 3.3V	Placeholder 0 ohm to LAN_MDC	-
		I2C Mode: I2C clock signal, of the 2-wire management interface used for serial data transfers between the MAC and an external PHY.	I/O OD	-	3.3V Suspend / 3.3V	-	-
C17	LAN1_PORT0_SDP0	Software-Definable Pins. Can also be used for IEEE1588 support such as a 1pps signal	I/O	-	3.3V Suspend / 3.3V	-	-
C18	GND	GND	-	-	-	-	-
C19	PCIE_RX_DP14_CB	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C20	PCIE_RX_DN14_CB	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C21	GND	GND(FIXED)	-	-	-	-	-

C22	PCIE_RX_DP15	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C23	PCIE_RX_DN15	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C24	10G_INT2_CN	Interrupt pin from copper PHY or optical SFP Module to the 10GbE controller	I	-	3.3V Suspend / 3.3V	NC	-
C25	GND	GND	-	-	-	-	-
C26	LAN1_RX_DP1	10GBASE-KR ports, receive input differential pairs.	I	KR	AC coupled on Module	-	-
C27	LAN1_RX_DN1	10GBASE-KR ports, receive input differential pairs.	I	KR	AC coupled on Module	-	-
C28	GND	GND	-	-	-	-	-
C29	LAN1_RX_DP0	10GBASE-KR ports, receive input differential pairs.	I	KR	AC coupled on Module	-	-
C30	LAN1_RX_DN0	10GBASE-KR ports, receive input differential pairs.	I	KR	AC coupled on Module	-	-
C31	GND	GND(FIXED)	-	-	-	-	-
C32	LAN1_P1_I2C_DAT	I2C data signal of the 2-wire management interface used by the 10GbE controller to access the management registers of an external Optical SFP Module	I/O	OD	3.3V Suspend / 3.3V	PU 1K ohm to 3VSB	-
C33	LAN1_P0_I2C_DAT	I2C data signal of the 2-wire management interface used by the 10GbE controller to access	I/O	OD	3.3V Suspend / 3.3V	PU 1K ohm to 3VSB	-

		the management registers of an external Optical SFP Module					
C34	10GPHY_RST23_CN	Output signal that resets an optical PHY on port 2 and port3 (Not used with copper PHY)	O	-	3.3V Suspend / 3.3V	To pltrst	-
C35	10GPHY_RST01_CN	Output signal that resets an optical PHY on port 0 and port1 (Not used with copper PHY)	O	-	3.3V Suspend / 3.3V	To pltrst	-
C36	10G_LED_SDA_CN	I2C Data of the 2-wire interface that transfers LED signals and PHY straps for I2C or MDIO operation of optical PHYs.	I/O	OD	3.3V Suspend / 3.3V	Placeholder 2.2K ohm to 3VSB	-
C37	10G_LED_SCL_CN	I2C Clock, of the 2-wire interface that transfers LED and strap signals for I2C or MDIO operation of optical PHYs	I/O	OD	3.3V Suspend / 3.3V	Placeholder 2.2K ohm to 3VSB	-
C38	LAN0_P1_I2C_DAT	I2C data signal of the 2-wire management interface used by the 10GbE controller to access the management registers of an external Optical SFP Module	I/O	OD	3.3V Suspend / 3.3V	PU 1K ohm to 3VSB	-
C39	LAN0_P0_I2C_DAT	I2C data signal of the 2-wire management interface used by the 10GbE controller to access	I/O	OD	3.3V Suspend / 3.3V	PU 1K ohm to 3VSB	-

		the management registers of an external Optical SFP Module					
C40	LAN0_PORT0_SDP0	Software-Definable Pins. Can also be used for IEEE1588 support such as a 1pps signal	I/O	-	3.3V Suspend / 3.3V		-
C41	GND	GND(FIXED)	-	-	-	-	-
C42	LAN0_RX_DP1	10GBASE-KR ports, receive input differential pairs.	I	KR	AC coupled on Module	-	-
C43	LAN0_RX_DN1	10GBASE-KR ports, receive input differential pairs.	I	KR	AC coupled on Module	-	-
C44	GND	GND	-	-	-	-	-
C45	10PHY_MDC1_CN	MDIO Mode: Management Data I/O interface mode clock signal for serial data transfers between the MAC and an external PHY.	O	-	3.3V Suspend / 3.3V	- Placeholder 0 ohm to LAN_MDC	-
		I2C Mode: I2C clock signal, of the 2-wire management interface used for serial data transfers between the MAC and an external PHY.	I/O OD	-	3.3V Suspend / 3.3V	-	-
C46	10PHY_MDC0_CN	MDIO Mode: Management Data I/O interface mode clock signal for serial data transfers between the MAC and an external PHY.	O	-	3.3V Suspend / 3.3V	- Placeholder 0 ohm to LAN_MDC	-

		I2C Mode: I2C clock signal, of the 2-wire management interface used for serial data transfers between the MAC and an external PHY.	I/O OD	-	3.3V Suspend / 3.3V	-	-
C47	10G_INT0_CN	Interrupt pin from copper PHY or optical SFP Module to the 10GbE controller	I	-	3.3V Suspend / 3.3V	NC	-
C48	GND	GND	-	-	-	-	-
C49	LAN0_RX_DP0	10GBASE-KR ports, receive input differential pairs.	I	KR	AC coupled on Module	-	-
C50	LAN0_RX_DN0	10GBASE-KR ports, receive input differential pairs.	I	KR	AC coupled on Module	-	-
C51	GND	GND(FIXED)	-	-	-	-	-
C52	PCIE_RX_DP0	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C53	PCIE_RX_DN0	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C54	TYPE0	The TYPE pins indicate to the Carrier Board the Pin-out Type that is implemented on the Module.	-	-	-	PD 0 ohm	-
C55	PCIE_RX_DP1	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C56	PCIE_RX_DN1	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-

C57	TYPE1	The TYPE pins indicate to the Carrier Board the Pin-out Type that is implemented on the Module.	-	-	-	Placeholder PD 0 phm	-
C58	PCIE_RX_DP2	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C59	PCIE_RX_DN2	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C60	GND	GND(FIXED)	-	-	-	-	-
C61	PCIE_RX_DP3	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C62	PCIE_RX_DN3	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C63	RSVD	Reserved Pin	-	-	-	-	-
C64	RSVD	Reserved Pin	-	-	-	-	-
C65	PCIE_RX_DP4	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C66	PCIE_RX_DN4	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C67	RAPID_SUTDN	Trigger for Rapid Shutdown. Must be driven to 5V though a <=50 ohm source impedance for a	I	CMOS	5.0V Suspend/ 5.0V	PD 150 ohm	-
C68	PCIE_RX_DP5	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C69	PCIE_RX_DN5	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C70	GND	GND(FIXED)	-	-	-	-	-

C71	PCIE_RX_DP6	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C72	PCIE_RX_DN6	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C73	GND	GND	-	-	-	-	-
C74	PCIE_RX_DP7	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C75	PCIE_RX_DN7	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C76	GND	GND	-	-	-	-	-
C77	RSVD	Reserved Pin	-	-	-	-	-
C78	PCIE_RX24+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C79	PCIE_RX24-	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C80	GND	GND(FIXED)	-	-	-	-	-
C81	PCIE_RX25+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C82	PCIE_RX25-	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C83	RSVD	Reserved Pin	-	-	-	-	-
C84	GND	GND	-	-	-	-	-
C85	PCIE_RX26+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C86	PCIE_RX26-	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C87	GND	GND	-	-	-	-	-

C88	PCIE_RX27+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C89	PCIE_RX27-	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C90	GND	GND(FIXED)	-	-	-	-	-
C91	PCIE_RX28+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C92	PCIE_RX28-	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C93	GND	GND	-	-	-	-	-
C94	PCIE_RX29+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C95	PCIE_RX29-	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C96	GND	GND	-	-	-	-	-
C97	RSVD	Reserved Pin	-	-	-	-	-
C98	PCIE_RX30+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C99	PCIE_RX30-	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C100	GND	GND(FIXED)	-	-	-	-	-
C101	PCIE_RX31+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C102	PCIE_RX31-	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C103	GND	GND	-	-	-	-	-

C104	+V12_A	Primary power input: +12V nominal.	-	PWR	+12V	-	-
C105	+V12_A	Primary power input: +12V nominal.	-	PWR	+12V	-	-
C106	+V12_A	Primary power input: +12V nominal.	-	PWR	+12V	-	-
C107	+V12_A	Primary power input: +12V nominal.	-	PWR	+12V	-	-
C108	+V12_A	Primary power input: +12V nominal.	-	PWR	+12V	-	-
C109	+V12_A	Primary power input: +12V nominal.	-	PWR	+12V	-	-
C110	GND	GND(FIXED)	-	-	-	-	-
D1	GND	GND(FIXED)	-	-	-	-	-
D2	GND	GND	-	-	-	-	-
D3	USB3_PCIE18_TXN0	Additional transmit signal differential pairs for the SuperSpeed USB data path.	O	PCIE	AC coupled on Module	-	-
D4	USB3_PCIE18_TXP0	Additional transmit signal differential pairs for the SuperSpeed USB data path.	O	PCIE	AC coupled on Module	-	-
D5	GND	GND	-	-	-	-	-
D6	USB3_PCIE19_TXN1	Additional transmit signal differential pairs for the SuperSpeed USB data path.	O	PCIE	AC coupled on Module	-	-

D7	USB3_PCIE19_TXP1	Additional transmit signal differential pairs for the SuperSpeed USB data path.	O	PCIE	AC coupled on Module	-	-
D8	GND	GND	-	-	-	-	-
D9	USB3_PCIE18_TXN2	Additional transmit signal differential pairs for the SuperSpeed USB data path.	O	PCIE	AC coupled on Module	-	-
D10	USB3_PCIE18_TXP2	Additional transmit signal differential pairs for the SuperSpeed USB data path.	O	PCIE	AC coupled on Module	-	-
D11	GND	GND(FIXED)	-	-	-	-	-
D12	USB3_PCIE19_TXN3	Additional transmit signal differential pairs for the SuperSpeed USB data path.	O	PCIE	AC coupled on Module	-	-
D13	USB3_PCIE19_TXP3	Additional transmit signal differential pairs for the SuperSpeed USB data path.	O	PCIE	AC coupled on Module	-	-
D14	GND	GND	-	-	-	-	-
D15	10PHY_MDA3_CN	MDIO Mode: Management Data I/O interface mode data signal for serial data transfers between the MAC and an external PHY.	O	-	3.3V Suspend / 3.3V	- Placeholder 0 ohm to LAN_MDIO	-
		I2C Mode: I2C data signal, of the 2-wire management interface used for serial data transfers between the MAC and an external PHY.	I/O OD	-	3.3V Suspend / 3.3V	-	-

D16	10PHY_MDA2_CN	MDIO Mode: Management Data I/O interface mode data signal for serial data transfers between the MAC and an external PHY.	O	-	3.3V Suspend / 3.3V	Placeholder 0 ohm to LAN_MDIO	-
		I2C Mode: I2C data signal, of the 2-wire management interface used for serial data transfers between the MAC and an external PHY.	I/O OD	-	3.3V Suspend / 3.3V	-	-
D17	LAN1_PORT1_SDP0	Software-Definable Pins. Can also be used for IEEE1588 support such as a 1pps signal	I/O	-	3.3V Suspend / 3.3V		-
D18	GND	GND	-	-	-	-	-
D19	PCIE_TX6+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D20	PCIE_TX6-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D21	GND(FIXED)	GND(FIXED)	-	-	-	-	-
D22	PCIE_TX7+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D23	PCIE_TX7-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D24	10G_INT3_CN	Interrupt pin from copper PHY or optical SFP Module to the 10GbE controller	I	-	3.3V Suspend / 3.3V	NC	-
D25	GND	GND	-	-	-	-	-

D26	LAN1_TX_DP1	10GBASE-KR ports, transmit output differential pairs.	O	KR	AC coupled on Carrier	-	-
D27	LAN1_TX_DN1	10GBASE-KR ports, transmit output differential pairs.	O	KR	AC coupled on Carrier	-	-
D28	GND	GND	-	-	-	-	-
D29	LAN1_TX_DP0	10GBASE-KR ports, transmit output differential pairs.	O	KR	AC coupled on Carrier	-	-
D30	LAN1_TX_DN0	10GBASE-KR ports, transmit output differential pairs.	O	KR	AC coupled on Carrier	-	-
D31	GND	GND(FIXED)	-	-	-	-	-
D32	LAN1_P1_I2C_CLK	I2C clock signal of the 2-wire management interface used by the 10GbE controller to access the management registers of an external Optical SFP Module	I/O	OD	3.3V Suspend / 3.3V	PU 1K ohm to 3VSB	-
D33	LAN1_P0_I2C_CLK	I2C clock signal of the 2-wire management interface used by the 10GbE controller to access the management registers of an external Optical SFP Module	I/O	OD	3.3V Suspend / 3.3V	PU 1K ohm to 3VSB	-
D34	10GPHY_SEL23_CN	Phy mode select pin: If high Phy2 and Phy3 are configured by MDIO. If low Phy2 and Phy3 are configured by I2C. For MDIO mode, this pin should be left not connected on the Carrier. For I2C	I	-	3.3V Suspend / 3.3V	-	-

		mode pull down with 1K on Carrier					
D35	10GPHY_SEL01_CN	Phy mode select pin: If high Phy0 and Phy1 are configured by MDIO. If low Phy2 and Phy3 are configured by I2C. For MDIO mode, this pin should be left not connected on the Carrier. For I2C mode pull down with 1K on Carrier	I	-	3.3V Suspend / 3.3V	-	-
D36	RSVD	RSVD	-	-	-	-	-
D37	RSVD	RSVD	-	-	-	-	-
D38	LAN0_P1_I2C_CLK	I2C clock signal of the 2-wire management interface used by the 10GbE controller to access the management registers of an external Optical SFP Module	I/O	OD	3.3V Suspend / 3.3V	PU 1K ohm to 3VSB	-
D39	LAN0_P0_I2C_CLK	I2C clock signal of the 2-wire management interface used by the 10GbE controller to access the management registers of an external Optical SFP Module	I/O	OD	3.3V Suspend / 3.3V	PU 1K ohm to 3VSB	-

D40	LAN0_PORT1_SDP0	Software-Definable Pins. Can also be used for IEEE1588 support such as a 1pps signal	I/O	-	3.3V Suspend / 3.3V	-	-
D41	GND	GND(FIXED)	-	-	-	-	-
D42	LAN0_TX_DP1	10GBASE-KR ports, transmit output differential pairs.	O	KR	AC coupled on Carrier	-	-
D43	LAN0_TX_DN1	10GBASE-KR ports, transmit output differential pairs.	O	KR	AC coupled on Carrier	-	-
D44	GND	GND	-	-	-	-	-
D45	10PHY_MDA1_CN	MDIO Mode: Management Data I/O interface mode data signal for serial data transfers between the MAC and an external PHY.	O	-	3.3V Suspend / 3.3V	Placeholder 0 ohm to LAN_MDIO	-
		I2C Mode: I2C data signal, of the 2-wire management interface used for serial data transfers between the MAC and an external PHY.	I/O OD	-	3.3V Suspend / 3.3V	-	-
D46	10PHY_MDA0_CN	MDIO Mode: Management Data I/O interface mode data signal for serial data transfers between the MAC and an external PHY.	O	-	3.3V Suspend / 3.3V	Placeholder 0 ohm to LAN_MDIO	-
		I2C Mode: I2C data signal, of the 2-wire management interface used for serial data transfers between the MAC and an external PHY.	I/O OD	-	3.3V Suspend / 3.3V	-	-

D47	10G_INT1_CN	Interrupt pin from copper PHY or optical SFP Module to the 10GbE controller	I	-	3.3V Suspend / 3.3V	NC	-
D48	GND	GND	-	-	-	-	-
D49	LAN0_TX_DP0	10GBASE-KR ports, transmit output differential pairs.	O	KR	AC coupled on Carrier	-	-
D50	LAN0_TX_DN0	10GBASE-KR ports, transmit output differential pairs.	O	KR	AC coupled on Carrier	-	-
D51	GND	GND(FIXED)	-	-	-	-	-
D52	PCIE_TX_DP0	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D53	PCIE_TX_DN0	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D54	CFG9	Reserved Pin	-	-	-	-	-
D55	PCIE_TX_DP1	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D56	PCIE_TX_DN1	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D57	TYPE2	The TYPE pins indicate to the Carrier Board the Pin-out Type that is implemented on the Module.	-	-	-	PD 0 ohm	-
D58	PCIE_TX_DP2	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D59	PCIE_TX_DN2	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D60	GND	GND(FIXED)	-	-	-	-	-

D61	PCIE_TX_DP3	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D62	PCIE_TX_DN3	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D63	RSVD	Reserved Pin	-	-	-	-	-
D64	RSVD	Reserved Pin	-	-	-	-	-
D65	PCIE_TX_DP4	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D66	PCIE_TX_DN4	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D67	GND	GND	-	-	-	-	-
D68	PCIE_TX_DP5	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D69	PCIE_TX_DN5	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D70	GND	GND(FIXED)	-	-	-	-	-
D71	PCIE_TX_DP6	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D72	PCIE_TX_DN6	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D73	GND	GND	-	-	-	-	-
D74	PCIE_TX_DP7	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D75	PCIE_TX_DN7	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D76	GND	GND	-	-	-	-	-
D77	RSVD	Reserved Pin	-	-	-	-	-

D78	PCIE_TX24+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D79	PCIE_TX24-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D80	GND	GND(FIXED)	-	-	-	-	-
D81	PCIE_TX25+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D82	PCIE_TX25-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D83	RSVD	Reserved Pin	-	-	-	-	-
D84	GND	GND	-	-	-	-	-
D85	PCIE_TX26+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D86	PCIE_TX26-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D87	GND	GND	-	-	-	-	-
D88	PCIE_TX27+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D89	PCIE_TX27-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D90	GND	GND(FIXED)	-	-	-	-	-
D91	PCIE_TX28+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D92	PCIE_TX28-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D93	GND	GND	-	-	-	-	-

D94	PCIE_TX29+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D95	PCIE_TX29-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D96	GND	GND	-	-	-	-	-
D97	RSVD	Reserved Pin	-	-	-	-	-
D98	PCIE_TX30+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D99	PCIE_TX30-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D100	GND	GND(FIXED)	-	-	-	-	-
D101	PCIE_TX31+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D102	PCIE_TX31-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D103	GND	GND	-	-	-	-	-
D104	+V12_A	Primary power input: +12V nominal.	-	PWR	+12V	-	-
D105	+V12_A	Primary power input: +12V nominal.	-	PWR	+12V	-	-
D106	+V12_A	Primary power input: +12V nominal.	-	PWR	+12V	-	-
D107	+V12_A	Primary power input: +12V nominal.	-	PWR	+12V	-	-
D108	+V12_A	Primary power input: +12V nominal.	-	PWR	+12V	-	-

D109	+V12_A	Primary power input: +12V nominal.	-	PWR	+12V	-	-
D110	GND	GND(FIXED)	-	-	-	-	-

Table 10 Pin out Description

6 BIOS Setup Items

PCOM-B702GT is equipped with the AMI BIOS stored in Flash ROM. These BIOS has a built-in Setup program that allows users to modify the basic system configuration easily. This type of information is stored in CMOS RAM so that it is retained during power-off periods. When system is turned on, PCOM-B702GT communicates with peripheral devices and checks its hardware resources against the configuration information stored in the CMOS memory. If any error is detected, or the CMOS parameters need to be initially defined, the diagnostic program will prompt the user to enter the SETUP program. Some errors are significant enough to abort the start up.

6.1 Entering Setup -- Launch System Setup

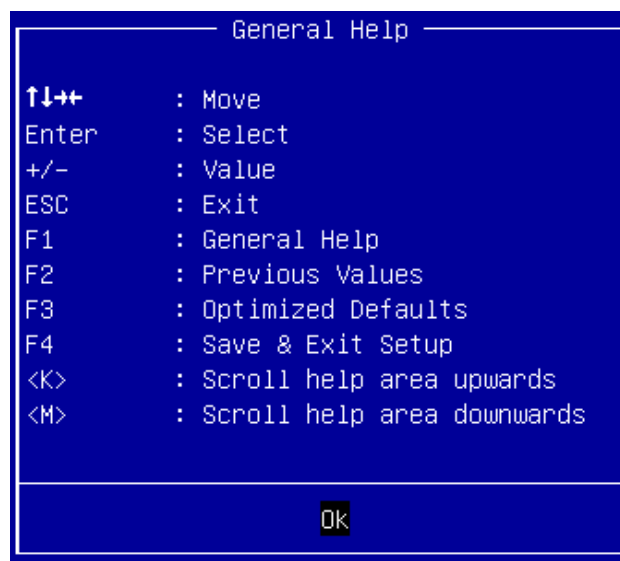
Power on the computer and the system will start POST (Power on Self-Test) process. When the message below appears on the screen, press key will enter BIOS setup screen.

Press to enter SETUP

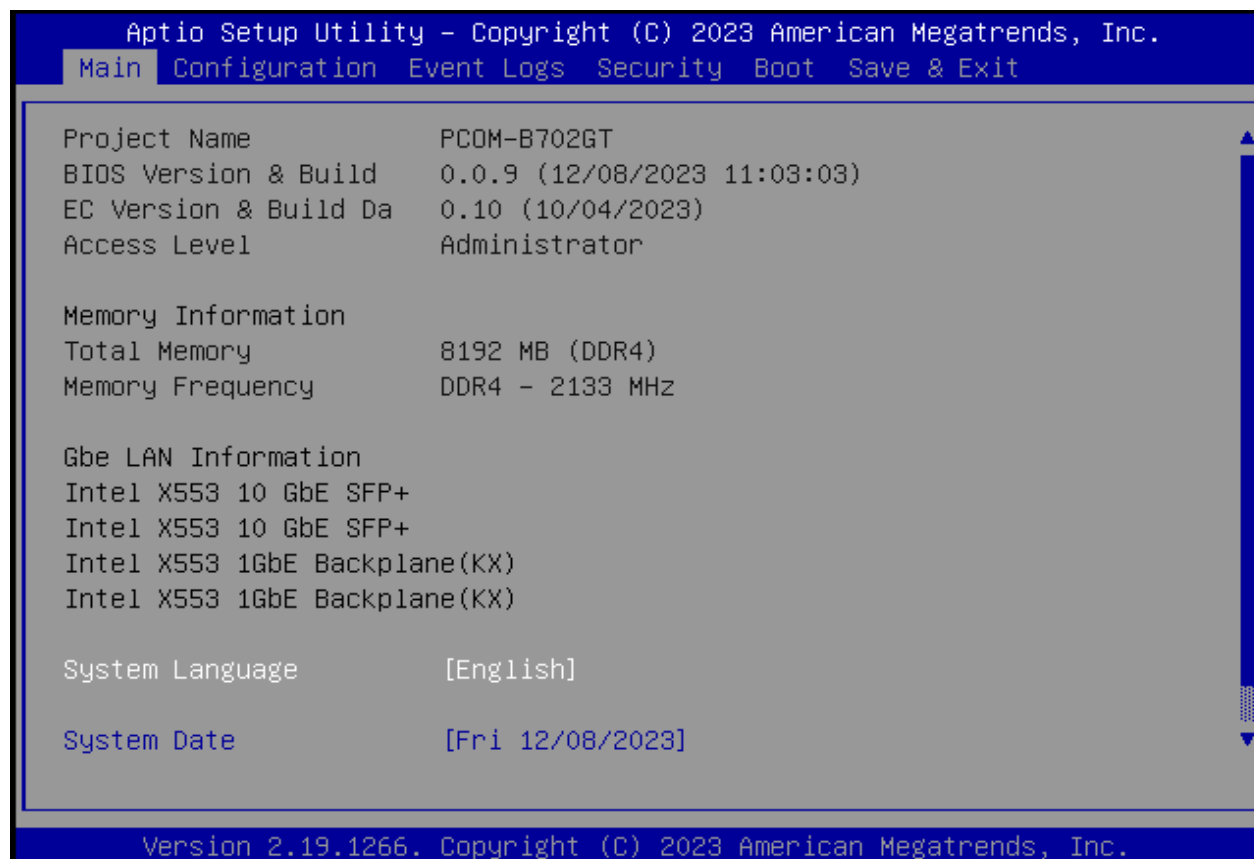
If the message disappears before responding and still wish to enter Setup, please restart the system by turning it OFF and On or pressing the RESET button. It can be also restarted by pressing <Ctrl>, <Alt>, and <Delete> keys on keyboard simultaneously.

Press <F1> to Run General Help or Resume

The BIOS setup program provides a General Help screen. The menu can be easily called up from any menu by pressing <F1>. The Help screen lists all the possible keys to use and the selections for the highlighted item. Press <Esc> to exit the Help screen.

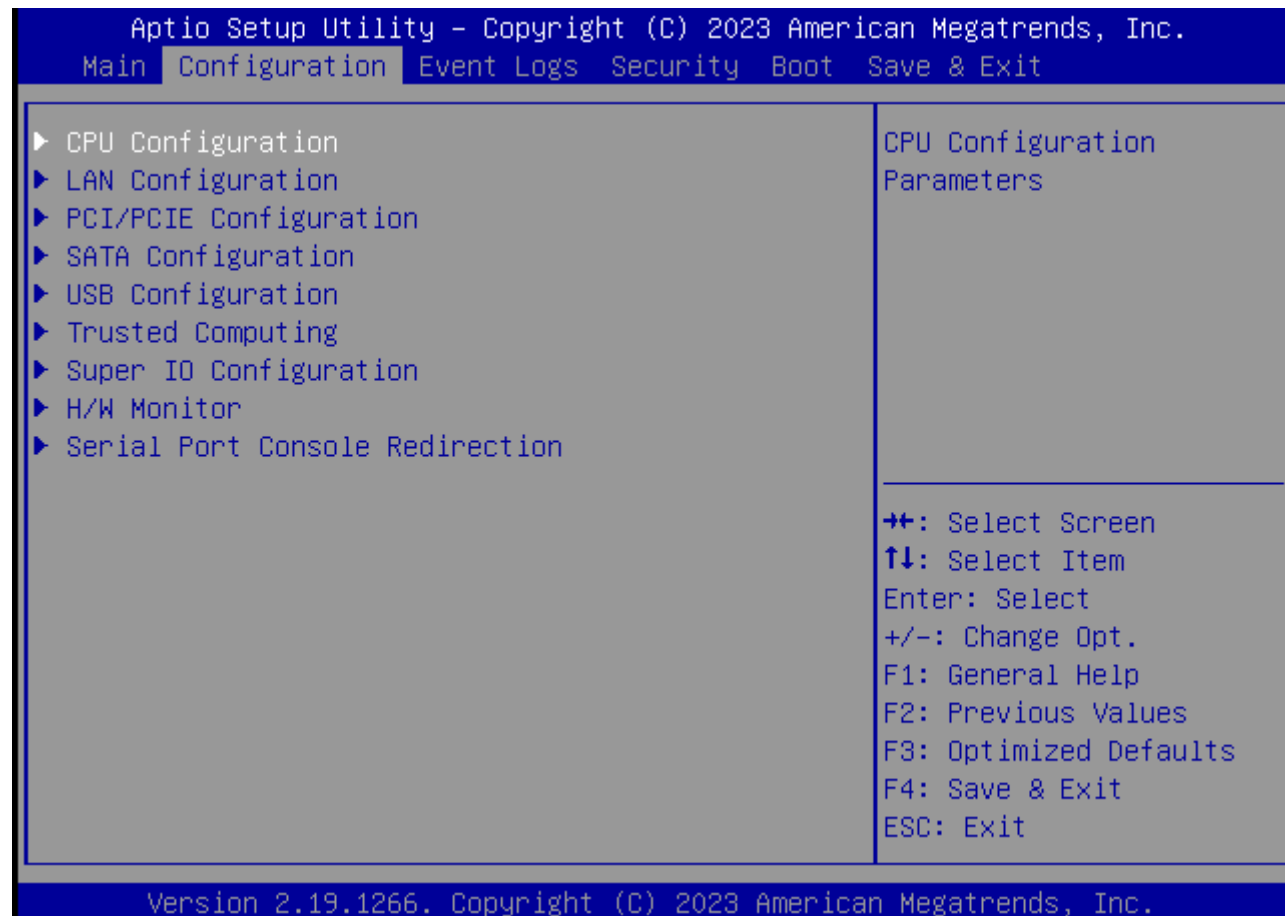


6.2 Main

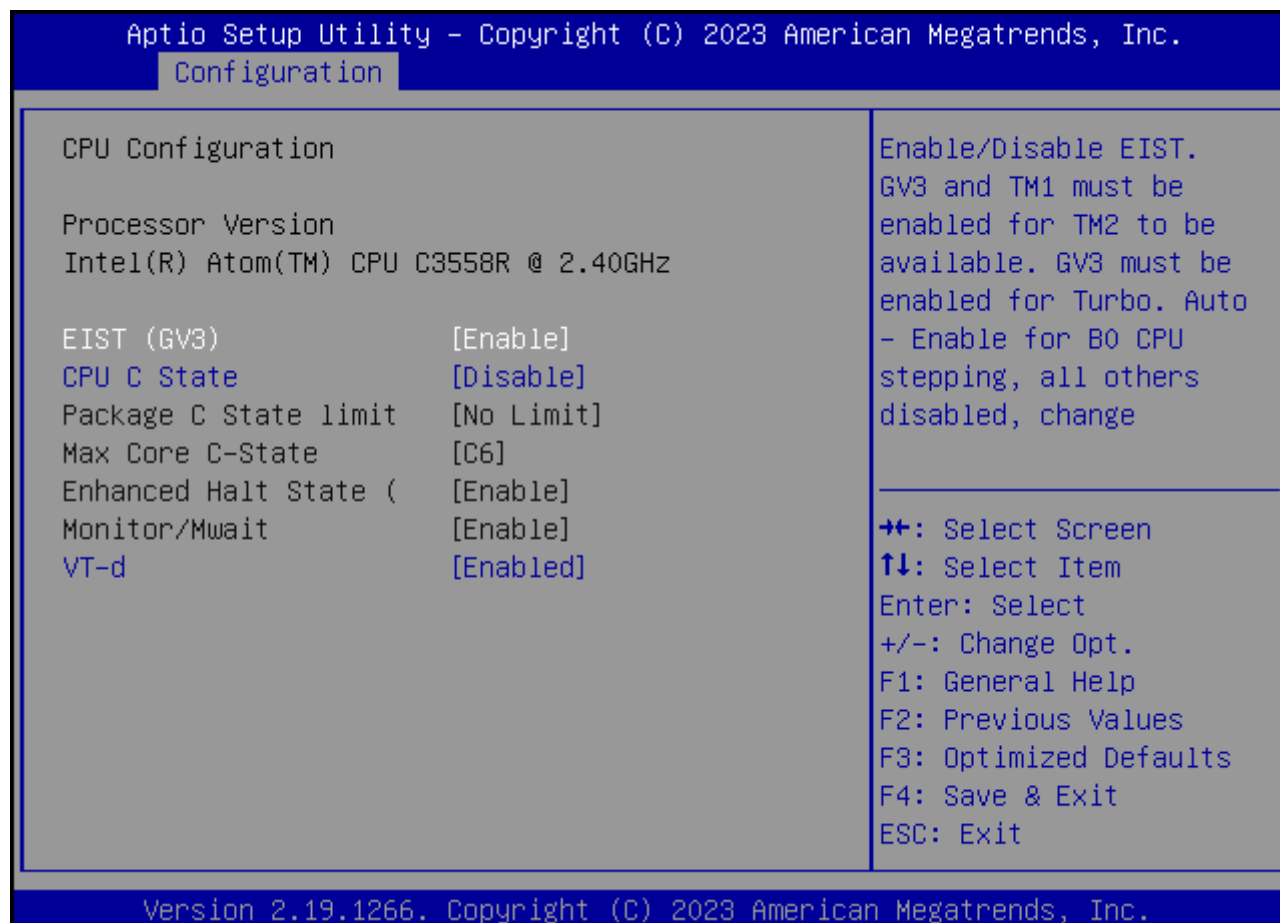


Feature	Description	Options
System Date	The date format is <Day>, <Month> <Date> <Year>. Use [+] or [-] to configure system Date.	
System Time	The time format is <Hour> <Minute> <Second>. Use [+] or [-] to configure system Time.	

6.3 Configuration

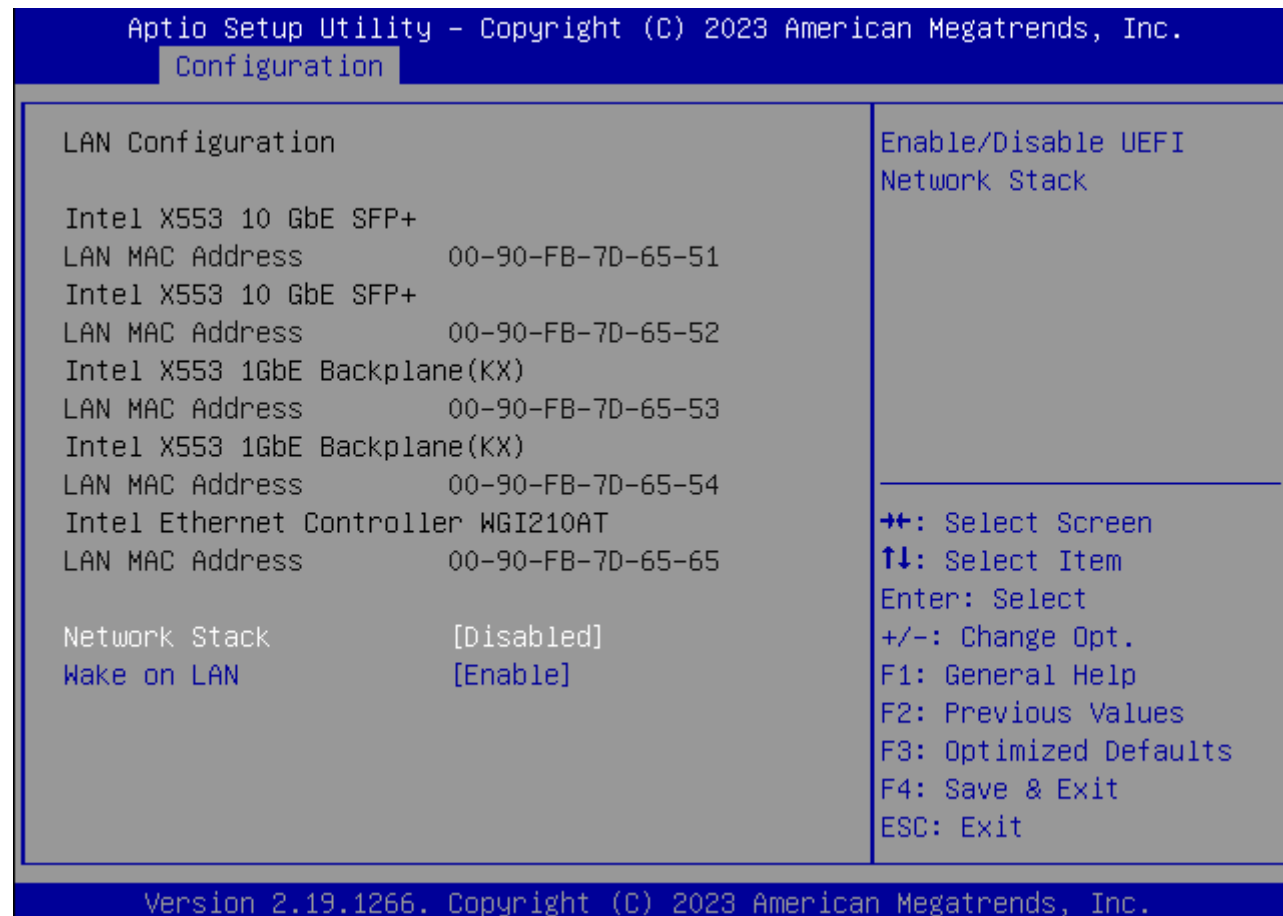


CPU



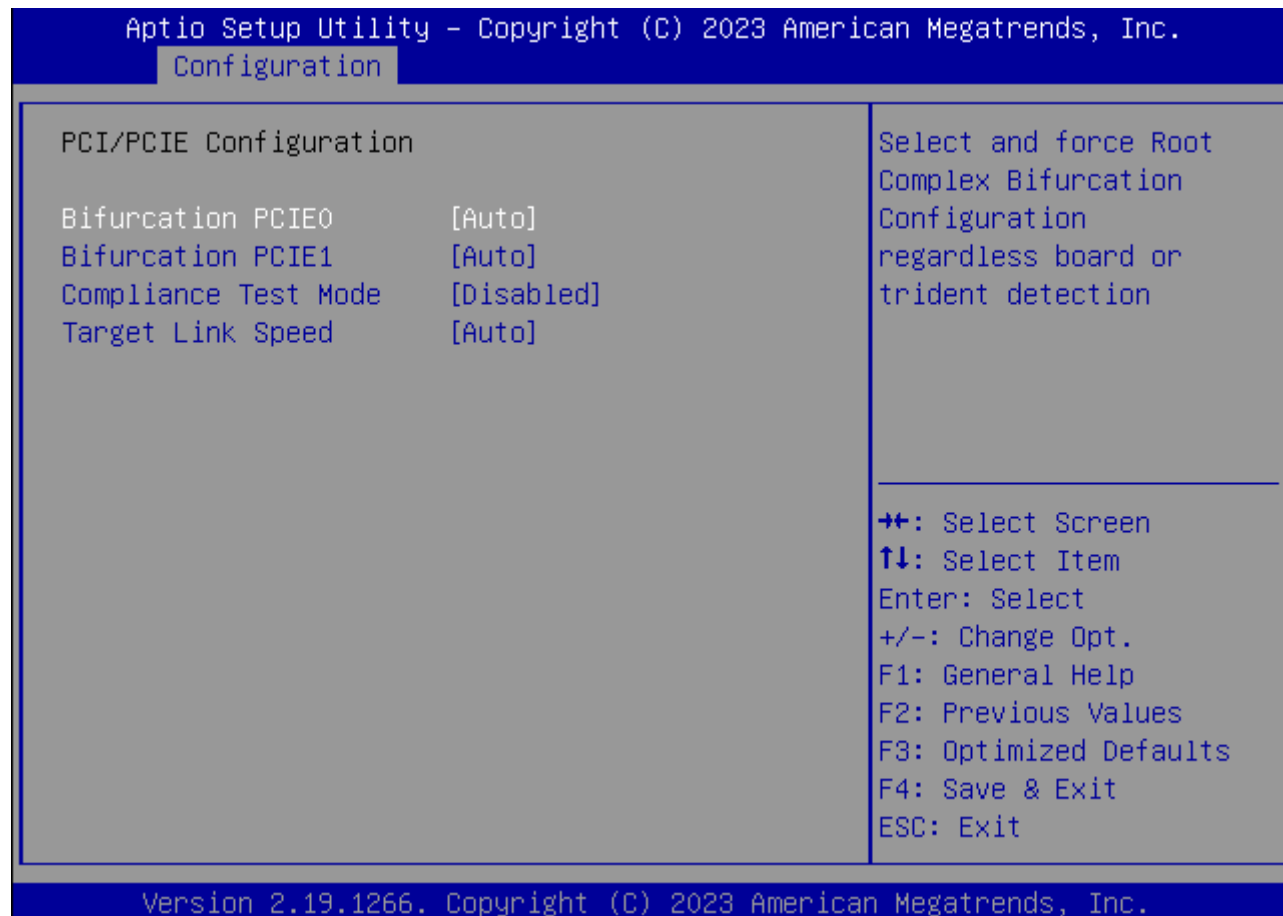
Feature	Description	Options
EIST (GV3)	Enable / Disable EIST. GV3 and TM1 must be enabled for TM2 to be available. GV3 must be enabled for Turbo. Auto – Enable for B0 CPU stepping, all others disabled, change	★Enabled, Disabled
CPU C State	Enables the Enhanced Ch state of the CPU, takes effect after reboot. Auto – Enable for B0 CPU stepping, all others disabled, change setting to override.	Enabled, ★Disabled
CPU C State [Enabled]		
Package C State limit	Package C State limit	★No Limit, No Pkg C-State, No S0Ix
Max Core C-State	Options are: C1 and C6.	★C6, C1
Enhanced Halt State	Enables the Enhanced C1E state of the CPU, takes effect after reboot.	★Enabled, Disabled
Monitor / Mwait	Enable or Disable the Monitor / Mwait instruction	★Enabled, Disabled
VT-d	Option to Enable / Disable VT-d	★Enabled, Disabled

LAN



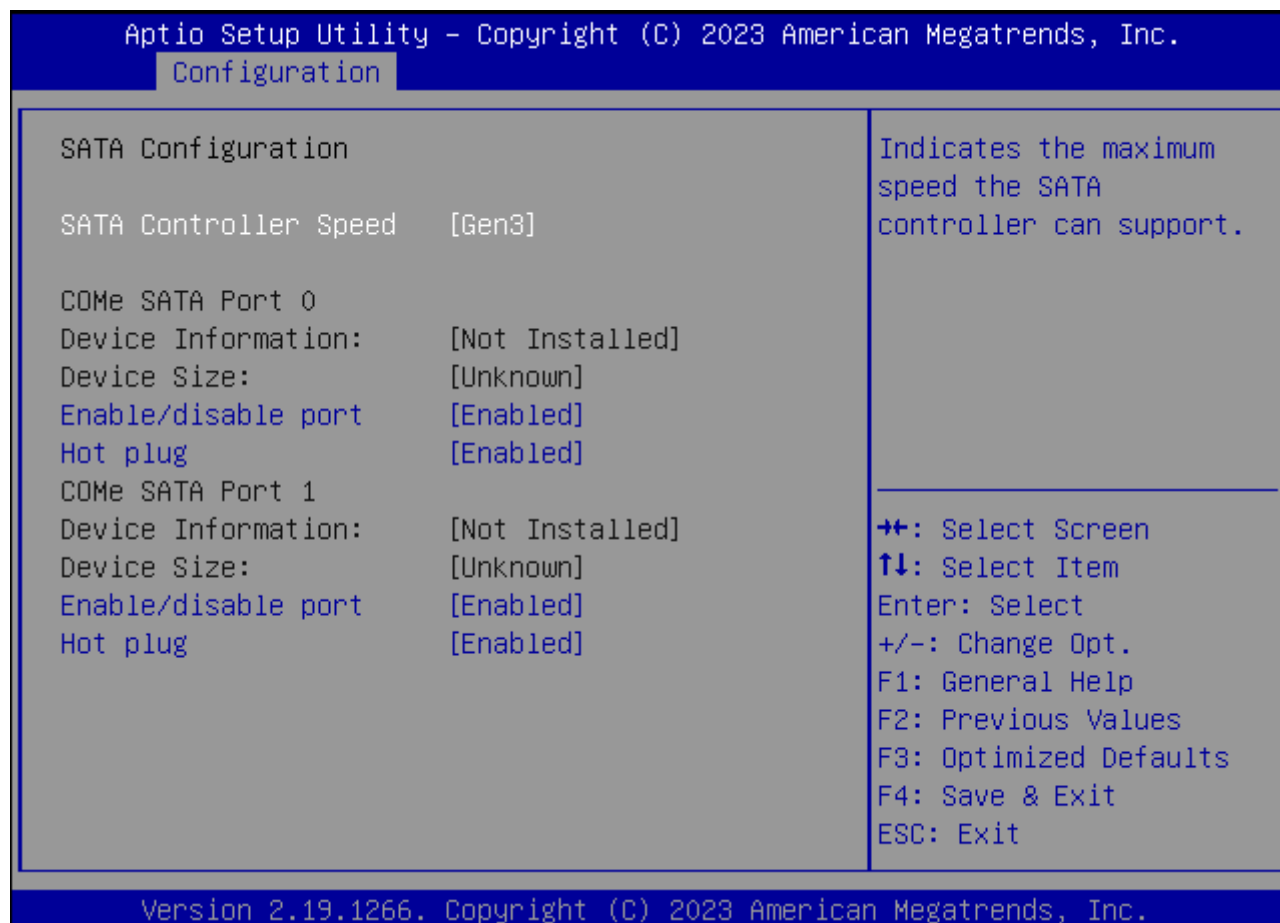
Feature	Description	Options
Network Stack	Enable/disable UEFI Network Stack	★Disabled, Enable
Network Stack [Enable]		
Ipv4 PXE Support	Enable Ipv4 PXE Boot Support. If disabled Ipv4 PXE boot support will not be available.	★Enabled, Disabled
Ipv4 HTTP Support	Enable Ipv4 HTTP Boot Support. If disabled Ipv4 HTTP boot support will not be available.	★Disabled, Enabled
Ipv6 PXE Support	Enable Ipv6 PXE Boot Support. If disabled Ipv6 PXE boot support will not be available.	★Enabled, Disabled
Ipv6 HTTP Support	Enable Ipv6 HTTP Boot Support. If disabled Ipv6 HTTP boot support will not be available.	★Disabled, Enabled
Ipv6 Configuration Pol	Set IP6 Configuration Policy	★Automatic, Manual
Wake On LAN	Enable or Disable integrated LAN to wake the system. (The wake on LAN cannot be disabled if ME is on at Sx state.)	★Enabled , Disabled

PCI/PCIE Configuration



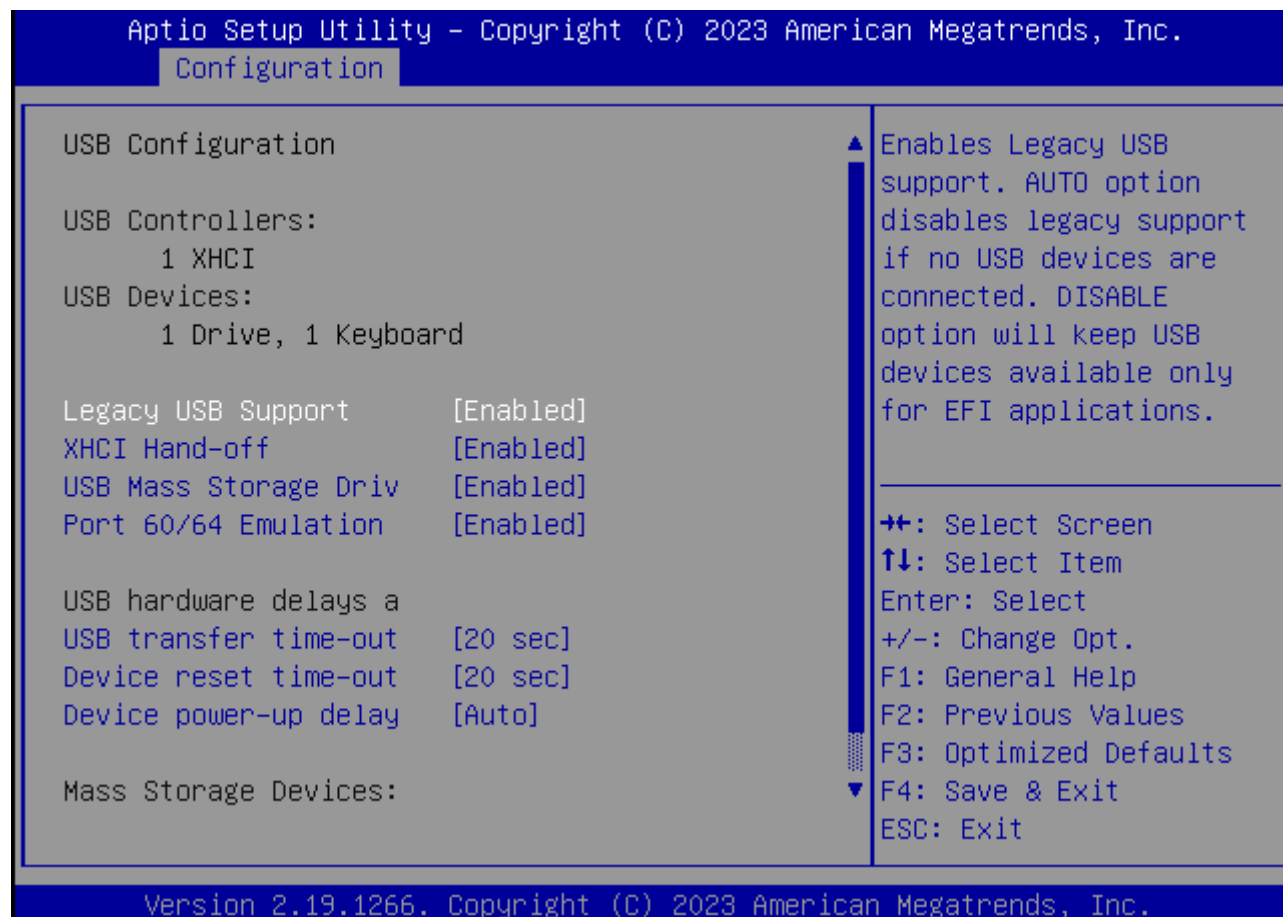
Feature	Description	Options
Bifurcation PCIE0	Select and force Root Complex Bifurcation regardless board or trident detection	★Auto, x8,x4x4,x4x2x2 x2x2x4,x2x2x2x2
Bifurcation PCIE1	Select and force Root Complex Bifurcation regardless board or trident detection	★Auto, x8,x4x4,x4x2x2 x2x2x4,x2x2x2x2
Compliance Test Mode	Enable when using Compliance Load Board	★Disabled, Enabled
Target Link Speed	If supported by hardware and set to 'Force to X.X GT/S' for Downstream Ports, this sets an upper limit on Link operational speed by restricting the values advertised by	★Auto, Force to 2.5GT/s, Force to 5.0GT/s Force to 8.0GT/s

SATA Configuration



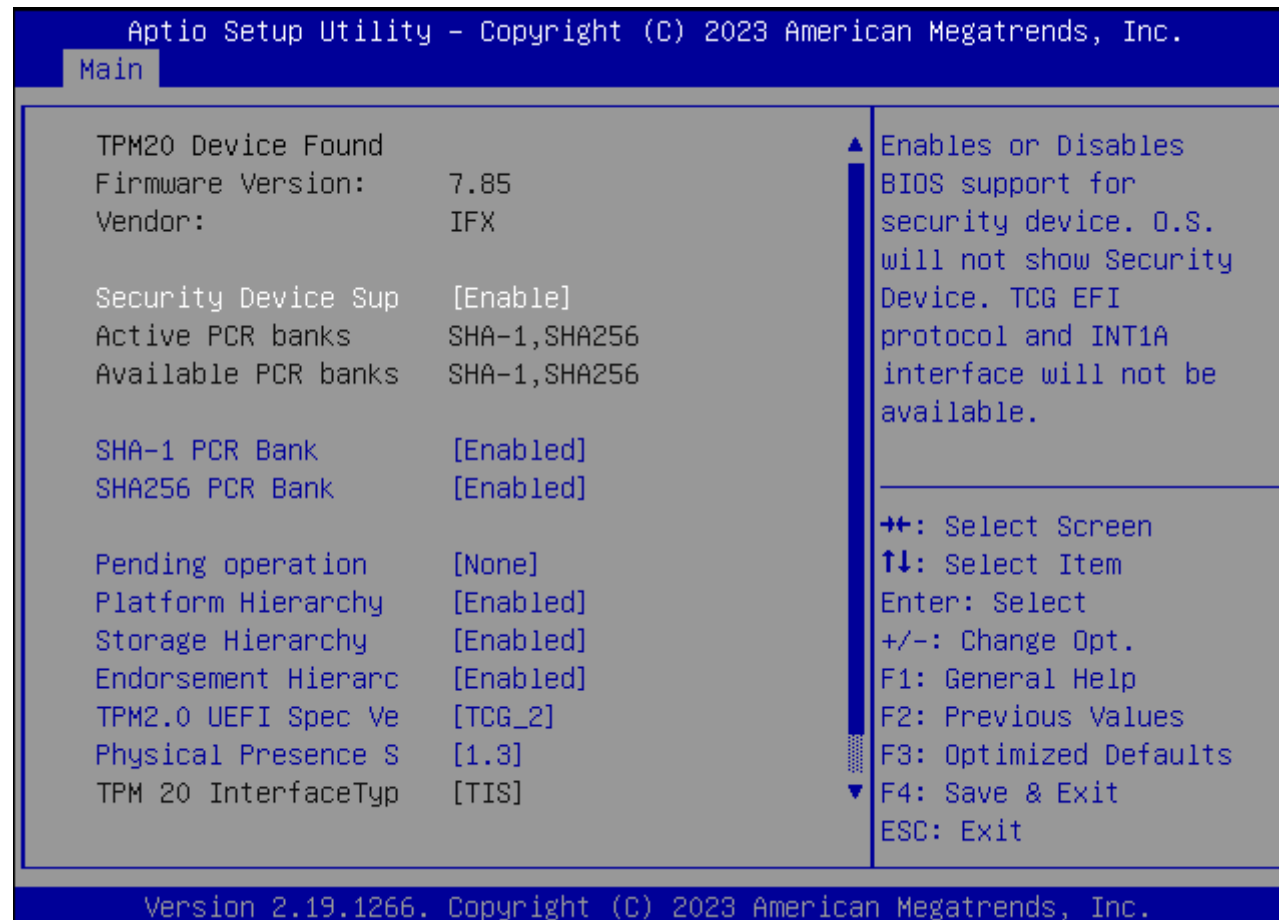
Feature	Description	Options
SATA Controller speed	Indicates the maximum speed the SATA controller can support.	★Gen3, Default, Gen1, Gen2
Enable / disable port	Enables / Disables SATA Controller port if supported by current CPU SKU.	★Enabled , Disabled
Hot plug	Hot plug.	★Enabled , Disabled

USB Configuration



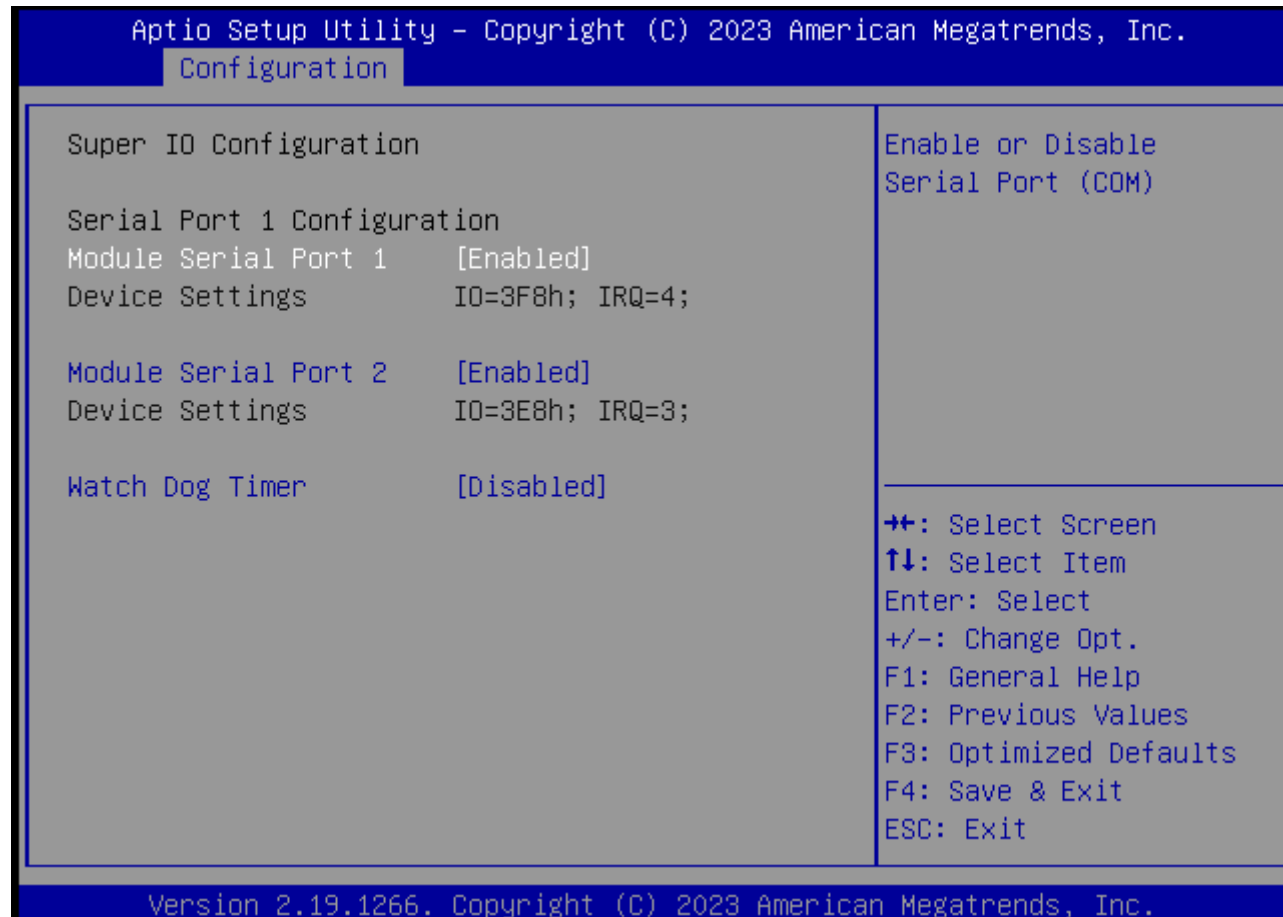
Feature	Description	Options
Legacy USB Support	Enables Legacy USB support. AUTO option disables legacy support if no USB devices are connected. DISABLE option will keep USB devices available only for EFI application	★Enabled , Disabled, Auto
XHCI Hand-off	This is a workaround for OSes without XHCI hand-off support. The XHCI ownership change should be claimed by XHCI driver	★Enabled , Disabled
USB Mass Storage Driver	Enable/Disable USB Mass Storage Driver Support	★Enabled , Disabled
Port 60/64 Emulation	Enables I/O port 60h/64h emulation support. This should be enabled for the complete USB keyboard legacy support for non-USB aware OSes.	★Enabled , Disabled
USB transfer time-out	The time-out value for Control, Bulk, and Interrupt transfers.	1, 5, 10, ★20 sec
Device reset time-out	USB mass storage device Start Unit command time-out.	10, ★20, 30, 40 sec
Device power-up delay	Maximum time the device will take before it properly reports itself to the Host Controller. 'AUTO' uses default value: for a Root port it is 100 ms, for a Hub port the delay is taken.	★AUTO, Manual
Device power-up delay [Manual]		
Device power-up delay	Delay range is 1~40 seconds, in one second increments.	★5

Trusted Computing



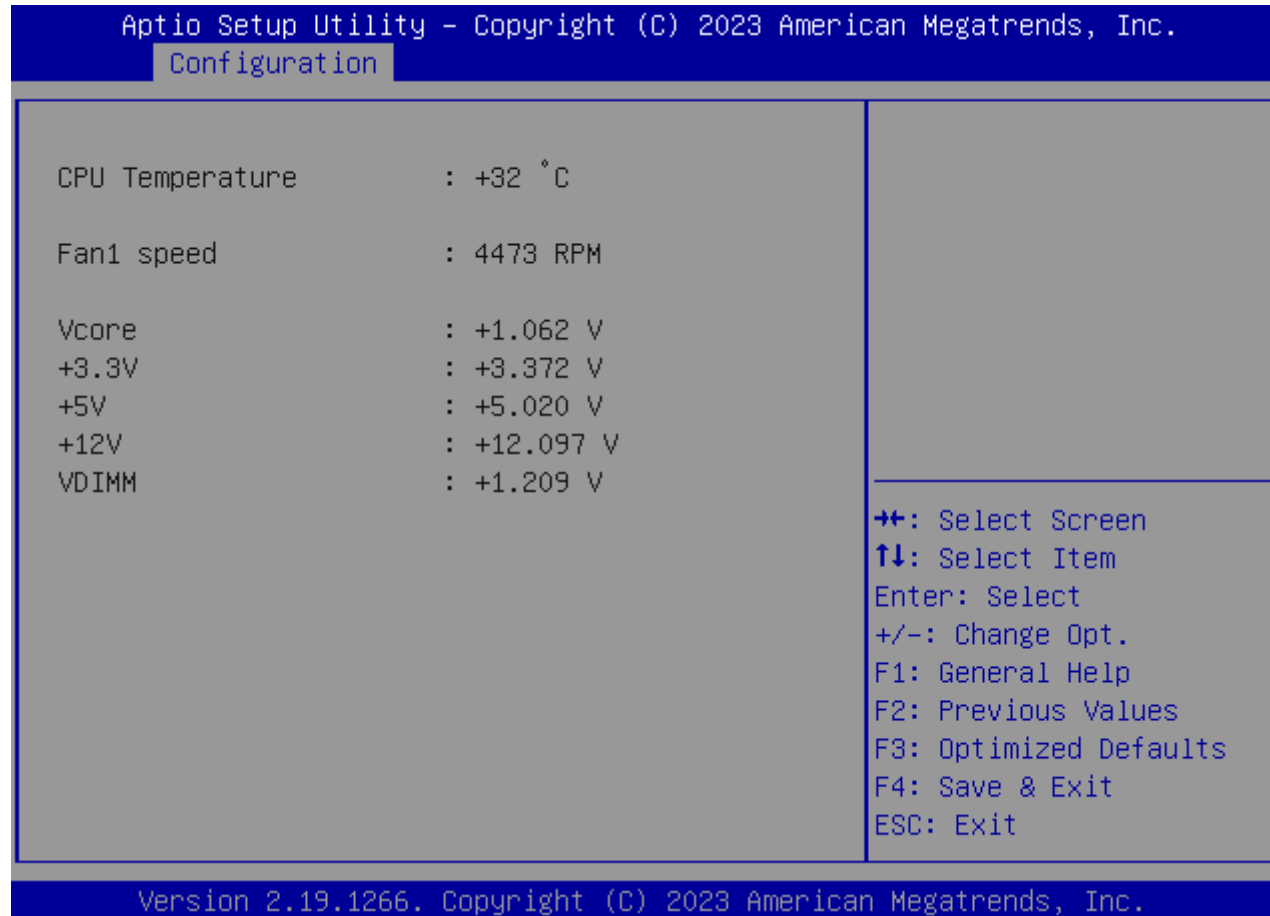
Feature	Description	Options
Security Device Support	Enables or Disables BIOS support for security device. O.S. will not show Security Device. TCG EFI protocol and INT1A Interface will not be available.	★Enabled, Disabled
SHA-1 PCR Bank	Enable or Disable SHA-1 PCR Bank	★Enabled, Disabled
SHA256 PCR Bank	Enable or Disable SHA256 PCR Bank	★Enabled, Disabled
Pending operation	Schedule an Operation for the Security Device. NOTE: Your Computer will reboot during restart in order to change State of Security Device.	★None, TPM Clear
Platform Hierarchy	Enable or Disable Platform Hierarchy	★Enabled, Disabled
Storage Hierarchy	Enable or Disable Storage Hierarchy	★Enabled, Disabled
Endorsement Hierarchy	Enable or Disable Endorsement Hierarchy	★Enabled, Disabled
TPM2.0 UEFI Spec Version	Select the TCG2 Spec Version Support, TCG_1_2: the Compatible mode for Win8 / Win10, TCG_2: Support new TCG2 protocol and event	★TCG_2, TCG_1_2
Physical Presence Spec Version	Select to Tell O.S. to support PPI Spec Version 1.2 or 1.3. Note some HCK tests might not support 1.3.	★1.3 1.2
Device Select	TPM 1.2 will restrict support to TPM 1.2 devices, TPM 2.0 will restrict support to TPM 2.0 devices, Auto will support both with the default set to TPM 2.0 devices if not found.	★Auto, TPM 2.0, TPM 1.2

Super IO Configuration

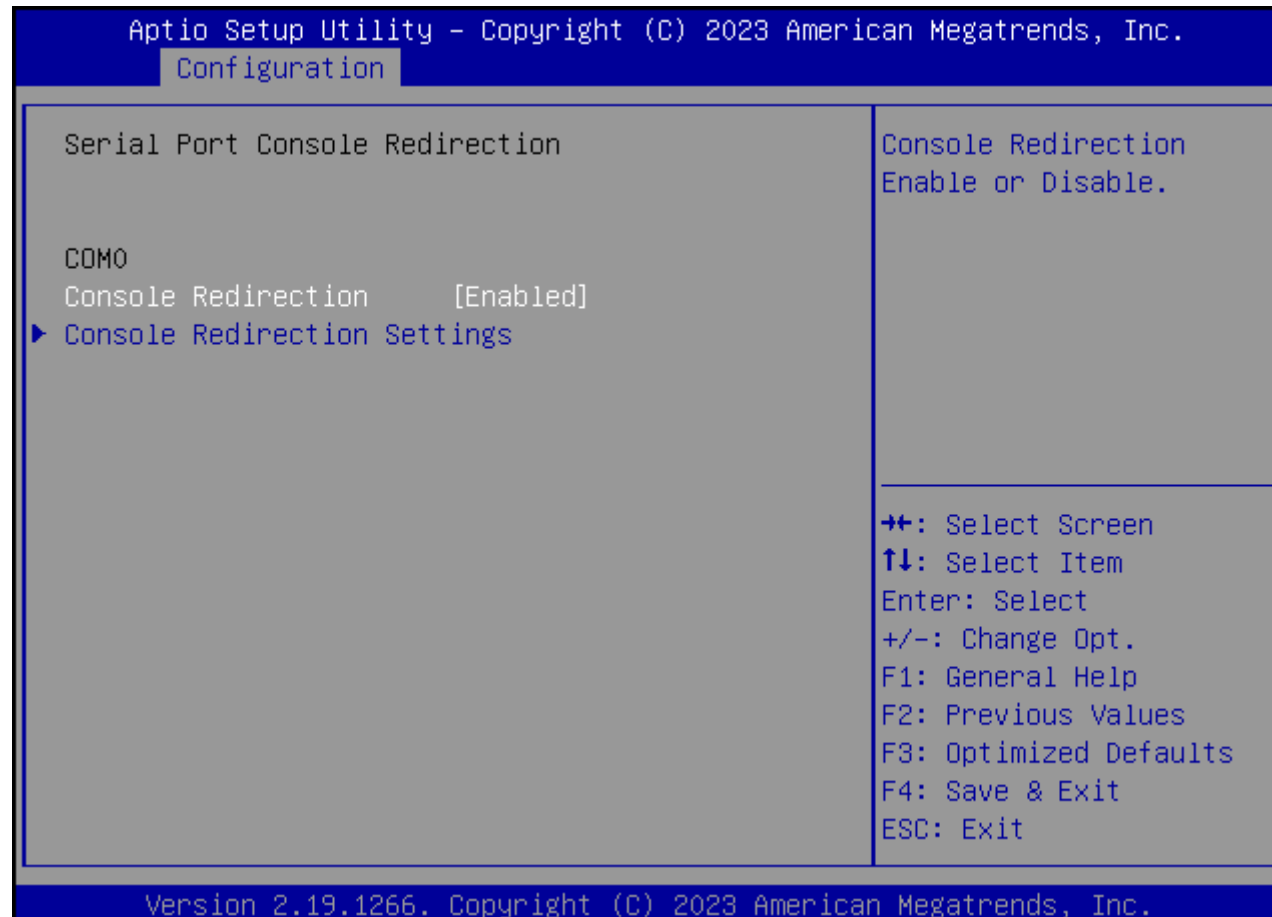


Feature	Description	Options
Module Serial Port 1~2	Enable or Disable Serial Port (COM)	★Enabled, Disabled
Watch Dog Timer	Enable/Disable Watch Dog Timer	★Disabled, Enabled
Watch Dog Timer [Enable]		
Timer Unit	Select Timer count unit of WDT	★Second, Minute
Timer value	Set WDT Timer value seconds / minutes	★20

HW Monitor

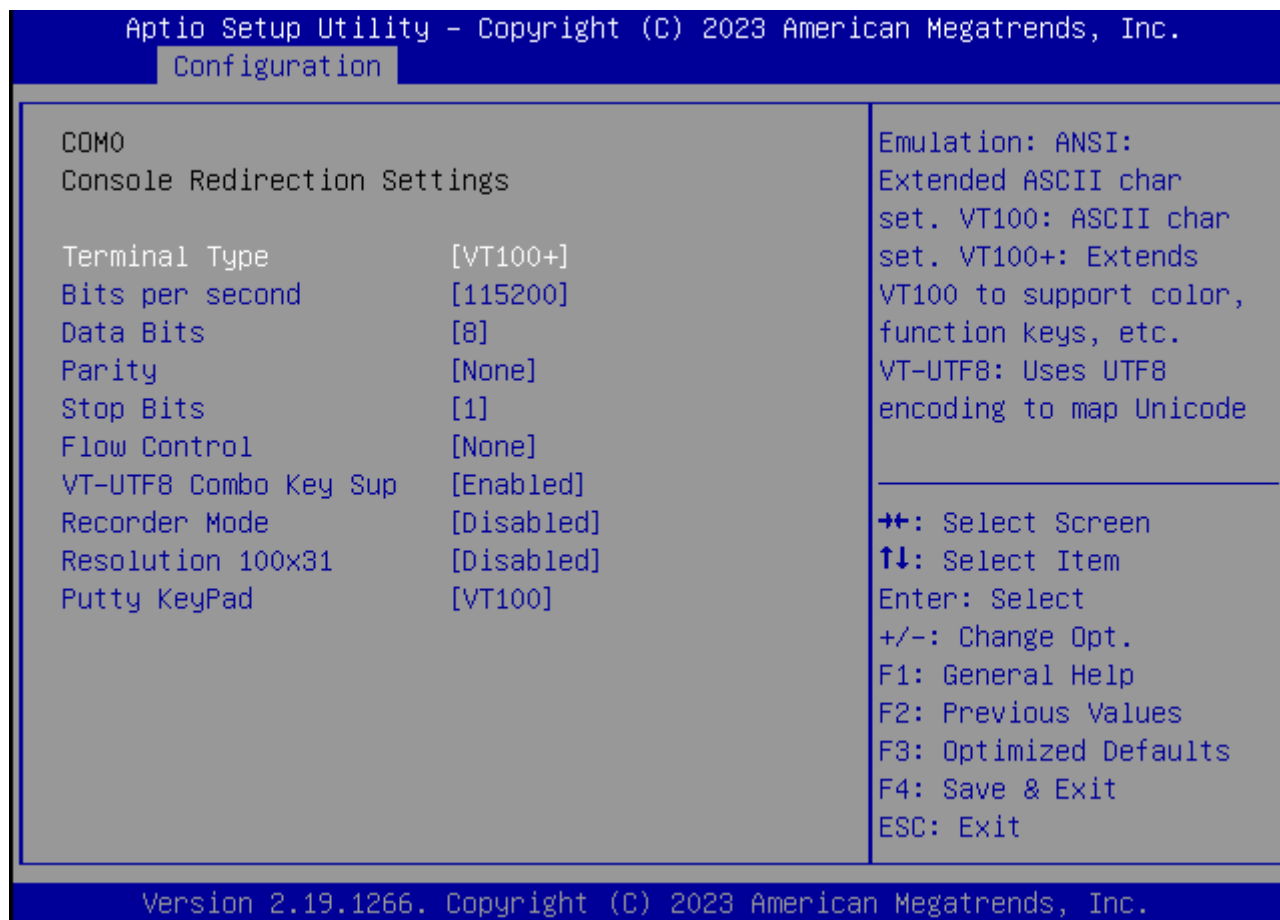


Serial Port



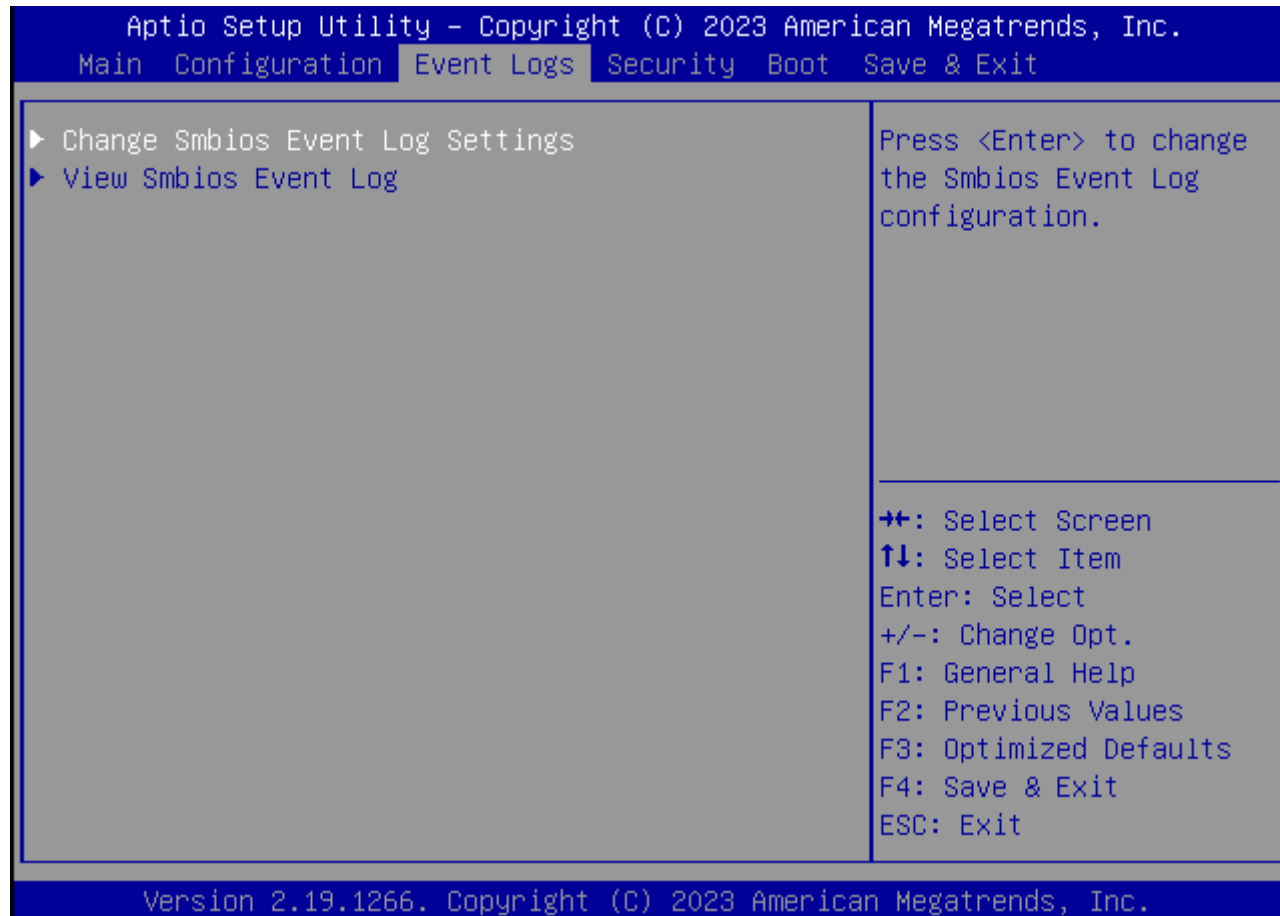
Feature	Description	Options
Console Redirection	Console Redirection Enable or Disable	★Enabled, Disabled

Console Redirection Settings



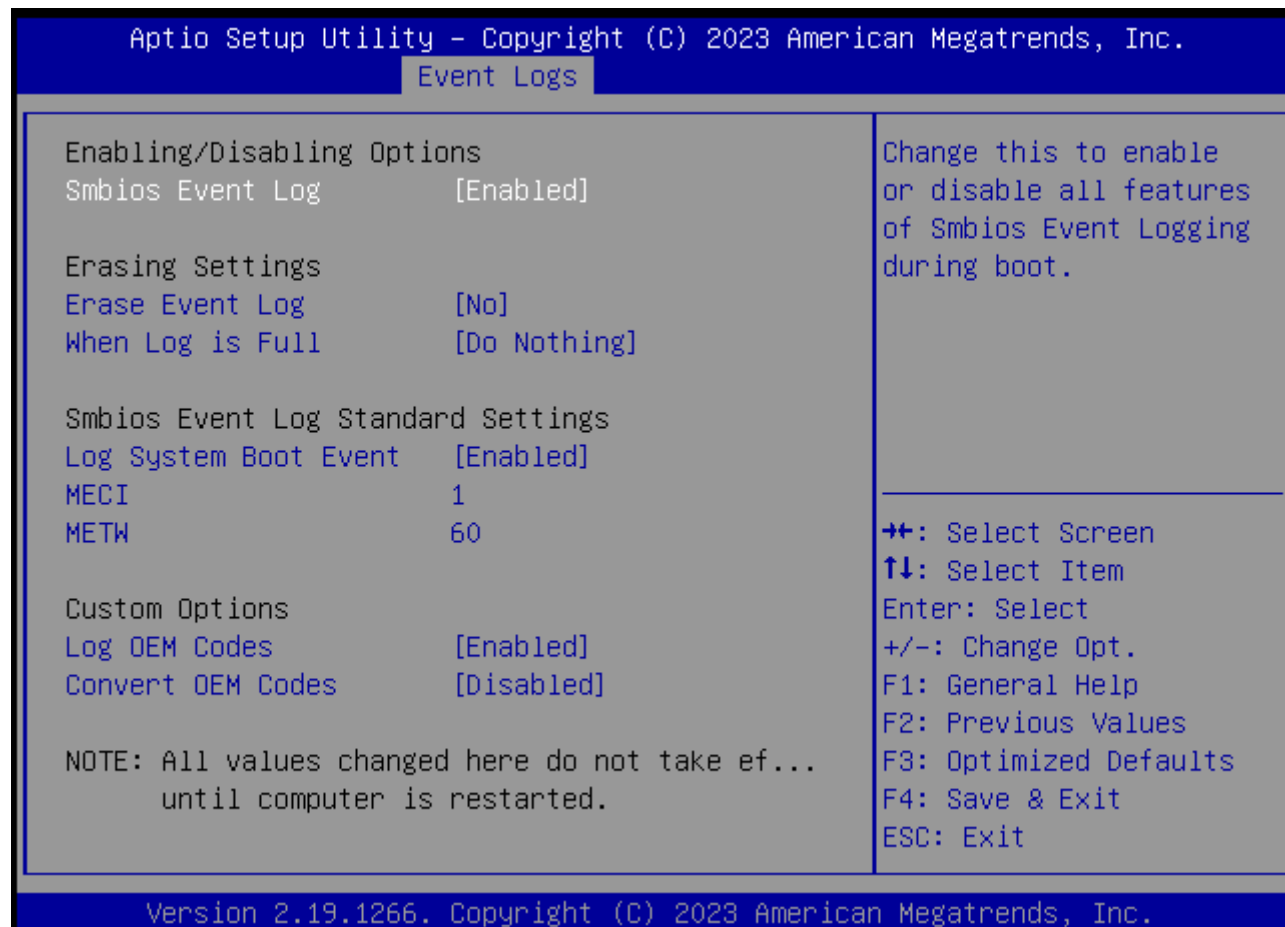
Feature	Description	Options
Terminal Type	Emulation: ANSI: Extended ASCII char set. VT100: ASCII char set. VT100+: Extends VT100 to support color, function keys, etc. VT-UTF8: Uses UTF8 encoding to map Unicode chars onto 1 or more bytes.	★VT100+, VT100, ANSI, VT-UTF8
Bits per second	Select Serial port transmission speed. The speed must be matched on other side. Long or noisy lines may require lower speeds.	★115200, 9600, 19200, 38400, 57600
Data bits	Data bits	★8, 7
Parity	A parity bit can be sent with the data bits to detect some transmission errors. Even: parity bit is 0 if the num of 1's in the data bits is even. Odd: parity bit is 0 if num of 1's in the data bits is odd. Mark: parity bit is always 1. Space parity bit is always 0. Mark and Space Parity do not allow for error detection. They can be used as an additional data bit.	★None, Even, Odd, Mark, Space
Stop Bits	Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may require more than 1 stop bit.	★1, 2
Flow Control	Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signal.	★None, Hardware RTS/CTS
VT-UTF8 Combo Key Support	Enable VT-UTF8 Combination Key Support for ANSI / VT100 terminals	★Enabled, Disabled
Recorder Mode	With this mode enabled only text will be sent. This is to capture Terminal data.	★Disabled, Enabled
Resolution 100x31	Enables or disables extended terminal resolution	★Disabled, Enabled
Putty KeyPad	Select Function Key and KeyPad on Putty.	★VT100, LINUX, XTERMR6, SCO, ESCN, VT400

6.4 Event Logs



Feature	Description	Options
Change Smbios Event Log Settings	Press <Enter> to change the Smbios Event Log configuration	
View Smbios Event Log	Press <Enter> to view the Smbios Event Log records	

Change Smbios Event Log Settings



Feature	Description	Options
Smbios Event Log	Change this to enable or disable all features of Smbios Event Logging during boot.	★Enabled, Disabled
Erase Event Log	Choose options for erasing Smbios Event Log. Erasing is done prior to any logging activation during reset.	★No, Yes Next reset, Yes Every reset
When Log is Full	Choose options for reactions to a full Smbios Event Log.	★Do Nothing, Erase Immediately
Log System Boot Event	Choose option to enable / disable logging of System boot event.	★Enabled, Disabled
MECI	Multiple Event Count Increment: The number of occurrences of a duplicate event that must pass before the multiple-event counter of log entry is updated.	★1
METW	Multiple Event Time Window: The number of minutes which must pass between duplicate log entries which utilize a multiple-event counter. The value ranges from 0 to 99 minutes.	★60
Log OEM Codes	Enable or disable the logging of EFI Status Codes as OEM Codes (if not already converted to legacy)	★Enabled, Disabled
Convert OEM Codes	Enable or disable the converting of EFI Status Codes to Standard Smbios Types (Not all may be translated).	Enabled, ★Disabled

View Smbios Event Log

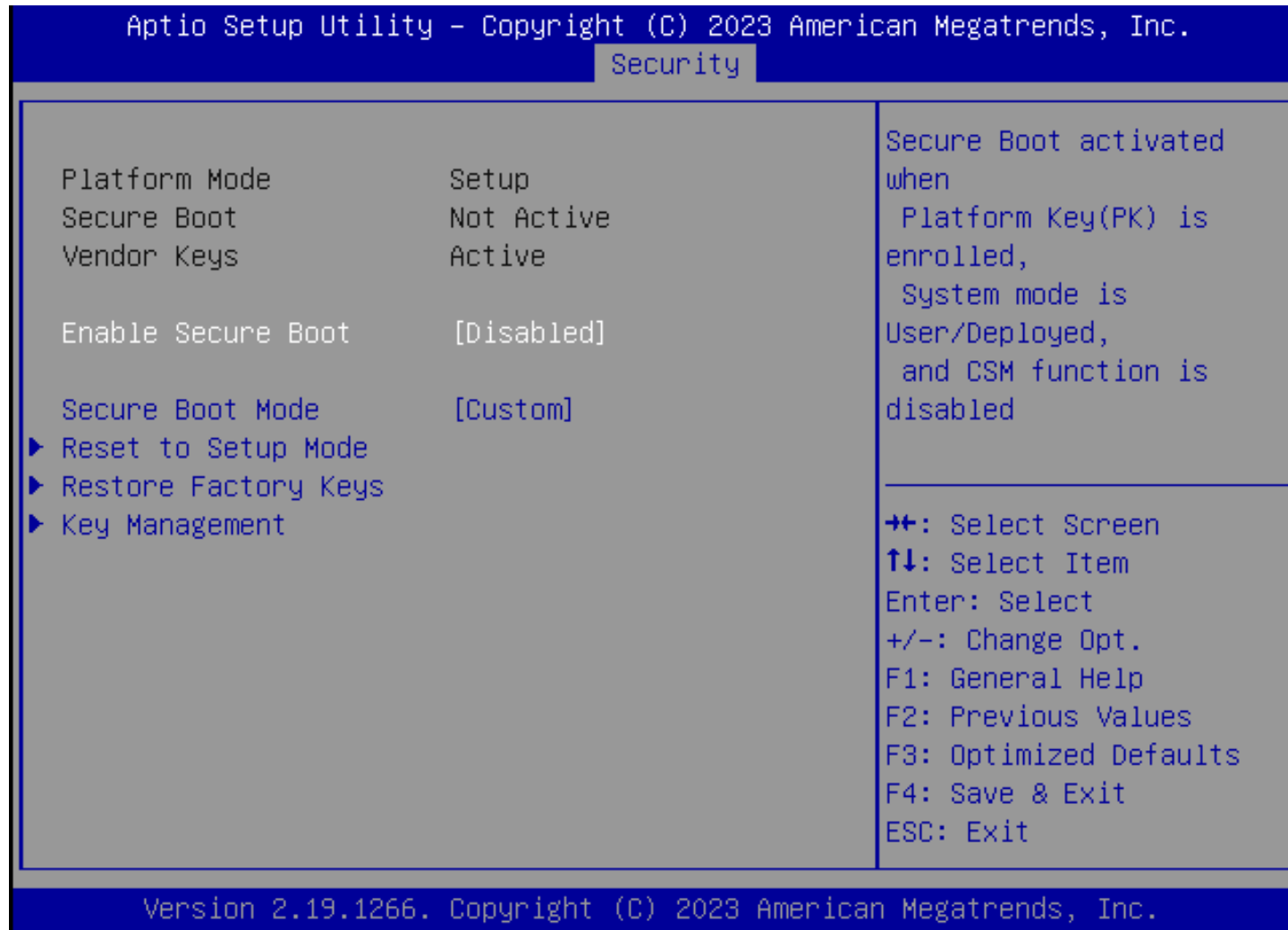
Aptio Setup Utility - Copyright (C) 2023 American Megatrends, Inc.				
Event Logs				
DATE	TIME	ERROR CODE	SEVERITY	DESCRIPTION
01/01/08	20:30:23	Smbios 0x16	N/A	Log Area Reset
01/01/08	20:30:23	Smbios 0x17	N/A	
01/01/08	20:30:25	Smbios 0x0A	N/A	
				↔: Select Screen ↑↓: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit
Version 2.19.1266. Copyright (C) 2023 American Megatrends, Inc.				

6.5 Security



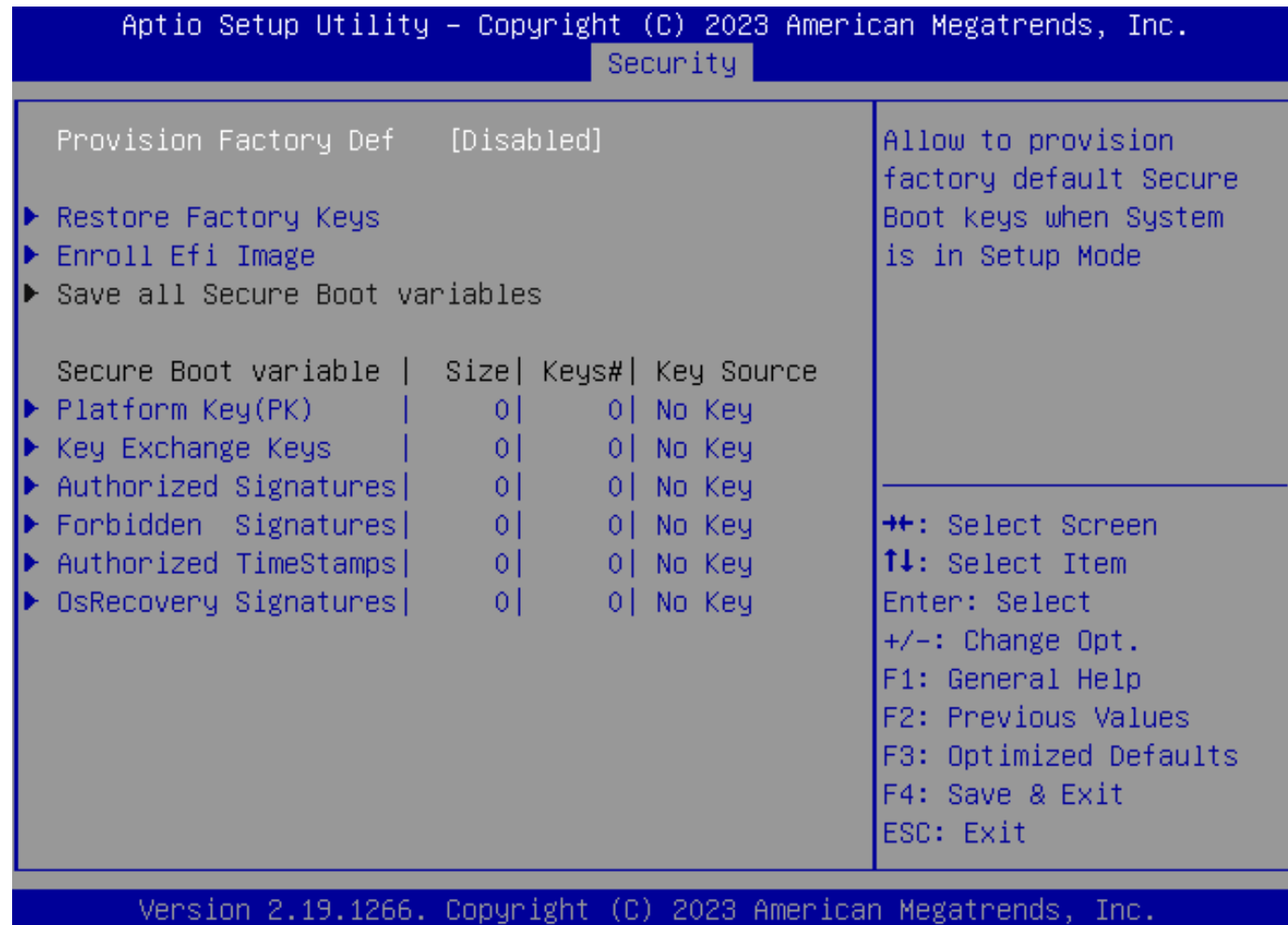
Feature	Description	Options
Password Check Mode	[Setup] check password when enter setup screen. [Power on] check password on every time system power on.	★Setup, Power On
Administrator Password	Set Administrator Password	

Secure Boot



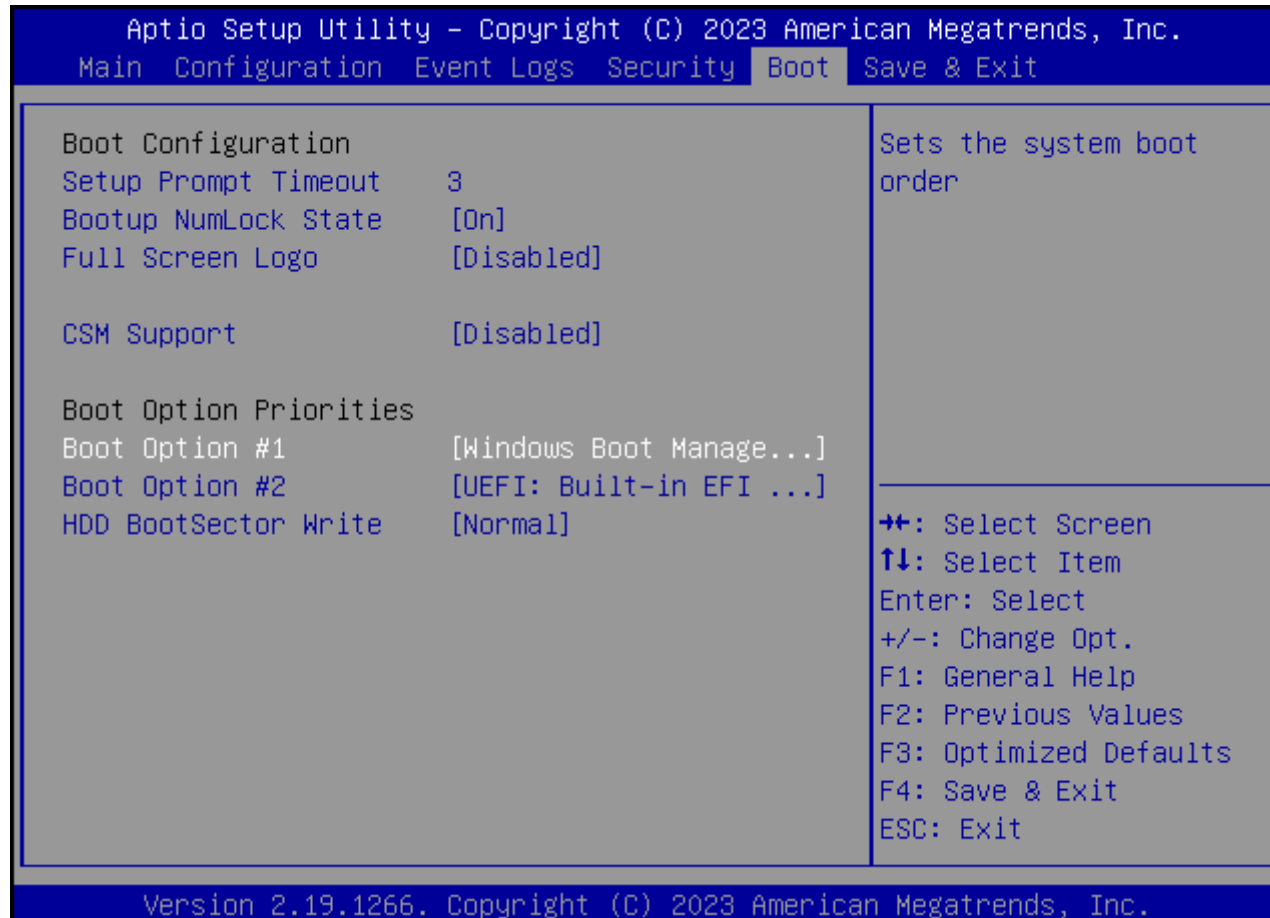
Feature	Description	Options
Enable Secure Boot	Secure Boot activated when Platform Key(PK) is enrolled, System mode is User / Deployed, and CSM function is disabled	Enabled, ★Disabled
Secure Boot Mode	Secure Boot mode selector: Standard / Custom. In Custom mode Secure Boot variables can be configured without authentication.	★Custom, Standard
Reset to Setup Mode	Force system to setup mode – delete all Secure Boot Key databases	
Install factory defaults	Force system to user mode – restore factory default Secure Boot Key databases.	
Key Management	Enables expert users to modify Secure Boot Policy variables without full authentication	

Key Management

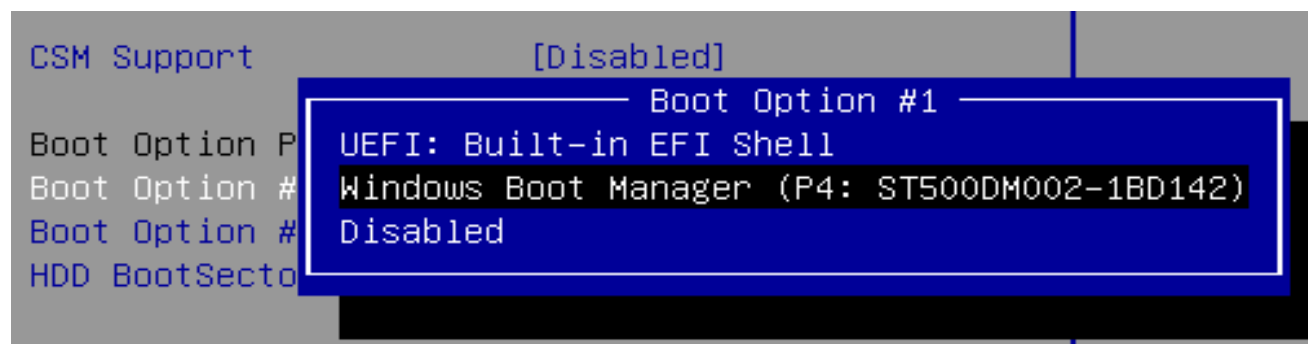


Feature	Description	Options
Provision Factory Def	Allow to provision factory default Secure Boot Keys when System is in Setup Mode.	★Disabled ,Enabled
Reset to Setup Mode	Force system to setup mode – delete all Secure Boot Key databases	
Enroll Efi Image	Allow the image to run in Secure Boot mode. Enroll SHA256 hash of the binary into Authorized Signature Database (db)	
Save all Secure Boot variables	Save NVRAM content of Secure Boot policy variables to the files (EFI_SIGNATURE_LIST data format) in root folder on a target file system device.	
Platform Key(PK)	Enroll Factory Defaults or load certificates from a file: 1. Public Key Certificate in: a)EFI_SIGNATURE_LIST b)EFI_CERT_X509 (DER encoded)	Set New
Key Exchange Keys	Enroll Factory Defaults or load certificates from a file: 1. Public Key Certificate in: a)EFI_SIGNATURE_LIST b)EFI_CERT_X509 (DER encoded)	Set New, Append
Authorized Signatures	Enroll Factory Defaults or load certificates from a file: 1. Public Key Certificate in: a)EFI_SIGNATURE_LIST b)EFI_CERT_X509 (DER encoded)	Set New, Append
Forbidden Signatures	Enroll Factory Defaults or load certificates from a file: 1. Public Key Certificate in: a)EFI_SIGNATURE_LIST b)EFI_CERT_X509 (DER encoded)	Set New, Append,
Authorized TimeStamps	Enroll Factory Defaults or load certificates from a file: 1. Public Key Certificate in: a)EFI_SIGNATURE_LIST b)EFI_CERT_X509 (DER encoded)	Set New, Append
OsRecovery Signatures	Enroll Factory Defaults or load certificates from a file: 1. Public Key Certificate in: a)EFI_SIGNATURE_LIST b)EFI_CERT_X509 (DER encoded)	Set New, Append

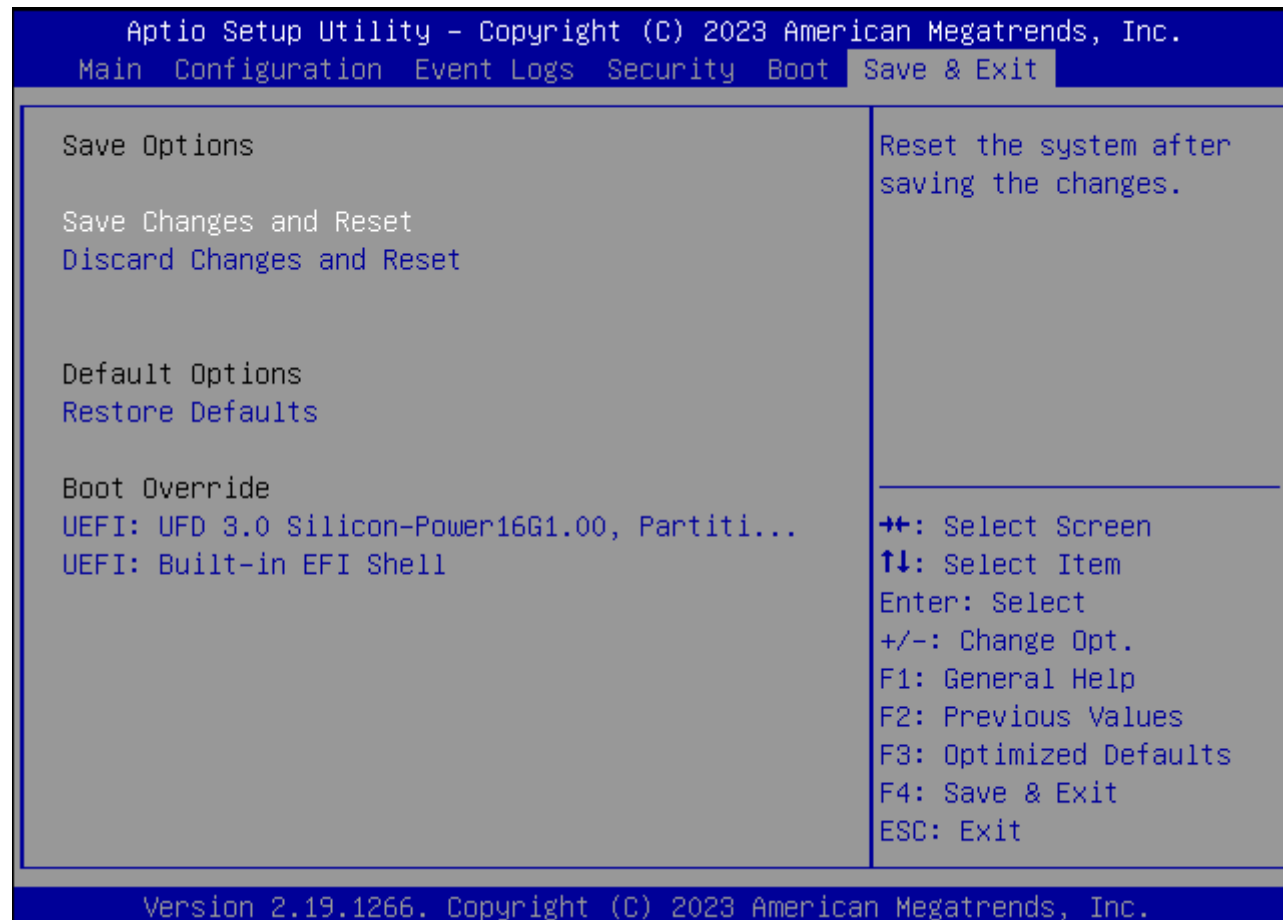
6.6 Boot



Feature	Description	Options
Setup Prompt Timeout	Number of seconds to wait for setup activation key. 65535(0xFFFF) means indefinite waiting.	★3
Bootup NumLock State	Select the keyboard NumLock state	★On, Off
Full Screen Logo	Enables or disables Quiet Boot option and Full screen Logo.	★Disabled, Enabled
CSM Support	Enable/Disable CSM support	★Disabled, Enabled
CSM Support [Enabled]		
Network	Controls the execution of UEFI and Legacy PXE OpROM	★UEFI, Do not launch, Legacy
Storage	Controls the execution of UEFI and Legacy Storage OpROM	★UEFI, Do not launch, Legacy
Launch Video OPROM	Controls the execution of UEFI and Legacy Video OpROM	★Legacy, Do not launch, UEFI
Other PCI devices	Determines OpROM execution policy for devices other than Network, Storage, or Video.	★UEFI, Do not launch, Legacy
Boot Option #1 ~ #2	Sets the system boot order.	Windows Boot Manager (SATA HDD) UEFI: Built-in EFI Shell Disabled
HDD BootSector Write	Enables or disables writes to Hard Disk Sector 0.	★Normal, Write Protect



6.5 Save & Exit



Feature	Description	Options
Save Changes and Reset	Reset the system after saving the changes.	
Discard Changes and Reset	Reset system setup without saving any changes.	
Restore Defaults	Restore/Load Default values for all the setup options.	
UEFI: Built-in EFI Shell	Reset the system after saving the changes. (Boot option filter: UEFI only)	

7 System Resources

Device	I/O Address	Note	
ITE series Embedded Controller	0x6E / 0x6F	EC Address	
	0x62 / 0x66	EC ACPI CMD Port	
	0x200 / 0x201	EC BRAM Port for I2C function	
	0xE300~0xE3FF	EC LPC IO Space	
	0x3F8~0x3FF	EC UART1	
	0x3E8~0x3EF	EC UART2	

Interface	8bit	7bit	Note
SMBus	0x30	0x18	DDR Temperature: Channel A DIMM0, J2 Slot
	0x34	0x1A	DDR Temperature: Channel B DIMM1, J3 Slot
	0x60	0x30	DDR EE Memory (SPD)
	0x62	0x31	DDR Set Write Protection, Block 0
	0x68	0x34	DDR Set Write Protection, Block 1
	0x6C	0x36	DDR4 Set SPD Page 0
	0x88	0x44	SMBus ARP
	0x96	0x4B	PECI Proxy Block Read
	0x98	0x4C	PECI Proxy Block Write
	0xA0	0x50	Memory SPD: Channel A DIMM0, J2 Slot
	0xA4	0x52	Memory SPD: Channel B DIMM1, J3 Slot

Table 11 System Resource

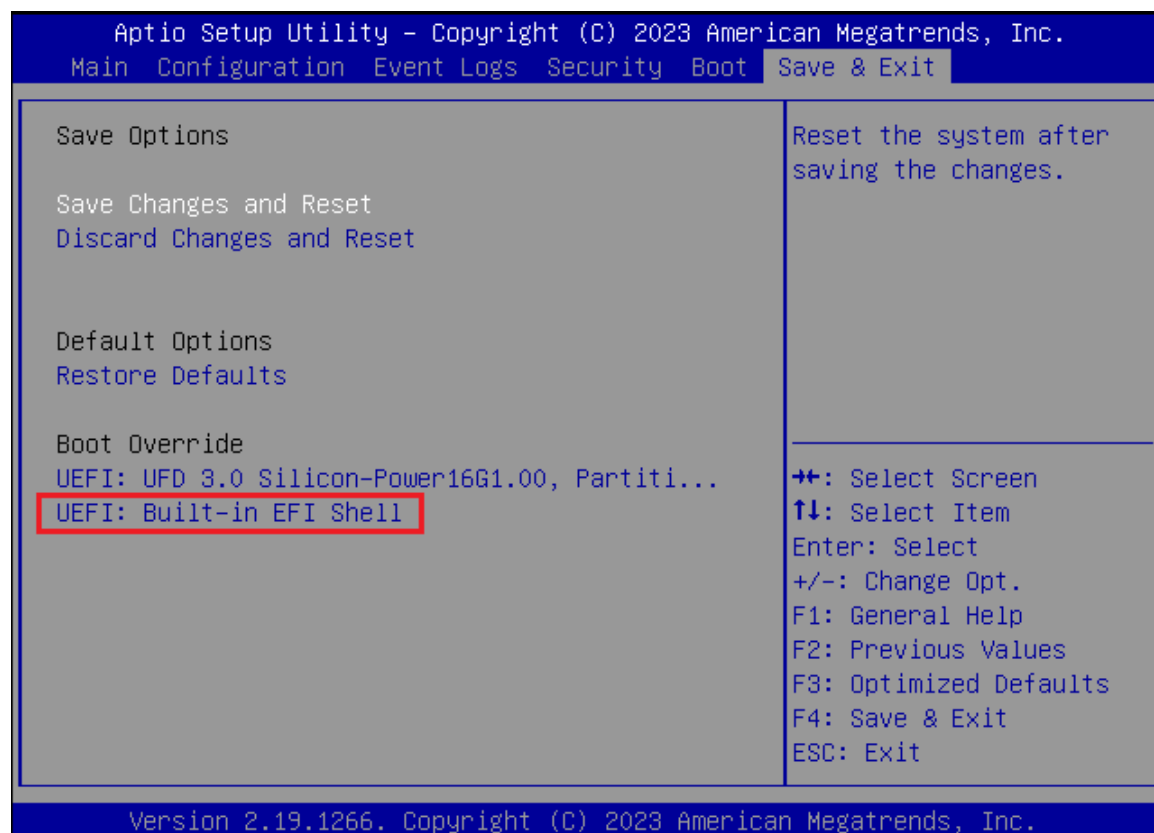
8 BIOS Update

BIOS/EC UEFI Update SOP process

Step 1. Prepare a USB Flash OK.

Step 2. Unzip update file to the USB Flash.

Step 3. Plug the USB Flash into the target system and boot from UEFI Shell.



Step 4. Under the UEFI shell, direct to your USB Flash, below is an example uses fs0; then direct to the folder with updated file and type command: "update" and press enter.

```
UEFI Interactive Shell v2.1
EDK II
UEFI v2.60 (American Megatrends, 0x0005000D)
Mapping table
  FS0: Alias(s):HD0d0b:;BLK1:
        PciRoot(0x0)/Pci(0x15,0x0)/USB(0x3,0x0)/HD(1,MBR,0x00057E24,0x800,0x1C
E7800)
  BLK0: Alias(s):
        PciRoot(0x0)/Pci(0x15,0x0)/USB(0x3,0x0)
  BLK2: Alias(s):
        PciRoot(0x0)/Pci(0x1C,0x0)/SD(0x0)
  BLK3: Alias(s):
        PciRoot(0x0)/Pci(0x1C,0x0)/SD(0x0)/HD(1,GPT,88895C1F-E2BF-44EA-8251-9B
7064C7FB79,0x22,0x7FDE)
  BLK4: Alias(s):
        PciRoot(0x0)/Pci(0x1C,0x0)/SD(0x0)/HD(2,GPT,A77E3B4B-5257-47E2-B4AA-CF
3CB5693AC3,0x8000,0x1D51000)
Press ESC in 4 seconds to skip startup.nsh or any other key to continue.
Shell> fs0:
FS0:\> _
```

```
FS0: Alias(s):HD0d0b:;BLK1:
      PciRoot(0x0)/Pci(0x15,0x0)/USB(0x3,0x0)/HD(1,MBR,0x00057E24,0x800,0x1C
E7800)
BLK0: Alias(s):
      PciRoot(0x0)/Pci(0x15,0x0)/USB(0x3,0x0)
BLK2: Alias(s):
      PciRoot(0x0)/Pci(0x1C,0x0)/SD(0x0)
BLK3: Alias(s):
      PciRoot(0x0)/Pci(0x1C,0x0)/SD(0x0)/HD(1,GPT,88895C1F-E2BF-44EA-8251-9B
7064C7FB79,0x22,0x7FDE)
BLK4: Alias(s):
      PciRoot(0x0)/Pci(0x1C,0x0)/SD(0x0)/HD(2,GPT,A77E3B4B-5257-47E2-B4AA-CF
3C85693AC3,0x8000,0x1D51000)
Press ESC in 4 seconds to skip startup.nsh or any other key to continue.
Shell> fs0:
FS0:\> cd Update_B702GT-C3558R_0_0_9
FS0:\Update_B702GT-C3558R_0_0_9> ls
Directory of: FS0:\Update_B702GT-C3558R_0_0_9\
12/08/2023  13:40 <DIR>                8,192
12/08/2023  13:40 <DIR>                0
12/08/2023  11:08                  383  ReadMe.txt
12/08/2023  11:08          5,857,553  Update.efi
          2 File(s)    5,857,936 bytes
          2 Dir(s)
FS0:\Update_B702GT-C3558R_0_0_9> Update_
```

Step 5. The updating process will start and you can see the updating progress. Once finished, please power off the system.

```
- ME Data Size checking . ok
- FFS checksums ..... ok
- Check RomLayout ..... Ok.
Erasing Boot Block ..... done
Updating Boot Block ..... done
Verifying Boot Block ..... done
Erasing Main Block ..... done
Updating Main Block ..... done
Verifying Main Block ..... done
Erasing NVRAM Block ..... done
Updating NVRAM Block ..... done
Verifying NVRAM Block ..... done
Erasing NCB Block ..... done
Updating NCB Block ..... done
Verifying NCB Block ..... done
- Update success for FDR
- Update success for GBEA... \
- Update success for GBEB.. |
- Successful Update Recovery Loader to OPRx!!
- Successful Update MFSB!!!
- Successful Update FTPR!!!
- Successful Update factory data partitions!!
- ME Entire Image update success !!
WARNING : System must power-off to have the changes take effect!
FS0:\Update_B702GT-C3558R_0_0_9\> _
```

EC UEFI update

Step 1. Prepare a USB Flash OK.; Unzip update file to the USB Flash; Plug the USB Flash into the target system and boot from UEFI Shell; Under the UEFI shell, direct to your USB Flash, below is an example uses fs0; then direct to the folder with updated file and type command: "update" and press enter.

```
FS0: Alias(s):HD0d0b:;BLK1:
      PciRoot(0x0)/Pci(0x15,0x0)/USB(0x3,0x0)/HD(1,MBR,0x00057E24,0x800,0x1C
E7800)
BLK0: Alias(s):
      PciRoot(0x0)/Pci(0x15,0x0)/USB(0x3,0x0)
BLK2: Alias(s):
      PciRoot(0x0)/Pci(0x1C,0x0)/SD(0x0)
BLK3: Alias(s):
      PciRoot(0x0)/Pci(0x1C,0x0)/SD(0x0)/HD(1,GPT,88895C1F-E2BF-44EA-8251-9B
7064C7FB79,0x22,0x7FDE)
BLK4: Alias(s):
      PciRoot(0x0)/Pci(0x1C,0x0)/SD(0x0)/HD(2,GPT,A77E3B4B-5257-47E2-B4AA-CF
3C85693AC3,0x8000,0x1D51000)
Press ESC in 5 seconds to skip startup.nsh or any other key to continue.
Shell> fs0:
FS0:\> cd Update_EC-B702G_AT_0_10
FS0:\Update_EC-B702G_AT_0_10> ls
Directory of: FS0:\Update_EC-B702G_AT_0_10\
12/08/2023  17:22 <DIR>          8,192  .
12/08/2023  17:22 <DIR>           0     ..
10/04/2023  17:50          384   ReadMe.txt
10/04/2023  17:50       71,632   Update.efi
          2 File(s)       72,016 bytes
          2 Dir(s)
FS0:\Update_EC-B702G_AT_0_10> Update_
```

Step 2. The updating process will start and you can see the updating progress. Once finished, please power off the system.

```
PciRoot(0x0)/Pci(0x1C,0x0)/SD(0x0)
BLK3: Alias(s):
PciRoot(0x0)/Pci(0x1C,0x0)/SD(0x0)/HD(1,GPT,88895C1F-E2BF-44EA-8251-9B
7064C7FB79,0x22,0x7FDE)
BLK4: Alias(s):
PciRoot(0x0)/Pci(0x1C,0x0)/SD(0x0)/HD(2,GPT,A77E3B4B-5257-47E2-B4AA-CF
3C85693AC3,0x8000,0x1D51000)
Current shell version is v2.x
ITE EC Flash Utility for UEFI Shell, Version : 1.4.0 (64)
<Re-Write by FoxYang .. 2021/12/22 >

[/NOKBC] support
!!Please don't use KB/MS during updating ...!!
Device ID       : C2 20 14 C2
SPI Vendor      : MXIC
Eraseing...     : ██████████ -- Erase OK.

Erase Verify... : ██████████ -- Erase Verify OK.

Programing...   : ██████████ -- Programing OK.

Verify...       : ██████████ -- Verify OK.

Please turn off power(G3) by manual , let EC reload new image !!
FS0:\Update_EC-B702G_AT_0_10\>
```

<End of BIOS/EC UEFI updates process>

9 PORTWELL Software Tool

PORTWELL Download Center

<https://www.portwell.com.tw/support-center/download-center/>

PORTWELL Evaluation Tool (PET)

The PORTWELL Evaluation Tool (PET) is an API which PORTWELL's customers can access the GPIO, I2C, SMBus, etc under Windows and Linux OS. For more information please contact PORTWELL.

10 Industry Specifications

The list below provides links to industry specifications that apply to PORTWELL modules.

Low Pin Count Interface Specification, Revision 1.0 (LPC) <http://www.intel.com/design/chipsets/industry/lpc.htm>

Universal Serial Bus (USB) Specification, Revision 2.0 <http://www.usb.org/home>

PCI Specification, Revision 2.3 <https://www.pcisig.com/specifications>

Serial ATA Specification, Revision 3.0 <http://www.serialata.org/>

PICMG® COM Express Module™ Base Specification <http://www.picmg.org/>

PCI Express Base Specification, Revision 2.0 <https://www.pcisig.com/specifications>