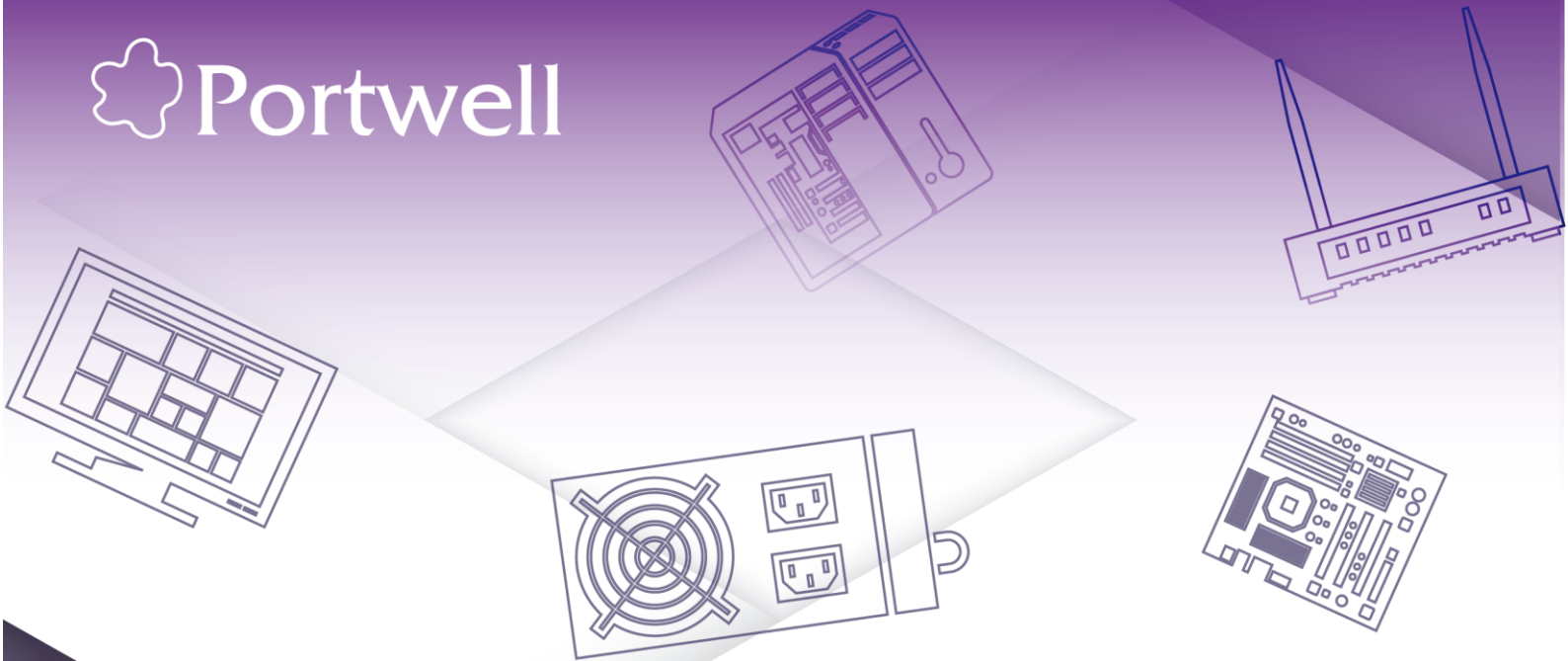




NANO-6064 Series

NANO-ITX Embedded Board

User Manual

Version R1.5

Copyright

The documentation and the software included with this product are copyrighted 2024 by Portwell. All rights are reserved. Portwell reserves the right to make improvements to the products described in this manual at any time without notice. No part of this manual may be reproduced, copied, translated, or transmitted in any form or by any means without the prior written permission of Portwell. The information provided in this manual is intended to be accurate and reliable. However, Portwell assumes no responsibility for its use, nor for any infringements of the rights of third parties that may result from its use.

Revision History

R1.0	Official release Rev. 1.0
R1.1	Update information to support Amston Lake
R1.2	Fix typos and add a note
R1.3	Change template
R1.4	Adding extension bracket for M.2 3052 module
R1.5	Correct the description of the Test Configuration

Table of Contents

1. Introduction.....	6
2. Specifications.....	8
2.1 Supported Operating Systems	9
2.2 Mechanical Dimensions	10
2.3 Power Consumption.....	10
2.4 Environmental Specifications	12
3 Block Diagram	14
4 Hardware Configuration	16
4.1 Jumpers and Connectors.....	16
4.2 Jumper Settings	17
5 Sample Code	25
5.1 Watch Dog Timer.....	25
5.2 Signal GPIO Signal	27
6 BIOS Setup Items	31
6.1 Entering Setup -- Launch System Setup	32
6.2 Main.....	33
6.3 Configuration.....	35
6.3.1 CPU Configuration	36
6.3.2 Chipset Configuration	38
6.3.3 Graphics Configuration	39
6.3.4 Power Control Configuration	42
6.3.5 PCI/PCIE Configuration	43
6.3.6 LAN Configuration.....	45
6.3.7 SATA Configuration.....	46
6.3.8 USB Configuration.....	47
6.3.9 TPM Configuration: TPM 2.0 Device Found	48
6.3.10 Super IO Configuration	49
6.3.11 HW Monitor	50
6.3.12 Serial Port Console Redirection	51
6.3.13 EC Firmware Update	53
6.3.14 Update EC	54
6.3.15 Security.....	55
6.3.16 Boot	58
6.3.17 Save & Exit.....	59
7 System Resources	64
7.1 Intel® Alder Lake N/ Amston Lake SoC	64
7.2 Main Memory.....	64
7.3 Installing the Single Board Computer	64

7.3.1	Chipset Component Driver	65
7.3.2	Chipset Component Driver	65
8	Troubleshooting.....	67
8.1	Hardware Quick Installation	67
8.2	BIOS Setting	69
8.3	FAQ.....	70
9	Portwell Software Service	73

Chapter 1

Overview

1 Introduction

1. Introduction

The NANO-6064 series utilizes the NANO-ITX form factor and is powered by the Intel Atom® processor x7000E series or Intel® Core™ i3 N-Series and Intel Atom® processor x7000RE series. It supports one DDR4 SO-DIMM socket with up to 16GB capacity, one M.2 E key socket, and one M.2 B key socket. The integrated Intel Gen 12 UHD Graphics with up to 32 EUs support triple independent displays via DisplayPort, HDMI, and LVDS. Additionally, it features one 2.5GbE port, one SD socket, and four USB 3.2 ports.

The NANO-6064 series is versatile, compact, powerful, and fanless, making it ideal for diverse applications such as industrial automation, robotic control systems, automated test equipment, medical equipment, gateways, digital signage, and more.

Chapter 2

Overview

- 2 Specifications
- 2.1 Supported Operating Systems
- 2.2 Mechanical Dimension
- 2.3 Power Consumption

2. Specifications

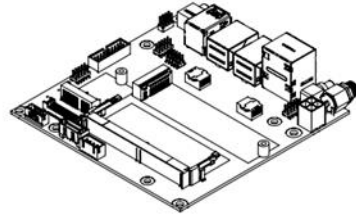
Main Processor	Intel® Atom®x7000E series Processor (up to 12W) Intel® Core™ i3 N-Series Processor (up to 15W) Intel® Atom®x7000RE series Processor (up to 12W)
System BIOS	AMI UEFI BIOS
Main Memory	1x non-ECC DDR4 3200MT/s SO-DIMM up to 16GB 1DPC, 1-channel Support In-Band ECC
Graphics	Intel® UHD Graphics Gen12 with up to 32 EUs HDMI: 1x HDMI port on rear I/O (HDMI 2.0b, 4096x2160 @ 60Hz) DP: 1x DP port on rear I/O (DP 1.4, 4096x2304 @ 60Hz) LVDS: 1x LVDS on board connector (Dual channel, 24bit, 1920x1200 @60Hz)
Expansion Interface	1x M.2 E key2230 1x M.2 B Key 3052+2280 (share with M.2 2280 SATAIII socket)
Storage Interface	1x SATA III port (SATA 6Gb/s) 1xM.2 2280 B Key (SATA III) 1xMicro SD socket
Input/Output	Serial Port: 1x RS-232/422/485 port (selectable via BIOS) 2x USB 3.2 Gen2 on rear I/O, 2x USB 3.2 Gen1 on board pin header (1x USB 3.2 Gen1 share with M.2 B key socket) Audio Interface: Audio jack on rear I/O (Line-out) and on-board pin header (Line-in, Line-out, Mic-in) 1x Nano SIM socket
Ethernet	2x Intel® 2.5GbE Controller 2x RJ45 connectors on rear I/O
High Drive GPIO	1x pin-header for GPIO(8bit)
Mechanical and environmental specifications	Board size: 120mm x 120 mm (4.72" x 4.72") Operating temperature: 0 ~ 60° C (Alder Lake N SKU)/ -40 ~ 85° C (Amston Lake SKU) Storage temperature: -40 ~ 85° C Humidity: 5 ~ 95% non-condensing Power supply voltage: 12V DC in
Certification	CE/FCC/UKCA

2.1 Supported Operating Systems

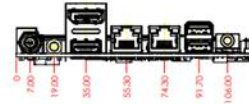
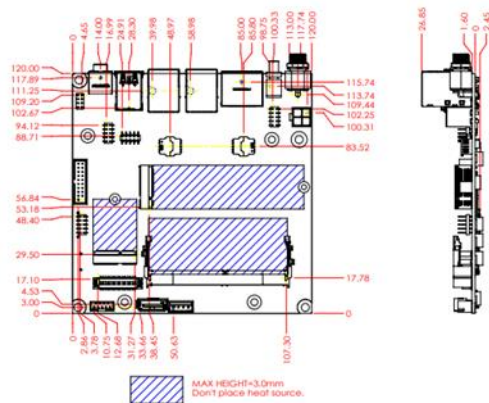
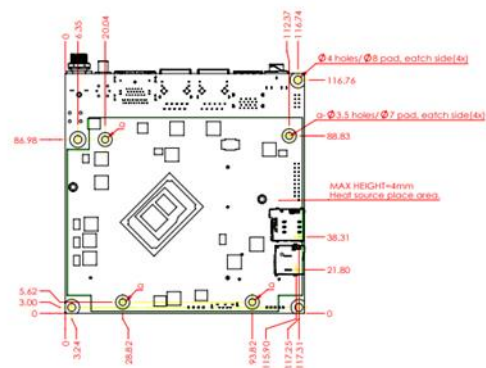
The NANO-6064 supports the following operating systems.

- Windows 10 IoT Enterprise LTSC 2021(64bit)
- Yocto YP 4.0 LTS (64 bit)
- Ubuntu 22.04
- Red Hat 8.8
- Linux Kernel version 6.1

2.2 Mechanical Dimensions



Note:
• 限高區域及淨空區域內皆禁放DIP件、發熱元件



2.3 Power Consumption

Test Configuration	
CPU Type	Intel® Atom® x7835RE 1.3GHz
	Intel® Atom® x7433RE 1.5GHz
	Intel® Atom® x7213RE 2.0GHz
	Intel® Atom® x7211RE 1.0GHz
	Intel® Atom® Core™ i3-N305 1.8GHz
	Intel® Atom® x7425E 1.5GHz
	Intel® Atom® x7213E 1.7GHz
	Intel® Atom® x7211E 1.0GHz
SBC BIOS	Portwell, Inc. NANO-6064 BIOS Rev.: 0.0.3 (04252023)
Memory	Innodisk 16GB DDR4 3200 W/T ECC SODIMM (SEC K4A8G085WC)

Graphic Card	Onboard Intel(R) UHD Graphics
Graphic Driver	Intel(R) UHD Graphics, version: 31.0.101.3417
LAN Card #1	Onboard Intel(R) Ethernet Controller (3) I226-LM/ I226-IT
LAN Driver #1	Intel(R) Ethernet Controller (3) I226-LM/ I226-IT, version: 1.1.4.42
LAN Card #2	Onboard Intel(R) Ethernet Controller (3) I226-LM/ I226-IT #2
LAN Driver #2	Intel(R) Ethernet Controller (3) I226-LM/ I226-IT #2, version: 1.1.4.42
Audio Card	Onboard Realtek High Definition Audio
Audio Driver	Realtek High Definition Audio, version: 6.0.9239.1
Chip Driver	Intel(R) Chipset Device Software, version: 3.1.7.143
USB3.1 Driver	Intel(R) USB 3.10 eXtensible Host Controller – 1.20 (Microsoft), version: 10.0.19041.1806
USB3.2 Driver	Intel(R) USB 3.20 eXtensible Host Controller – 1.20 (Microsoft), version: 10.0.19041.1806
EC Version	0.4 (10/03/2023)
Hard Drive	ST1000DM010
Power Supply	Switching Power Adpater, FSP120-AHAN1

Power consumption(12V)		
Item	Power On	Full Loading 10Min
DC in +12V	2.21A	2.60A
DC in + Device +12V	2.23A	2.70A
Device +5V	0.50A	
USB Loading Test Port J5 up	5.001V/ 1.03A	

USB Loading Test Port J5 down	5.003V/ 1.01A
USB Loading Test Port J13 left	4.938V/ 1.01A
USB Loading Test Port J13 right	4.937V/ 1.01A
Full USB port Loading Test(X4)	<u>4.934V</u> / <u>0.99A</u> (J13 left)

2.4 Environmental Specifications

Storage Temperature: -40~85° C

Operation Temperature:

0~60° C (Alder Lake N SKU)、-40~85° C (Amston Lake SKU)

Storage Humidity: 5~95%, non-condensing

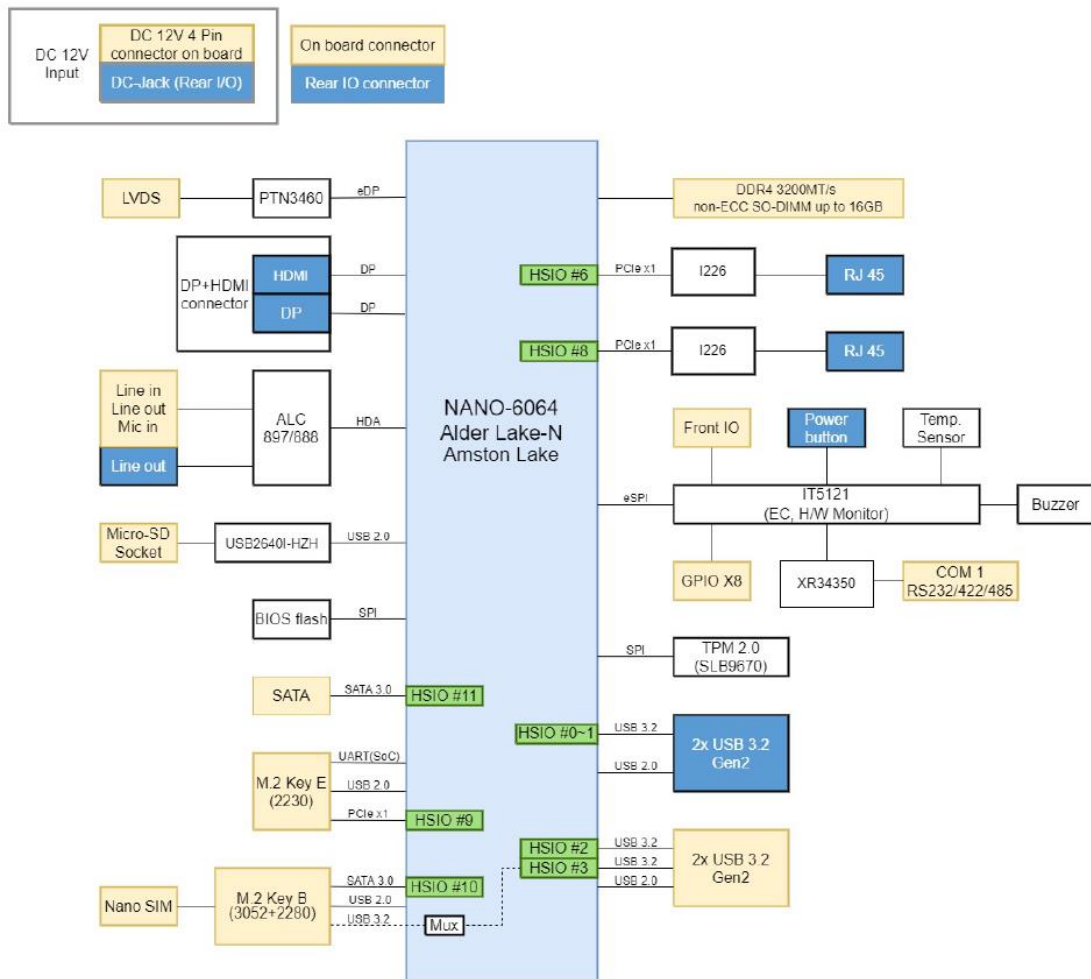
Operation Humidity: 5~95%, non-condensing

Chapter 3

Overview

3 Block Diagram

3 Block Diagram



Chapter 4

Overview

- 4 Hardware Configuration
- 4.1 Jumpers and Connectors
- 4.2 Jumper Settings

4 Hardware Configuration

4.1 Jumpers and Connectors

Figure 1, NANO-6064 Top View

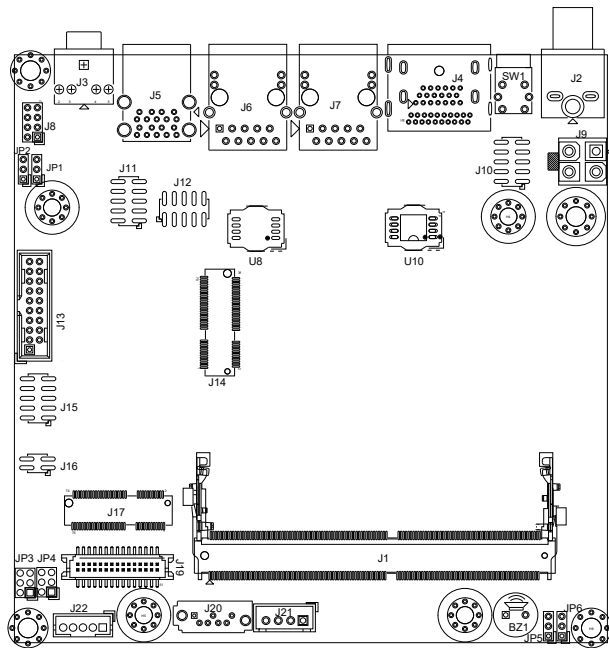
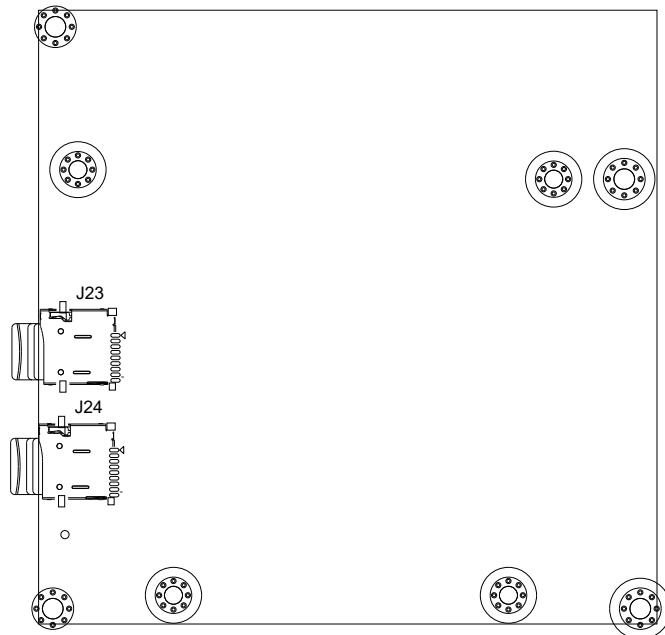


Figure 2, NANO-6064 Bottom View



4.2 Jumper Settings

For users to customize NANO-6064's features. In the following sections, Short means covering a jumper cap over jumper pins; Open or N/C (Not Connected) means removing a jumper cap from jumper pins. Users can refer to Figure 1 for the Jumper allocations.

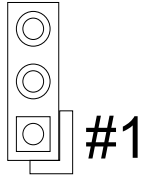
Jumper Table

The jumper settings are schematically depicted in this manual as follows:

Jump Function List:

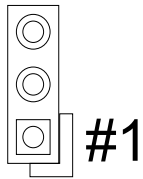
Jump	Function	Remark
J1	DDR4 SO-DIMM Socket	
J2	DC Jack	+12V Input
J3	Audio Jack (Line_out)	
J4	DP++ and HDMI Port	
J5	USB3 Connector	
J6/J7	RJ45 Connector	
J8	External Audio (Mic + Line_in + Line_out)Pin HDR.	4x2 pin header
J9	ATX 4 Pin Connector	+12V Input
J10	Front Panel Pin HDR	5x2 pin header
J11	80 Port Connector	5x2 pin header
J12	General Purpose I/O Pin HDR	5x2 pin header
J13	External USB3 Connector	
J14	M.2 key B Socket	
J15	RS232/422/485 Pin HDR	5x2 pin header
J17	M.2 key E Socket	
J19	LVDS Connector	
J20	SATA GEN3 Connector	
J21	SATA Power Connector	
J22	Backlight Connector	
J23	Nano SIM	
J24	Micro SD	

JP1 : GPIO4~7 Voltage Output Level Selection



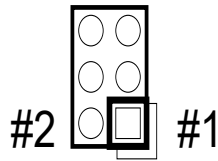
PIN No.	Signal Description
1-2 Short	5V
2-3 Short	3.3V ★

JP2 : Power On Mode Selection



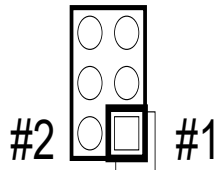
PIN No.	Signal Description
1-2 Short	AT
2-3 Short	ATX ★

JP3 : BACKLIGHT Enable Voltage Selection



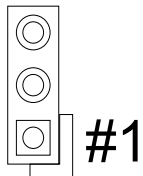
PIN No.	Signal Description
1-3, 2-4	5V, Active High ★
1-3, 4-6	12V, Active High
3-5, 2-4	5V, Active Low
3-5, 4-6	12V, Active Low

JP4 : PANEL Voltage Selection



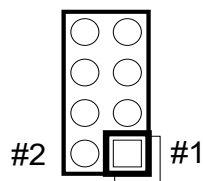
PIN No.	Signal Description
1-3 Short	3.3V
3-5 Short	5V ★
3-4 Short	12V

JP6 : CMOS Clear



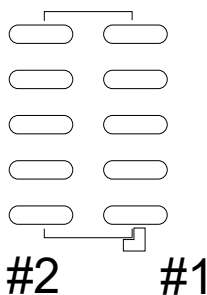
PIN No.	Signal Description
1-2 Short	Clear CMOS
2-3 Short	n/a

J8 : External Audio Connector



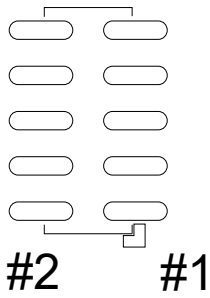
PIN No.	Signal Description	PIN No.	Signal Description
1	MIC_L	2	Line_in_L
3	Ground	4	Line_in_R
5	Line_out_L	6	Ground
7	Line_out_R	8	MIC_R

J10 : Front Panel Pin HDR



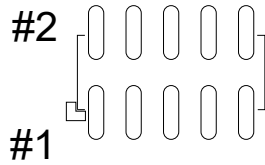
PIN No.	Signal Description	PIN No.	Signal Description
1	Ground	2	n/c
3	External Power LED(+)	4	External Power LED(-)
5	HDD_LED(+)	6	HDD_LED(-)
7	Reset (+)	8	Power On(-)
9	Reset (-)	10	Power On(+)

J11 : 80 Port Connector



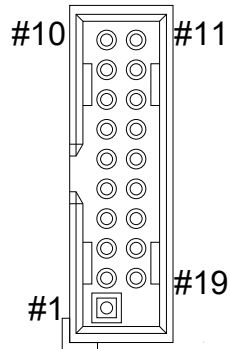
PIN No.	Signal Description	PIN No.	Signal Description
1	EC_LEDA	2	3.3V
3	EC_LEDB	4	EC_LEDE
5	EC_LEDC	6	EC_LEDF
7	EC_LEDD	8	EC_LEDG
9	EC_DGL#	10	GND

J12: General Purpose I/O Connector



PIN No.	Signal Description	PIN No.	Signal Description
1	GPIO0	2	GPIO4 (Output Only)
3	GPIO1	4	GPIO5 (Output Only)
5	GPIO2	6	GPIO6 (Output Only)
7	GPIO3	8	GPIO7 (Output Only)
9	Ground	10	+5V

J13: External USB3 Connector

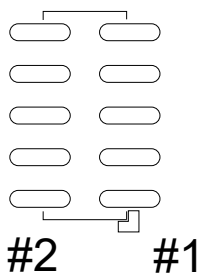


PIN No.	Signal Description	PIN No.	Signal Description
1	+5V always	11	USB2_DP_#2
2	USB3_RXM_#3	12	USB2_DM_#2
3	USB3_RXP_#3	13	Ground
4	Ground	14	USB3_TXP_#2
5	USB3_TXM_#3	15	USB3_TXM_#2
6	USB3_TXP_#3	16	Ground
7	Ground	17	USB3_RXP_#2
8	USB2_DM_#3	18	USB3_RXM_#2
9	USB2_DP_#3	19	+5V always
10	Ground		Key(no pin)

Note:

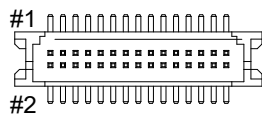
5V Dual is always available. It's supplied by either 5V VCC power source in normal operation mode or 5V standbypower source in standby mode.

J15: RS-232/422/485I/O Connector



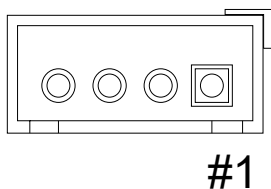
PIN No.	Signal Description	PIN No.	Signal Description
1	DCD#/485D-/422T-	2	RXD#/485D+/422T+
3	TXD#/422R+	4	DTR#/422R-
5	Ground	6	DSR#
7	RTS#	8	CTS#
9	RI#	10	N/C

J19: LVDS Connector



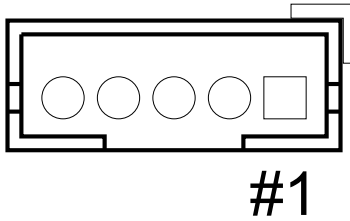
PIN No.	Signal Description	PIN No.	Signal Description
1	VDD_LVDS	2	VDD_LVDS
3	LVDSA_DATA0	4	LVDSA_DATA#0
5	LVDSA_DATA1	6	LVDSA_DATA#1
7	LVDSA_DATA2	8	LVDSA_DATA#2
9	LVDSA_DATA3	10	LVDSA_DATA#3
11	LVDSA_CLKP	12	LVDSA_CLKN
13	DDC_SCL	14	DDC_SDA
15	Ground	16	Ground
17	LVDSB_DATA0	18	LVDSB_DATA#0
19	LVDSB_DATA1	20	LVDSB_DATA#1
21	LVDSB_DATA2	22	LVDSB_DATA#2
23	LVDSB_DATA3	24	LVDSB_DATA#3
25	LVDSB_CLKP	26	LVDSB_CLKN
27	N/C	28	N/C
29	Ground	30	Ground

J21 : SATA Power Connector



PIN No.	Signal Description
1	+12V
2	Ground
3	Ground
4	+5V

J22 : Backlight Connector



PIN No.	Signal Description
1	+5V
2	BL_CTRL
3	+12V
4	Ground
5	BL_Enable

Chapter 5

Overview

- 5 Sample Code
- 5.1 Watch Dog Timer
- 5.2 Signal GPIO Signal

5 Sample Code

5.1 Watch Dog Timer

```
#include <stdio.h>
#include <unistd.h>
#include <stdint.h>
#include <sys/io.h>

#define EC_IOSpace 0xE300 // EC IO Space Base Addr = 0xE000
                          // EC Internal Offset = 0x300
                          // EC IO Address = Base Addr + Internal
                          offset

#define WDTCFG          0x06 // WDT Timer Control Register
                          // Bit 6: Write 1 to clear WDT pin event
                          (COMe Only)
                          // Bit 4: 1: Driving WDT pin to Carrier
                          (COMe Only)
                          //          0: System Reset
                          // Bit 1: 1: Min Mode
                          //          0: Second Mode
                          // Bit 0: 1: Enable WDT

#define WDTMIN          0x07 // WDT Timer Counter Register
                          (Minute)
#define WDTSEC          0x08 // WDT Timer Counter Register
                          (Second)

int Read_EC_SRAM(int offset)
{
    int Temp;
    Temp = inb_p(EC_IOSpace+offset);
}
```

```
        return Temp;
    }

void Write_EC_SRAM(int offset, int value)
{
    outb_p(value, EC_IOSpace+offset);
}

//-----
// Reset WDT pin status
//-----
int WDT_Reset()
{
    int Temp;

    Temp = Read_EC_SRAM(WDTCFG);
    Write_EC_SRAM(WDTCFG, (Temp|0x40)); // Bit 6: Write 1 to clear WDT
    pin event
}

//-----
// Main Function
//-----
int main (int argc, char ** argv)
{
    int Temp;

    // Initial
    if(iopl(3)!=0){
printf("error: I/O Permission Error!\n");
        return 1;
    }
}
```

```

// Enable WDT 10min, 20sec
Write_EC_SRAM(WDTSEC,5);           // 5 Sec
Write_EC_SRAM(WDTMIN,1);           // 1 min

// Enable WDT 5sec and WDT pin mode
Temp = Read_EC_SRAM(WDTCFG);
Write_EC_SRAM(WDTCFG,(Temp|0x13)); // Bit4: 1: Driving WDT pin
                                   // BIT1: 1: Minute Mode
                                   // Bit0: 1: Enable WDT

// Check Current WDT status
while((Read_EC_SRAM(WDTCFG)&0x01) != 0)
{
printf("WDT          Counting:          %d          M.,          %d\n",
Read_EC_SRAM(WDTMIN),Read_EC_SRAM(WDTSEC));
}
}

```

5.2 Signal GPIO Signal

```

#include <stdio.h>
#include <unistd.h>
#include <stdint.h>
#include <sys/io.h>

#define EC_IOSpace 0xE300 // EC IO Space Base Addr = 0xE000
                          // EC Internal Offset = 0x300
                          // EC IO Address = IO Space Base Addr
                          + Internal offset

#define GPCR 0x2B // GPIO Control Register, Bit7 = GPO3, Bit6 =
GPO2, ...,
                          // Bit3 = GPI3,
Bit2 = GPI2, ...,

```

```

// 0: Output; 1: Input

#define GPDR 0x2C      // GPIO Status Register, Bit7 = GPO3, Bit6 =
GPO2, ...,
                        //                               Bit3 = GPI3,
Bit2 = GPI2, ...,
                        // 0: Low; 1: High

int Read_EC_SRAM(int offset)
{
    int Temp;
    Temp = inb_p(EC_IOSpace+offset);
    return Temp;
}

void Write_EC_SRAM(int offset, int value)
{
    outb_p(value,EC_IOSpace+offset);
}

int main (int argc, char ** argv)
{
    int Temp;

    // Initial
    if(iopl(3)!=0){
printf("error: I/O Permission Error!¥n");
        return 1;
    }
    // Get GPI status
    Temp = Read_EC_SRAM(GPDR);                               //Bit3-0: GPI3-0
status

    // Set GPO4 Output & High

```

```
Temp = Read_EC_SRAM(GPDR);  
Write_EC_SRAM(GPDR,Temp|0x80);           //Bit7-4: Set GPO3-0  
status, 0: Low 1: High
```

Chapter 6

Overview

- 6 BIOS Setup Items
- 6.1 Entering Setup -- Launch System Setup
- 6.2 Main
- 6.3 Configuration

6 BIOS Setup Items

NANO-6064 is equipped with the AMI BIOS stored in Flash ROM. These BIOS has a built-in Setup program that allows users to modify the basic system configuration easily. This type of information is stored in SPI Flash so that it is retained during power-off periods. When system is turned on, NANO-6064 communicates with peripheral devices and checks its hardware resources against the configuration information stored in the CMOS memory. If any error is detected, or the CMOS parameters need to be initially defined, the diagnostic program will prompt the user to enter the SETUP program. Some errors are significant enough to abort the start up.

6.1 Entering Setup -- Launch System Setup

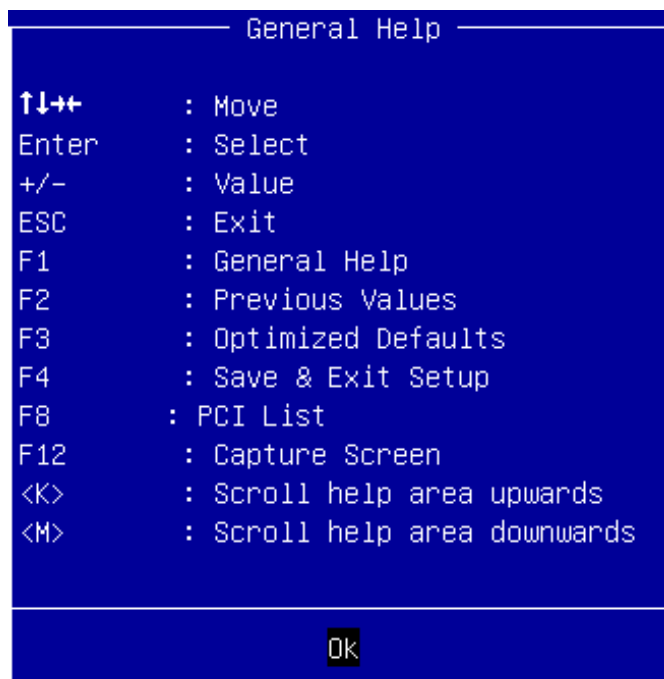
Power on the computer and the system will start POST (Power On Self Test) process. When the message below appears on the screen, press key will enter BIOS setup screen.

Press to enter SETUP

If the message disappears before responding and still wish to enter Setup, please restart the system by turning it OFF and On or pressing the RESET button. It can be also restarted by pressing <Ctrl>, <Alt>, and <Delete> keys on keyboard simultaneously.

Press <F1> to Run General Help or Resume

The BIOS setup program provides a General Help screen. The menu can be easily called up from any menu by pressing <F1>. The Help screen lists all the possible keys to use and the selections for the highlighted item. Press <Esc> to exit the Help screen.



6.2 Main

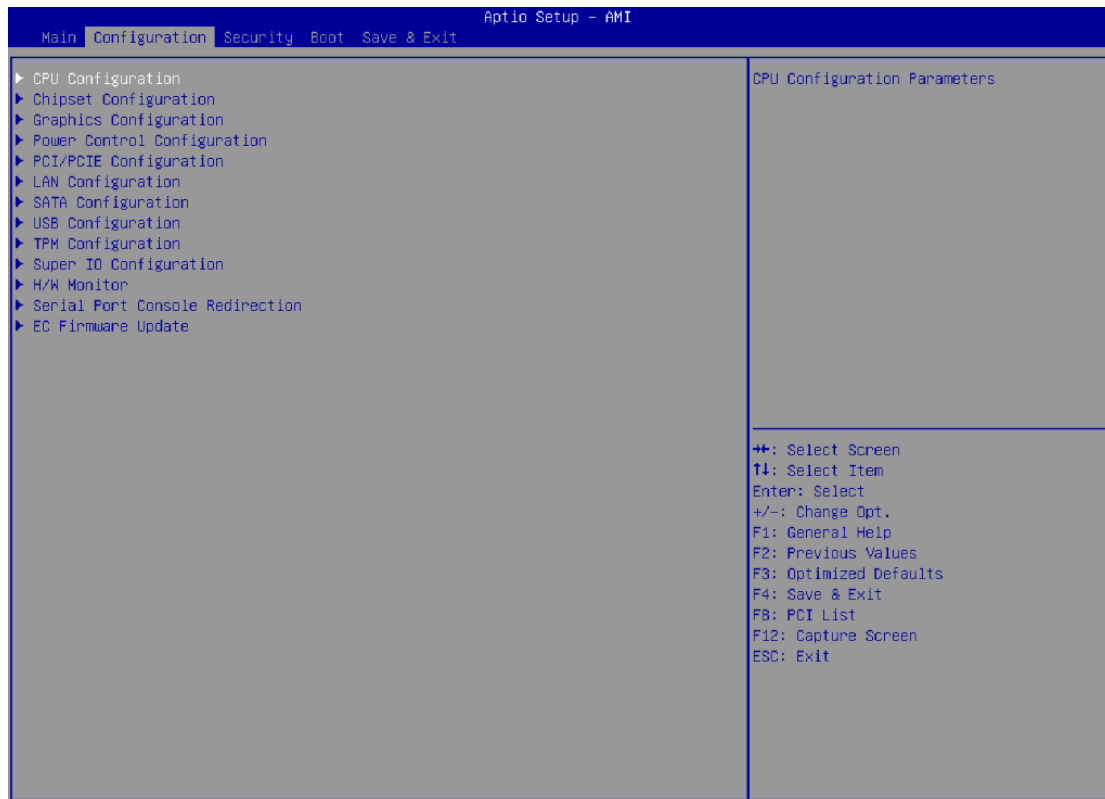


Feature	Description	Options
System Date	The date format is <Day>, <Month><Date><Year>. Use [+] or [-] to configure system Date.	
System Time	The time format is <Hour><Minute><Second>. Use [+] or [-] to configure system Time.	

Detailed System Information

Main	
Aptio Setup - AMI	
FSP Information	
FSP version	0C.02.81.70
RC version	0C.00.81.70
Build Date	08:27 07/25/2022
FSP Mode	Dispatch Mode
Board Information	
Board Name	NANO-6064
Processor Information	
Name	AlderLake ULX
Type	Intel(R) Core(TM) i3-N305
Speed	1800 MHz
ID	0xB06E0
Stepping	A0
Package	Not Implemented Yet
Number of Efficient-cores	8Core(s) / 8Thread(s)
Microcode Revision	B
GT Info	0x46D0
eDRAM Size	N/A
IGFX GOP Version	21.0.1056
Memory RC Version	0.0.4.33
Total Memory	8192 MB
Memory Frequency	2400 MHz
MC 0 Ch 0 DIMM 0	Populated & Enabled
Size	8192 MB (DDR4)
PCH Information	
Name	PCH-N
Stepping	A0
ChipsetInit Base Revision	2
ChipsetInit OEM Revision	0
Package	Not Implemented Yet
TXT Capability of Platform/PCH	Unsupported
Production Type	Production
Dual Output Fast Read support	Supported
Read ID/Status Clock Freq	50 MHz
Write and Erase Clock Freq	50 MHz
Fast Read Clock Freq	50 MHz
Fast Read support	Supported
Number of Components	1 Component
SPI Component 0 Density	32 MB
eSPI Flash Sharing Mode	G3
EC PECI Mode	Legacy PECI mode
ME FW Version	16.50.0.1215
ME Firmware SKU	Consumer SKU
PMC FW Version	160.50.0.1008

6.3 Configuration



6.3.1 CPU Configuration

Configuration Aptio Setup - AMI		
CPU Configuration		
Type	Intel(R) Core(TM) i3-N305	Number of E-cores to enable in each processor package. Note: Number of Cores and E-cores are looked at together. When both are {0,0}, Pcode will enable all cores.
ID	0x806E0	
Speed	1800 MHz	
L1 Data Cache	32 KB x 8	
L1 Instruction Cache	64 KB x 8	
L2 Cache	2048 KB x 2	
L3 Cache	6 MB	
VMX	Supported	
SMX/TXT	Not Supported	
Active Efficient-cores	[All]	
Boot performance mode	[Turbo Performance]	++: Select Screen T1: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit F8: PCI List F12: Capture Screen ESC: Exit
Intel (VMX) Virtualization Technology	[Enabled]	
Intel(R) SpeedStep(tm)	[Enabled]	
Intel(R) Speed Shift Technology	[Enabled]	
Turbo Mode	[Enabled]	
C states	[Enabled]	
Enhanced C-states	[Enabled]	
C-State Auto Demotion	[C1]	
C-State Un-demotion	[C1]	
Package C-State Demotion	[Enabled]	
Package C-State Un-demotion	[Enabled]	
CState Pre-Wake	[Enabled]	
IO MWAIT Redirection	[Disabled]	
Package C State Limit	[Auto]	

Feature	Description	Options
Active Efficient-Cores	Number of E-cores to enable in each processor package. Note: Number of Cores and E-cores are looked at together, When both are {0,0}, Pcode will enable all cores.	★All, 1, 2, 3, 4, 5, 6, 7
Boot performance mode	Select the performance state that the BIOS will set starting from reset vector	★Turbo Performance Max Battery Max Non-Turbo Performance
Intel (VMX) Virtualization Technology	When enabled, a VMM can utilize the additional hardware capabilities provided by Vander pool Technology.	Disabled, ★Enabled
Intel®Speed Step™	Allows more than two frequency ranges to be supported.	Disabled, ★Enabled

Intel® Speed Shift Technology	Enable/Disable Intel® Speed Shift Technology support. Enabling will expose the CPPC v2 interface to allow for hardware controlled P-states	Disabled, ★Enabled
Turbo Mode	Enable/Disable processor Turbo Mode (requires EMTTM enabled too). AUTO means enabled.	Disabled, ★Enabled
C states	Enable/disable CPU Power Management. Allows CPU to go to C states when it's not 100% utilized	Disabled, ★Enabled
Enhanced C-states	Enable/Disable C1E. When enabled, CPU will switch to minimum speed when all cores enter C-state	Disabled, ★Enabled
C-State Auto Demotion	Configure C-State Auto Demotion	Disable, ★C1
C-State Un-demotion	Configure C-State Un-demotion	Disable, ★C1
Package C State Demotion	Package C-State Demotion	Disabled, ★Enabled
Package C State Un-demotion	Package C-State Un-demotion	Disabled, ★Enabled
CState Pre-Wake	Disable – Sets bit 30 of POWER_CTL MSR(0x1FC) to 1 to disable the Cstate Pre-Wake	Disabled, ★Enabled
IO MWAIT Redirection	When set, will map IO_read instructions sent to IO registers PMG_IO_BASE_ADDRBASE+offset to MWAIT(offset)	★Disabled, Enabled
Package C State Limit	Maximum Package C State Limit Setting. CPU Default: Leaves to Factory default value. Auto: Initializes to deepest available Package C States Limit	C0/C1,C2,C3,C6,C7,C7S,C8,C9,C10,Cpu Default, ★Auto

6.3.2 Chipset Configuration



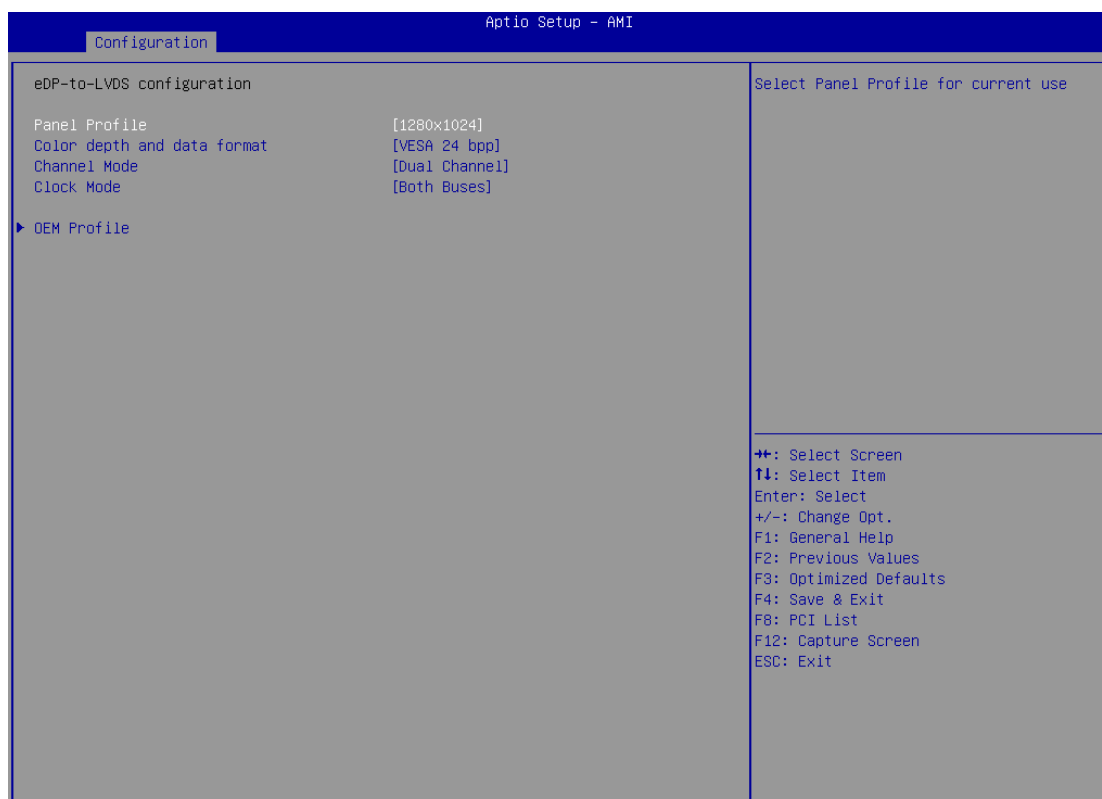
Feature	Description	Options
VT-d	VT-d Capability	★Enabled ,Disabled
Above 4GB MMIO BIOS assignment	Enable/Disable above 4GB Memory Mapped IO BIOS assignment	Enabled ,★Disabled
	This is enabled automatically when Aperture Size is set to 2048MB	
HD Audio	Control Detection of the HD-Audio device.	★Enabled ,Disabled
	Disabled = HDA will be unconditionally disabled	
	Enabled = HDA will be unconditionally enabled	
Port 80h Redirection	Control when the Port 80h cycles are sent.	★LPC Bus, PCIE Bus
Me FW Image Re-Flash	Enable/Disable Me FW Image Re-Flash function.	★Disabled, Enabled

6.3.3 Graphics Configuration



Feature	Description	Options
Primary Display	Select which of IGFX/PEG/PCI Graphics device should be Primary Display Or Select HG for Hybrid Gfx.	★Auto, IGFX, PEGSlot, PCH PCI
Internal Graphics	Keep IGFX enable based on the setup options.	★Auto, Disable, Enable
DVMT Pre-Allocated	Select DVMT 5.0 Pre-Allocated (Fixed) Graphics Memory size used by the Internal Graphics Device.	32M,64M, 96M, 128M, 160M, 12M, 16M,20M, 24M, 28M, 32M/F7,36M,40M,44M,48M,52M,56M, ★60M
DVMT Total Gfx Mem	Select DVMT5.0 Total Graphic Memory size used by the Internal Graphics Device	★256M, 128M, MAX
VBT Select	Select VBT for GOP Driver Select vbt to 'No LVDS' if no need LVDS	★Standard, No LVDS
eDP-to-LVDS configuration	eDP-to-LVDS(PTN3460)	

eDP-to-LVDS configuration



Feature	Description	Options
Panel Profile	Select Panel Profile for current use	640x480, 800x480, 800x600, 1024x768, 1280x800, ★1280x1024, 1366x768, 1440x900, 1920x1080, OEM Profile
Color depth and data format	Select Color depth and data format.	★VESA 24 bpp, JEIDA 24 bpp, VESA and JEIDA 18 bpp
Channel Mode	Select LVDS Channel Mode	Single Channel ★Dual Channel
Clock Mode	Select clock output for LVDS.	Even Bus, Odd Bus, ★Both Buses
OEM Profile	PANEL 1 Help	

OEM Profile: PANEL 1 Configuration

Configuration		Aptio Setup - AMI	
PANEL 1 Configuration Profile Name : empty Rename Profile Color depth and data format [VESA and JEIDA 18 bpp] Channel Mode [Single Channel] Clock Mode [Even Bus] Pixel Clock 0.000 Mhz 2500 H Active Pixels 0 640 H Blank Pixels 0 160 H Offset Pixels 0 16 H Width Pixels 0 96 V Active Lines 0 480 V Blank Lines 0 45 V Offset Lines 0 10 V Width Lines 0 2 H & V sync Signal Polarity [Postive]			
++: Select Screen ↑↓: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit F8: PCI List F12: Capture Screen ESC: Exit			

Feature	Description	Options
Rename Profile	Rename Profile name	
Color depth and data format	Select Color depth and data format.	VESA 24 bpp JEIDA 24 bpp ★VESA and JEIDA 18 bpp
Channel Mode	Select LVDS Channel Mode.	Dual channel ★Single channel
Clock Mode	Select Clock output for LVDS.	Both Buses, ★Even Bus, Odd Bus
Pixel Clock	Pixel Clock (10Khz)	★ 2500
H Active Pixels	H Active Pixels (Pixel)	★ 640
H Blank Pixels	H Blank Pixels (Pixel)	★ 160
H Offset Pixels	H Offset Pixels (Pixel)	★ 16
H Width Pixels	H Width Pixels (Pixel)	★ 96
V Active Lines	V Active Lines (Line)	★ 480
V Blank Lines	V Blank Lines (Line)	★ 45
V Offset Lines	V Offset Lines (Line)	★ 10
V Width Lines	V Width Lines (Line)	★ 2
H & V sync Signal Polarity	Flag: 0x1E Signal Polarity is Postive; 0x18 Signal Polarity is Non-Postive	★ Postive, Non-Postive

6.3.4 Power Control Configuration

Configuration Aptio Setup - AMI		
<div> <div>Power Control Configuration</div> <div> <div>Enable Hibernation</div> <div>ACPI Sleep State</div> <div>Restore AC Power Loss</div> </div> <div> <div>[Enabled]</div> <div>[S3 (Suspend to RAM)]</div> <div>[Power Off]</div> </div> <div> <div>Enables or Disables System ability to Hibernate (OS/S4 Sleep State). This option may not be effective with some operating systems.</div> <div> <div>↔: Select Screen</div> <div>↑↓: Select Item</div> <div>Enter: Select</div> <div>+/-: Change Opt.</div> <div>F1: General Help</div> <div>F2: Previous Values</div> <div>F3: Optimized Defaults</div> <div>F4: Save & Exit</div> <div>F8: PCI List</div> <div>F12: Capture Screen</div> <div>ESC: Exit</div> </div> </div> </div>		
Feature	Description	Options
Enable Hibernation	Enables or Disables System ability to Hibernate (OS/S4 Sleep State). This option may not be effective with some operating systems.	★Enabled, Disabled
ACPI Sleep State	Select the highest ACPI sleep state the system will enter when the SUSPEND button is pressed.	★S3 (Suspend to RAM), Suspend Disabled
Restore AC Power Loss	Specify what state to go to when power is re-applied after a power failure (G3 state)	★Power Off, Power On, Last State

6.3.5 PCI/PCIE Configuration

Configuration Aptio Setup - AMI

PCI/PCIE Configuration

POH PCI Express Root Port

- ▶ PCI Express Root Port 7
- ▶ PCI Express Root Port 9
- ▶ PCI Express Root Port 10

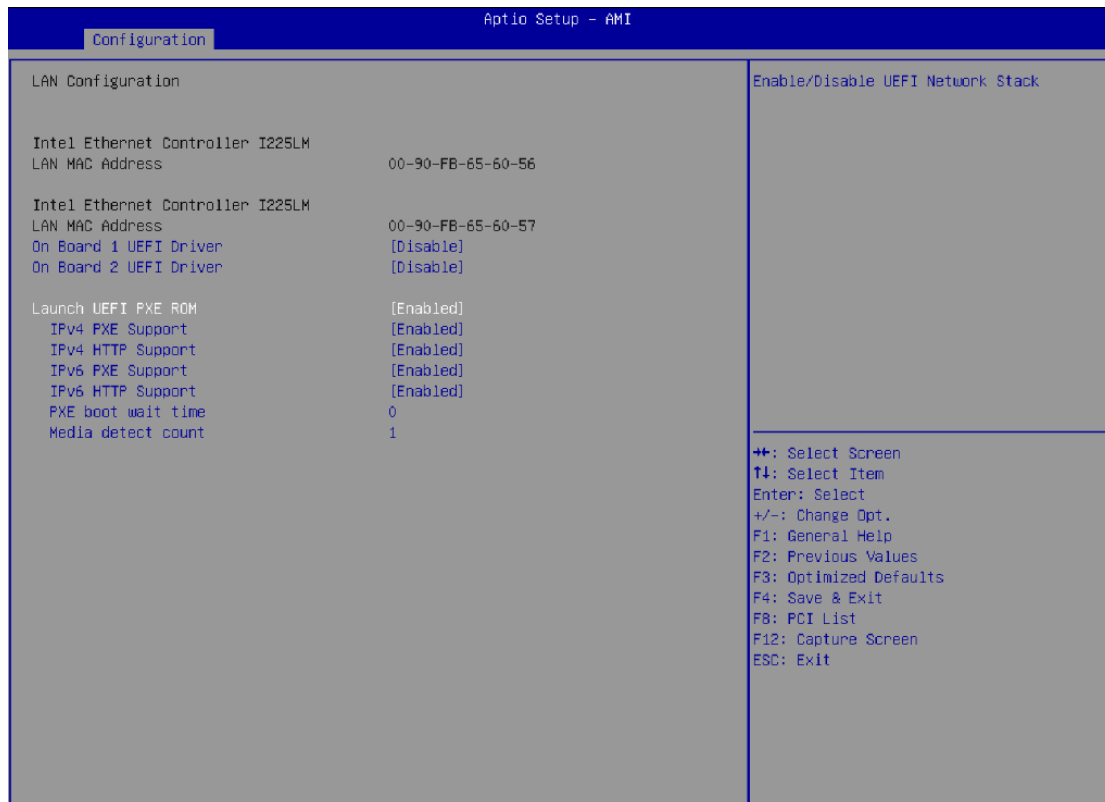
PCI Express Root Port Settings.

←→: Select Screen
 ↑↓: Select Item
 Enter: Select
 +/-: Change Opt.
 F1: General Help
 F2: Previous Values
 F3: Optimized Defaults
 F4: Save & Exit
 F8: PCI List
 F12: Capture Screen
 ESC: Exit

Feature	Description	Options
PCI Express Root Port 7, 9, 10	PCI Express Root Port Setting	

Configuration		
Aptio Setup - AMI		
PCI Express Root Port 7 [Enabled] ASPM [Disabled] PCIe Speed [Auto]		Control the PCI Express Root Port. ** : Select Screen T1 : Select Item Enter : Select +/- : Change Opt. F1 : General Help F2 : Previous Values F3 : Optimized Defaults F4 : Save & Exit F8 : PCI List F12 : Capture Screen ESC : Exit
Feature	Description	Options
PCI Express Root Port	Control the PCI Express Root Port.	★Enabled ,Disabled
ASPM	Set the ASPM Level: Force L0s – Force all links to L0s State AUTO-BIOS auto configure DISABLE – Disables ASPM	★Disabled, L1, Auto
PCIe Speed	Configure PCIe Speed	★Auto, Gen1, Gen2, Gen3

6.3.6 LAN Configuration



Feature	Description	Options
On Board 1 UEFI Driver	Control On Board LAN UEFI Driver Disabled or Enabled.	Enabled, ★ Disabled
On Board 2 UEFI Driver	Control On Board LAN UEFI Driver Disabled or Enabled.	Enabled, ★ Disabled
Launch UEFI PXE ROM	Enable/Disable UEFI Network Stack	Enabled, ★ Disabled
Launch UEFI PXE ROM (Enabled)		
IPv4 PXE Support	Enable/Disable IPv4 PXE boot support. If disabled, IPv4 PXE boot support will not be available.	★ Enabled, Disabled
IPv4 HTTP Support	Enable/Disable IPv4 HTTP boot support. If disabled, IPv4 HTTP boot support will not be available.	★ Enabled, Disabled
IPv6 PXE Support	Enable/Disable IPv6 PXE boot support. If disabled, IPv6 PXE boot support will not be available.	★ Enabled, Disabled
IPv6 HTTP Support	Enable/Disable IPv6 HTTP boot support. If disabled, IPv6 HTTP boot support will not be available.	★ Enabled, Disabled
PXE boot wait time	Wait time in seconds to press ESC key to abort the PXE boot. Use either +/- or numeric keys to set the value.	★ 0
Media detect count	Number of times the presence of media will be checked. Use either +/- or numeric keys to set the value.	★ 1

6.3.7 SATA Configuration

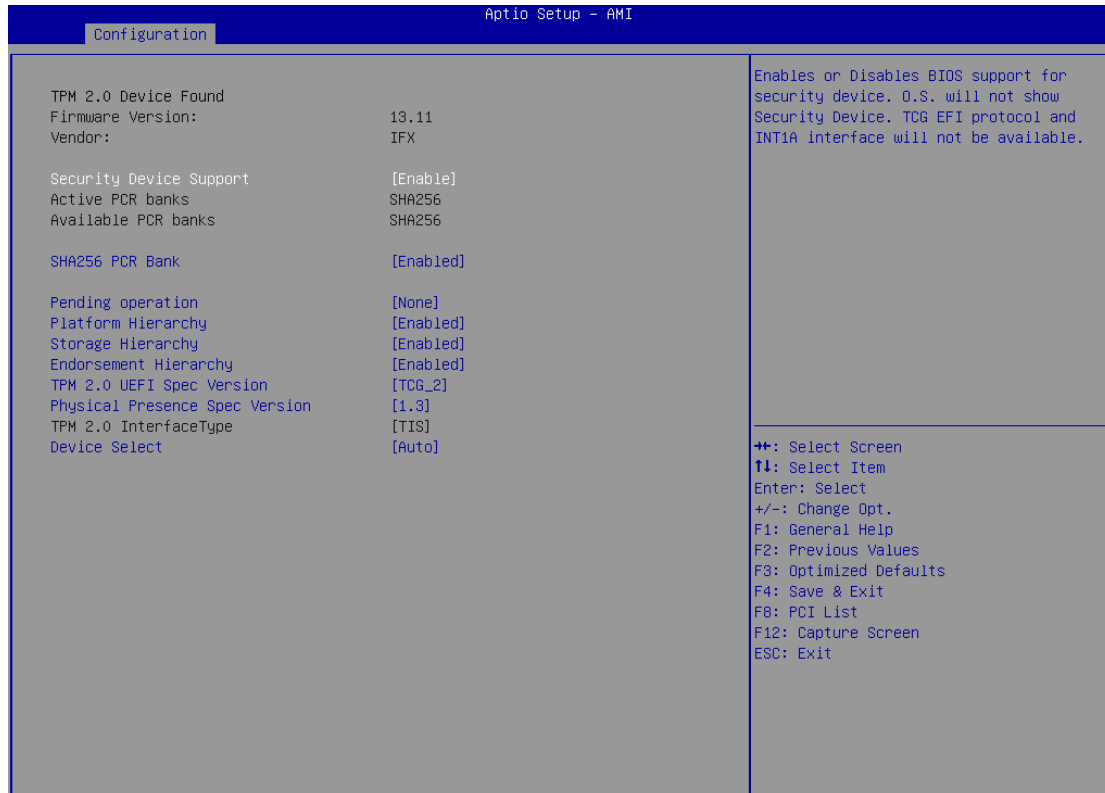


Feature	Description	Options
SATA Controller(s)	Enable/Disable SATA Device	★Enabled , Disabled
Serial ATAPort 0		
Port 0	Enabledor Disabled SATA Port	★Enabled , Disabled
Hot plug	Designates this port as Hot pluggable.	★Disabled, Enabled
SATA Device Type	Identify the SATA port is connected to Solid State Drive or Hard Disk Drive.	Hard Disk Drive, Solid State Drive
SerialATAPort1		
Port 1	Enabledor Disabled SATA Port	★Enabled , Disabled
Hot plug	Designates this port as Hot pluggable.	★Disabled, Enabled
SATA Device Type	Identify the SATA port is connected to Solid State Drive or Hard Disk Drive.	Hard Disk Drive, Solid State Drive

6.3.8 USB Configuration

Configuration		Aptio Setup - AMI	
<div>USB Configuration</div> <div>USB Controllers: 2 XHCIs</div> <div>USB Devices: 2 Drives, 1 Keyboard, 1 Hub</div> <div>USB SS Physical Connector #0 [Enabled]</div> <div>USB SS Physical Connector #1 [Enabled]</div> <div>USB SS Physical Connector #2 [Enabled]</div> <div>USB SS Physical Connector #3 [Enabled]</div> <div>USB HS Physical Connector #0 [Enabled]</div> <div>USB HS Physical Connector #1 [Enabled]</div> <div>USB HS Physical Connector #2 [Enabled]</div> <div>USB HS Physical Connector #3 [Enabled]</div> <div>USB HS Physical Connector #4 [Enabled]</div> <div>USB HS Physical Connector #5 [Enabled]</div> <div>USB HS Physical Connector #6 [Enabled]</div> <div>USB HS Physical Connector #7 [Enabled]</div> <div>XHCI Hand-off [Enabled]</div> <div>USB Mass Storage Driver Support [Enabled]</div> <div>On Board USB Power</div> <div>USB3 Port 3 Route [Connector]</div> <div>USB Port0/1 Power [Enable]</div> <div>USB Port2/3 Power [Enable]</div> <div>Mass Storage Devices:</div> <div>Generic Ultra HS-SD/MMC [Auto]</div> <div>USB [Auto]</div>		<div>Enable/Disable this USB Physical Connector (physical port). Once disabled, any USB devices plug into the connector will not be detected by BIOS or OS.</div> <div>++: Select Screen</div> <div>f1: Select Item</div> <div>Enter: Select</div> <div>+/-: Change Opt.</div> <div>F1: General Help</div> <div>F2: Previous Values</div> <div>F3: Optimized Defaults</div> <div>F4: Save & Exit</div> <div>F8: PCI List</div> <div>F12: Capture Screen</div> <div>ESC: Exit</div>	
Feature	Description	Options	
USB SS Physical Connector #0 ~ #3	Enable/Disable this USB Physical connector (Physical port). Once disabled, any USB devices plug into the connector will not be detected by BIOS or OS.	★Enabled ,Disabled,	
USB HS Physical Connector #0 ~ #7	Enable/Disable this USB Physical connector (Physical port). Once disabled, any USB devices plug into the connector will not be detected by BIOS or OS.	★Enabled ,Disabled	
XHCI Hand-off	This is a workaround for OSeS without XHCI hand-off support. The XHCI ownership change should be claimed by XHCI driver	★Enabled ,Disabled	
USB Mass Storage Driver Support	Enable/Disable USB Mass Storage Driver Support	★Enabled ,Disabled	
USB3 Port 3 Route	Control USB3 Port3 Route to M2 or Connector	★Connector, M.2	
USB Port0/1 Power	Control USB Port Power Enable or Disable	★Enabled ,Disabled	
USB Port2/3 Power	Control USB Port Power Enable or Disable	★Enabled ,Disabled	
Generic Ultra HS-SD/MMC	Mass storage device emulation type. ‘AUTO’ enumerates devices according to their media format. Optical drives are emulated as ‘CDROM’; drives with no media will be emulated according to a drive type.	★Auto, Floppy, Forced FDD, Hard Disk, CD-ROM	

6.3.9 TPM Configuration: TPM 2.0 Device Found



Feature	Description	Options
Security Device Support	Enables or Disables BIOS support for security device. O.S. will not show Security Device. TCG EFI protocol and INT1A Interface will not be available.	★Enabled, Disabled
SHA256 PCR Bank	Enables or Disables SHA256 PCR Bank.	★Enabled, Disabled
Pending operation	Schedule an Operation for the Security Device. Note: Your Computer will reboot during restart in order to change State of Security Device.	★None, TPM Clear
Platform Hierarchy	Enables or Disables Platform Hierarchy.	★Enabled, Disabled
Storage Hierarchy	Enables or Disables Storage Hierarchy.	★Enabled, Disabled
Endorsement Hierarchy	Enables or Disables Endorsement Hierarchy.	★Enabled, Disabled
TPM2.0 UEFI Spec Version	Select the TCG2 Spec Version Support.	★TCG_2, TCG_1_2
	TCG_1_2: the Compatible mode for Win8/Win10.	
	TCG_2: Support new TCG2 protocol and event format for Win10 or later.	

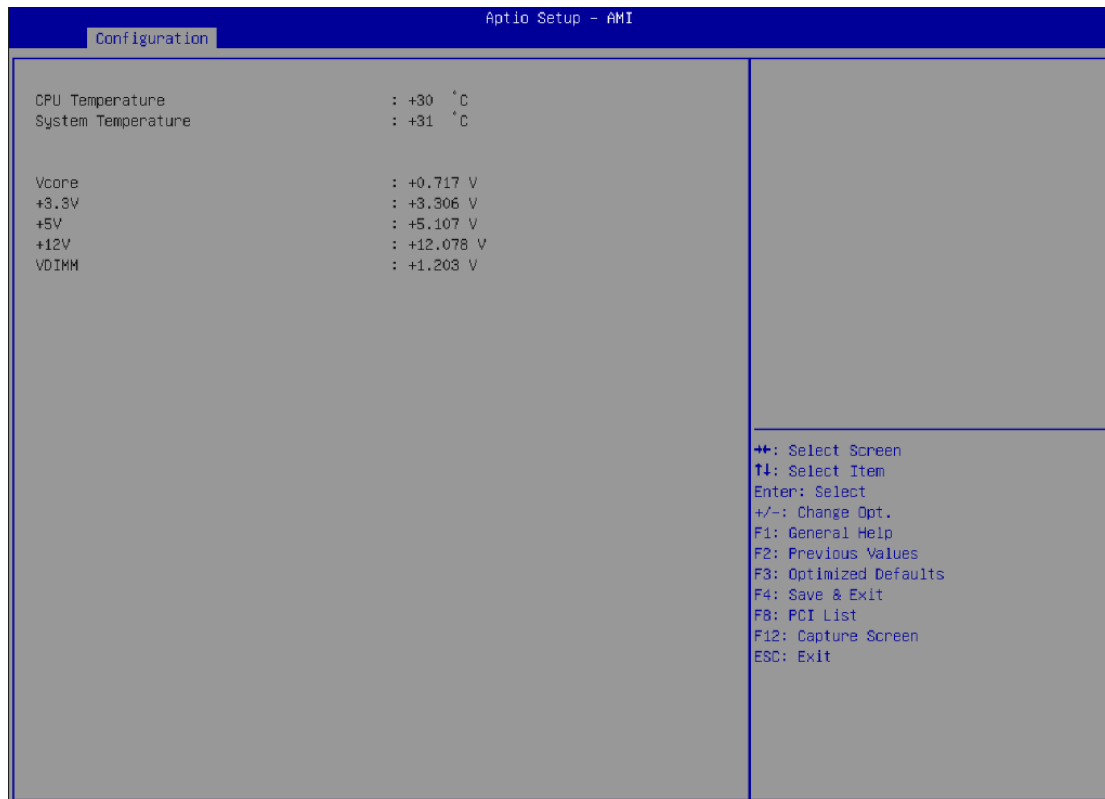
Physical Presence Spec Version	Select to Tell O.S. to Support PPI Spec Version 1.2 or 1.3. Not some HCK tests might not support 1.3.	★1.3, 1.2
Device Select	TPM 1.2 will restrict support to TPM 1.2 devices, TPM 2.0 will restrict support to TPM 2.0 devices, Auto will support both with the default set to TPM 2.0 devices if not found, TPM 1.2 devices will be enumerated.	★Auto, TPM 1.2, TPM 2.0

6.3.10 Super IO Configuration



Feature	Description	Options
ModuleSerialPort 1	Enable or Disable Serial Port (COM)	★Enabled, Disabled
RS-232/422/485 Control Option	SerialPort 3 RS-232/422/485 Control Option	★RS-232, RS-485 HALF DUPLEX, RS-422 FULL DUPLEX,
Watch Dog Timer	Enable/Disable Watch Dog Timer	★Disabled, Enabled
Watch Dog Timer [Enabled]		
Timer Unit	Select Timer count unit of WDT	★Second, Minute
Timer value	Set WDT Timer value seconds / minutes	★20

6.3.11 HW Monitor



6.3.12 Serial Port Console Redirection

Configuration
Aptio Setup - AMI

Serial Port Console Redirection

COM0

Console Redirection [Disabled]

► Console Redirection Settings

Console Redirection Enable or Disable.

←→: Select Screen
 F1: Select Item
 Enter: Select
 +/-: Change Opt.
 F1: General Help
 F2: Previous Values
 F3: Optimized Defaults
 F4: Save & Exit
 F12: Capture Screen
 ESC: Exit

Version 2.21.1278 Copyright (C) 2021 AMI

Feature	Description	Options
Console Redirection	Console Redirection Enable or Disable	★Disabled, Enabled

COM0 Console Redirection Settings:

Configuration
Aptio Setup - AMI

COM0
Console Redirection Settings

Terminal Type [VT100Plus]
 Bits per second [115200]
 Data Bits [8]
 Parity [None]
 Stop Bits [1]
 Flow Control [None]
 VT-UTF8 Combo Key Support [Enabled]
 Recorder Mode [Disabled]
 Resolution 100x31 [Disabled]
 Putty KeyPad [VT100]

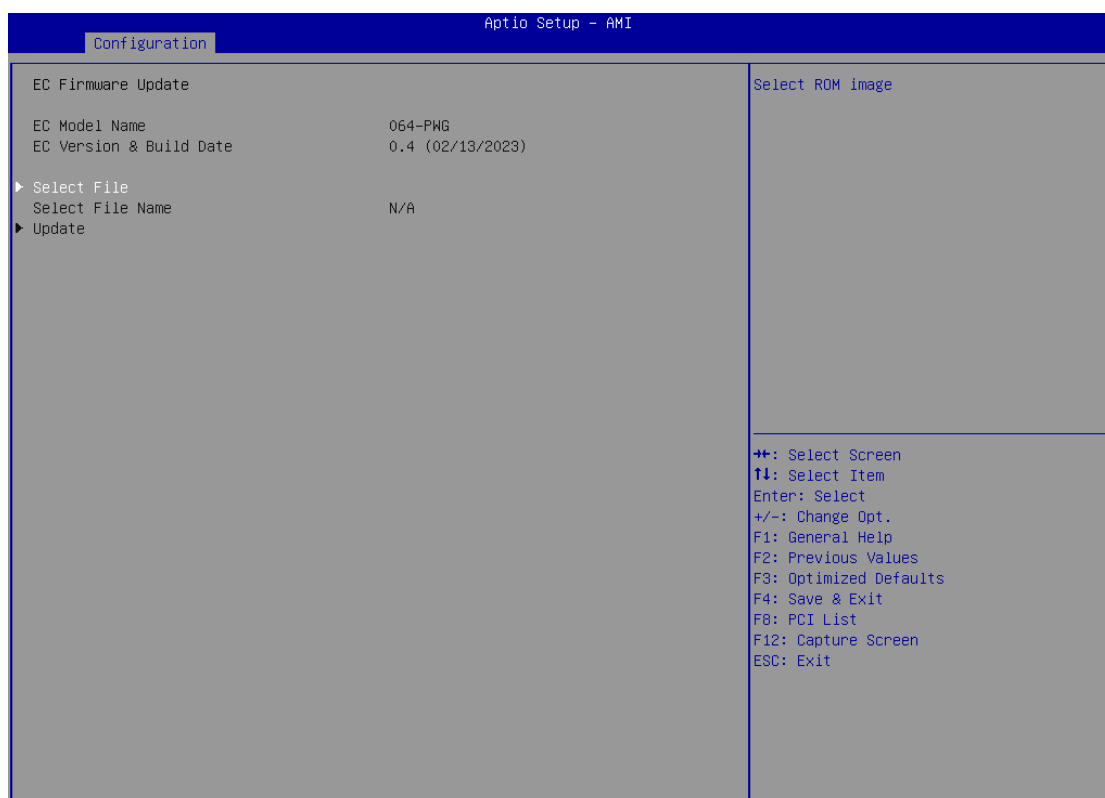
Emulation: ANSI: Extended ASCII char set. VT100: ASCII char set. VT100Plus: Extends VT100 to support color, function keys, etc. VT-UTF8: Uses UTF8 encoding to map Unicode chars onto 1 or more bytes.

** : Select Screen
 ↑↓ : Select Item
 Enter : Select
 +/- : Change Opt.
 F1: General Help
 F2: Previous Values
 F3: Optimized Defaults
 F4: Save & Exit
 F8: PCI List
 F12: Capture Screen
 ESC: Exit

Feature	Description	Options
Terminal Type	Emulation: ANSI: Extended ASCII char set. VT100: ASCII char set. VT100Plus: Extends VT100 to support color, function keys, etc. VT-UTF8: Uses UTF8 encoding to map Unicode chars onto 1 or more bytes.	★VT100Plus, ANSI, VT100, VT-UTF8
Bits per second	Select Serial port transmission speed. The speed must be matched on other side. Long or noisy lines may require lower speeds.	★115200, 9600, 19200, 38400, 57600
Data bits	Data bits	★8, 7
Parity	A parity bit can be sent with the data bits to detect some transmission errors. Even: parity bit is 0 if the num of 1's in the data bits is even. Odd: parity bit is 0 if num of 1's in the data bits is odd. Mark: parity bit is always 1. Space parity bit is always 0. Mark and Space Parity do not allow for error detection. They can be used as an additional data bit.	★None, Even, Odd, Mark, Space
Stop Bits	Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may require more than 1 stop bit.	★1,2
Flow Control	Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signal.	★None, Hardware RTS/CTS

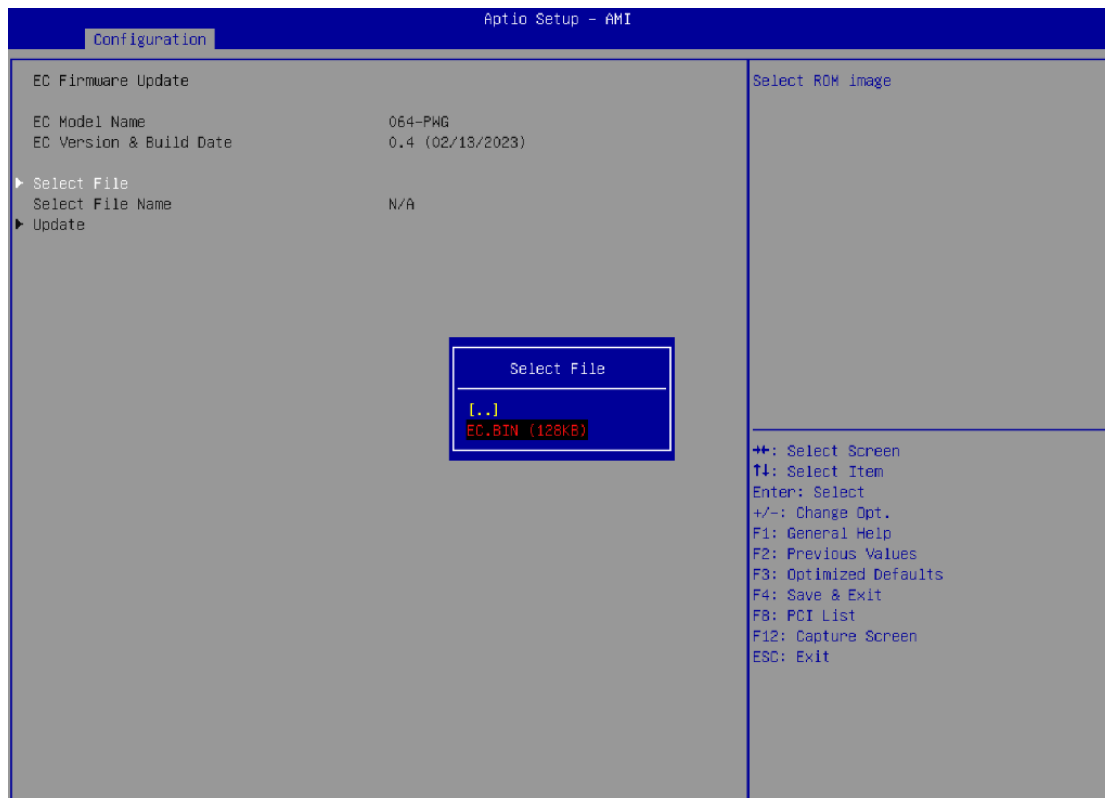
VT-UTF8 Combo Key Support	Enable VT-UTF8 Combination Key Support for ANSI/VT100 terminals	★Enabled, Disabled
Recorder Mode	With this mode enabled only text will be sent. This is to capture Terminal data.	★Disabled, Enabled
Resolution 100x31	Enables or disables extended terminal resolution	★Disabled, Enabled
Putty KeyPad	Select FunctionKey and KeyPad on Putty	★VT100, LINUX,XTERMR6, SCO,ESCN,VT400

6.3.13 EC Firmware Update

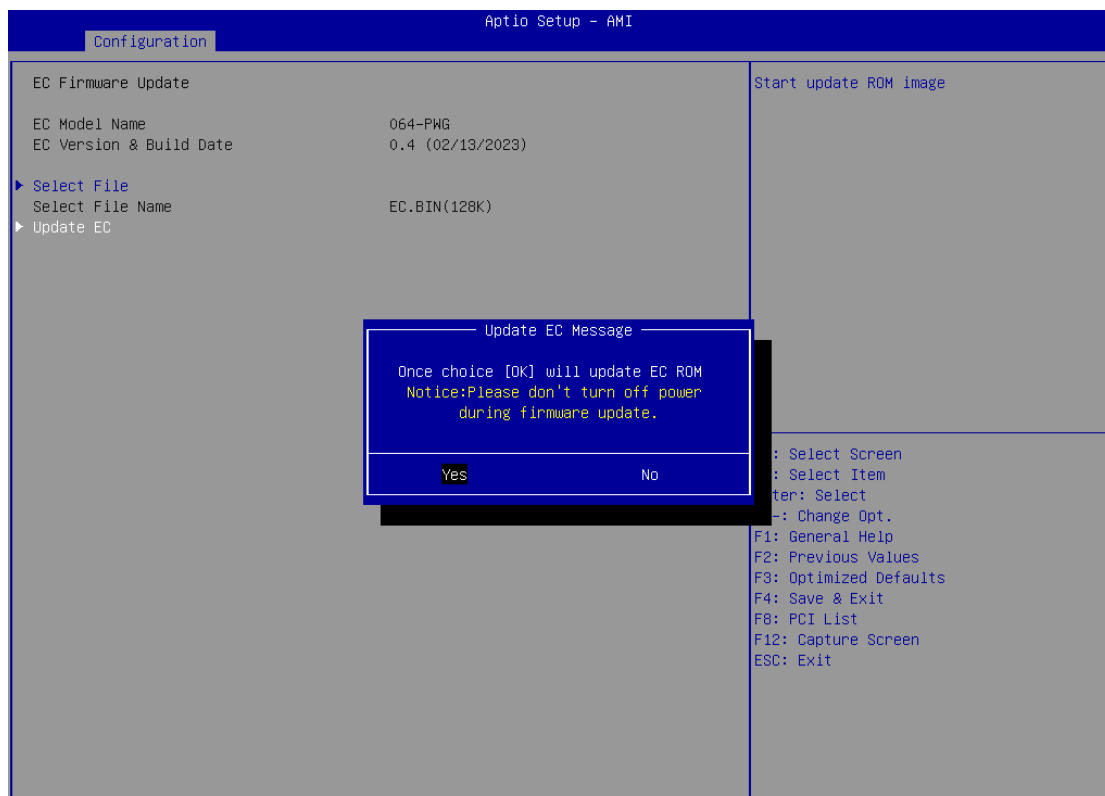


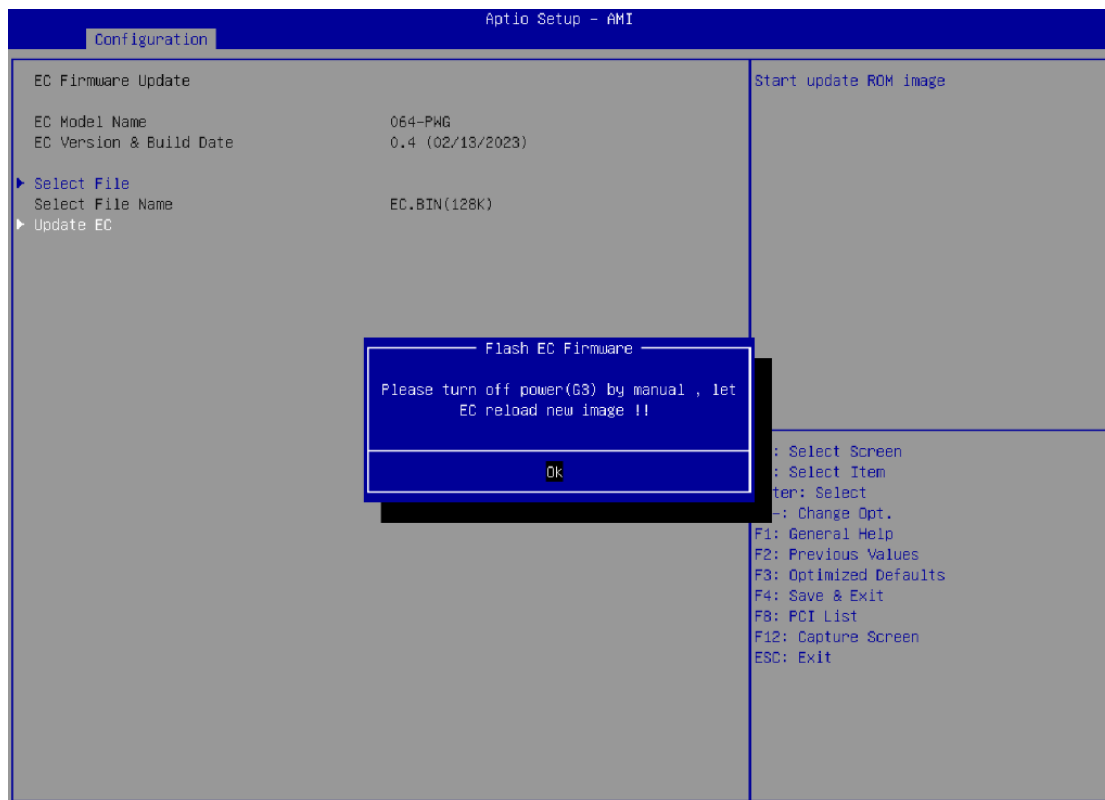
Feature	Description	Options
Select File	Select BIOS BIN file in (USB) drive to update	
Update	Start update ROM image	

Select file

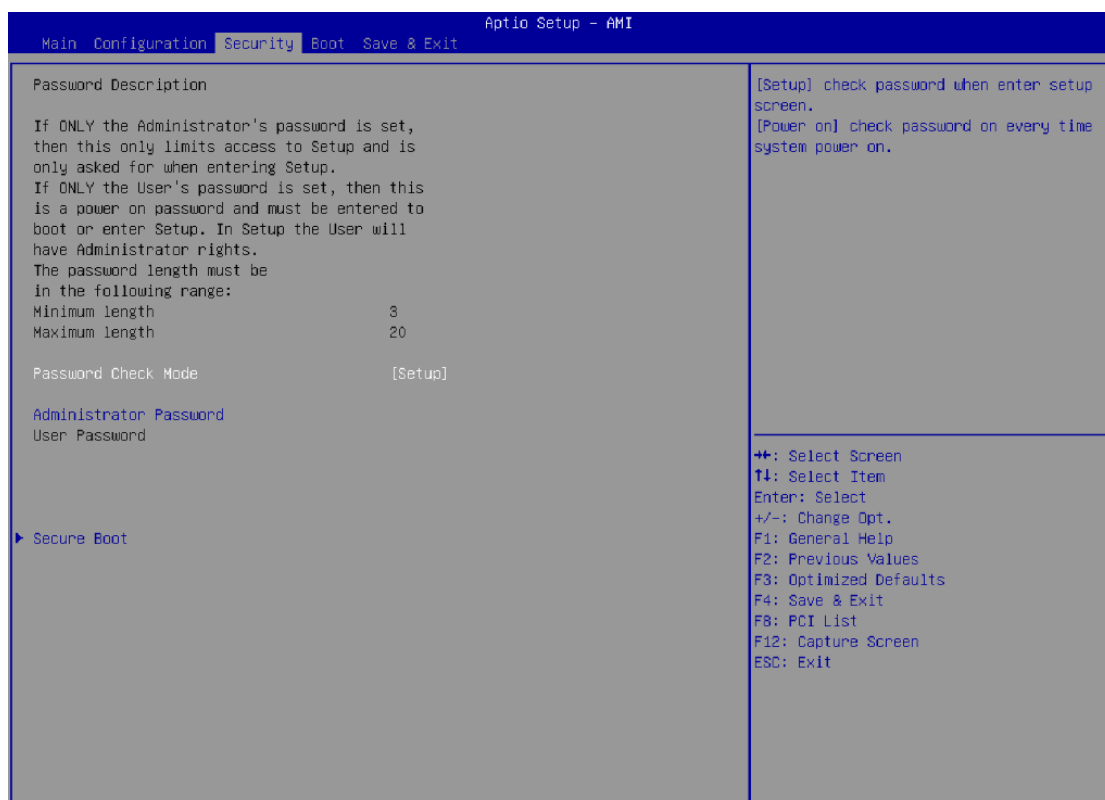


6.3.14 Update EC





6.3.15 Security



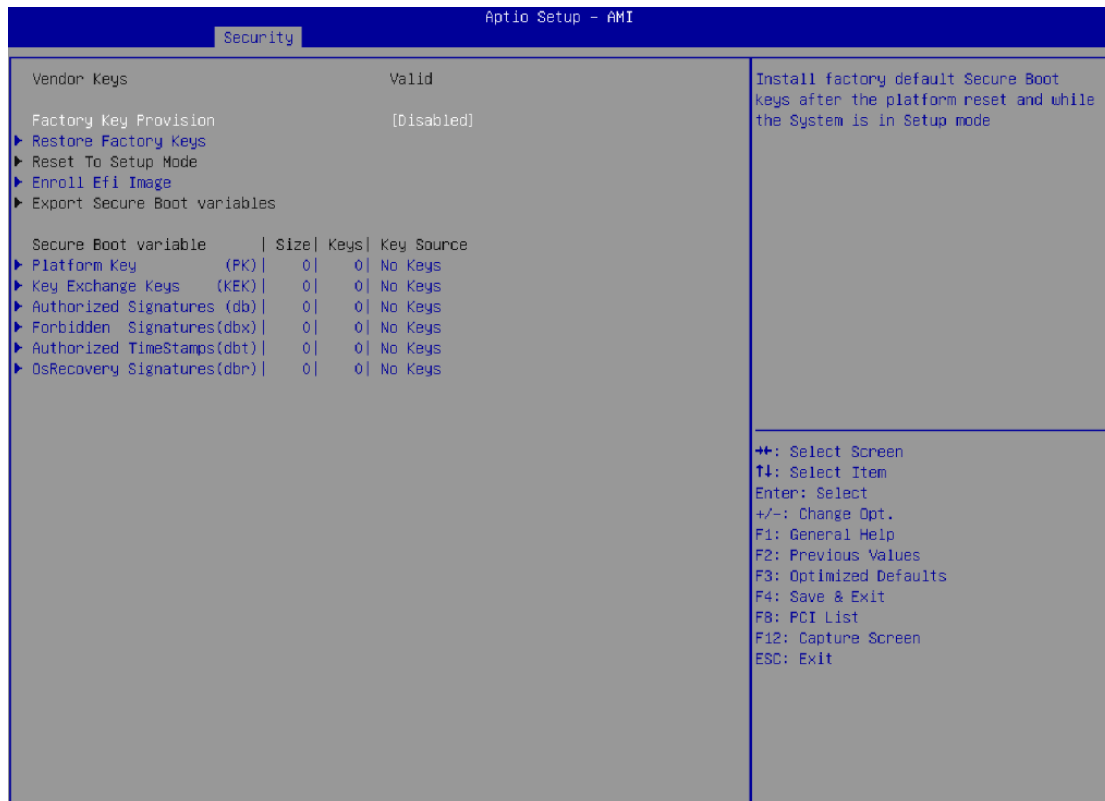
Feature	Description	Options
Password Check Mode	[Setup] check password when enter setup screen. [Power on] check password on every time system power on.	★Setup, Power On
Administrator Password	Set Administrator Password	
Secure Boot	Secure Boot configuration	

Secure Boot



Feature	Description	Options
Secure Boot	Secure Boot feature is Active if Secure Boot is Enabled, Platform Key (PK) is enrolled and the System is in User mode. The mode change requires platform reset.	★Disabled, Enabled
Secure Boot Mode	Secure Boot Mode options: Standard or Custom. In Custom mode, Secure Boot Policy variables can be configured by a physically present user without full authentication	★Custom, Standard
Restore Factory keys	Force System to User Mode. Install factory default Secure Boot key databases	Yes, No
Key Management	Enables expert users to modify Secure Boot Policy variables without variable authentication	

Key Management



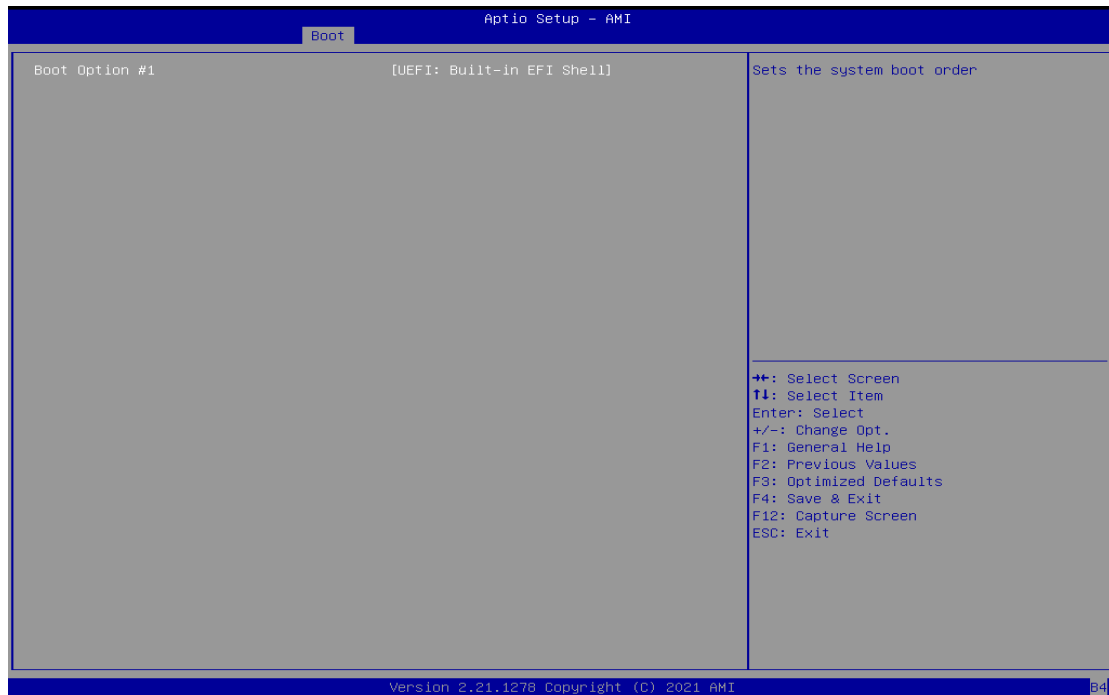
Feature	Description	Options
Factory keys Provision	Install factory default Secure Boot key after the platform reset and while the System is in Setup mode.	★Disabled, Enabled
Restore Factory keys	Force System to User Mode. Install factory default Secure Boot key databases	Yes, No
Enroll Efi Image	Allow Efi image to run in Secure Boot mode. Enroll SHA256 Hash certificate of a PE image into Authorized Signature Database (db)	
Platform Key(PK)	Enroll Factory Defaults or load certificates from a file:	
	1.Public Key Certificate:	
	a)EFI_SIGNATURE_LIST	
	b) EFI_CERT_X509 (DER)	
	c) EFI_CERT_RSA2048 (bin)	
Key Exchange Keys(KEK)	d)EFI_CERT_SHAXXX	
Authorized Signatures(db)	2.Authenticated UEFI Variable	
Forbidden Signatures(dbx)	3.EFI PE/COFF Image(SHA256)	
Authorized TimeStamps(dbt)	Key Source:	
OsRecovery Signatures(dbr)	Factory, Modified, Mixed	

6.3.16 Boot

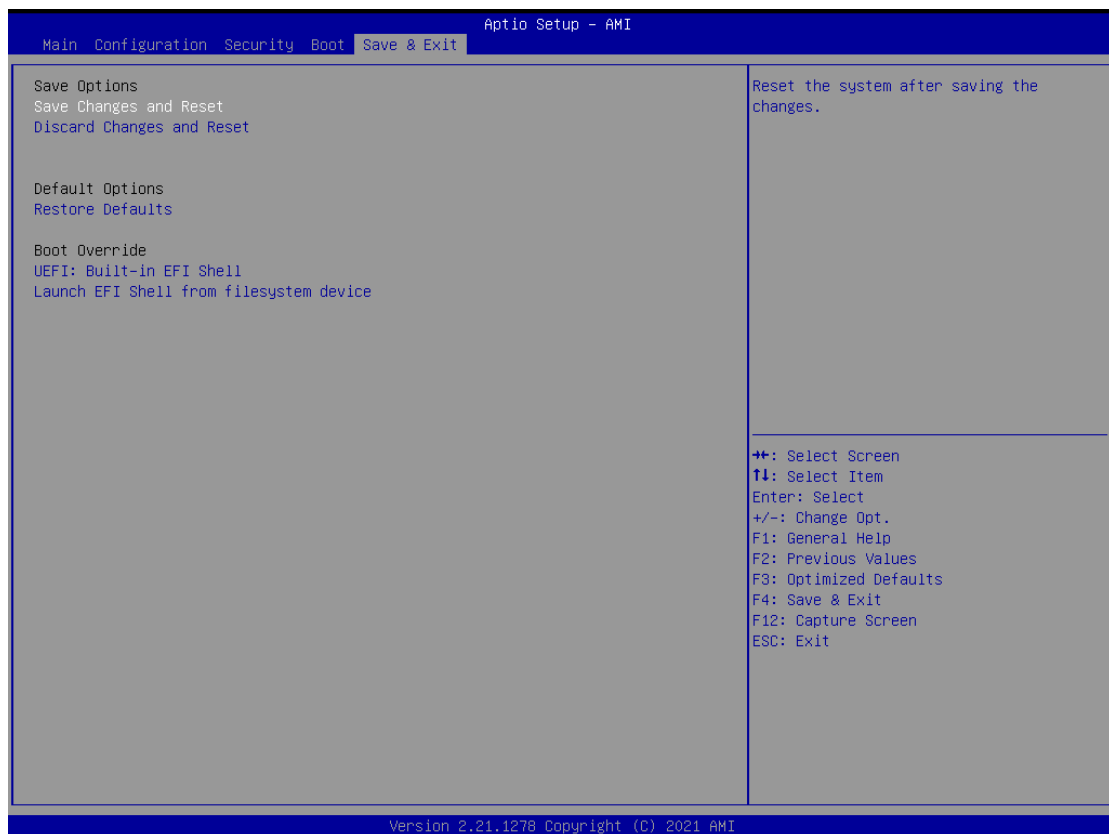


Feature	Description	Options
Setup Prompt Timeout	Number of seconds to wait for setup activation key. 65535(0xFFFF) means indefinite waiting.	★1
BootupNumLockState	Select the keyboard NumLock state.	★On, Off
Full Screen LOGO	Enables or disables Quiet Boot option and Full screen Logo.	★Disabled, Enabled
Boot Option #1 ~ #5	Sets the system boot order	Hard Disk, UEFI AP: UEFI: Built-in EFI Shell, CD/DVD, USB Device; Network, Disabled
UEFI Application Boot Priorities	Specifies the Boot Device Priority sequence from available UEFI Application	

UEFI Application Boot Priorities:



6.3.17 Save & Exit



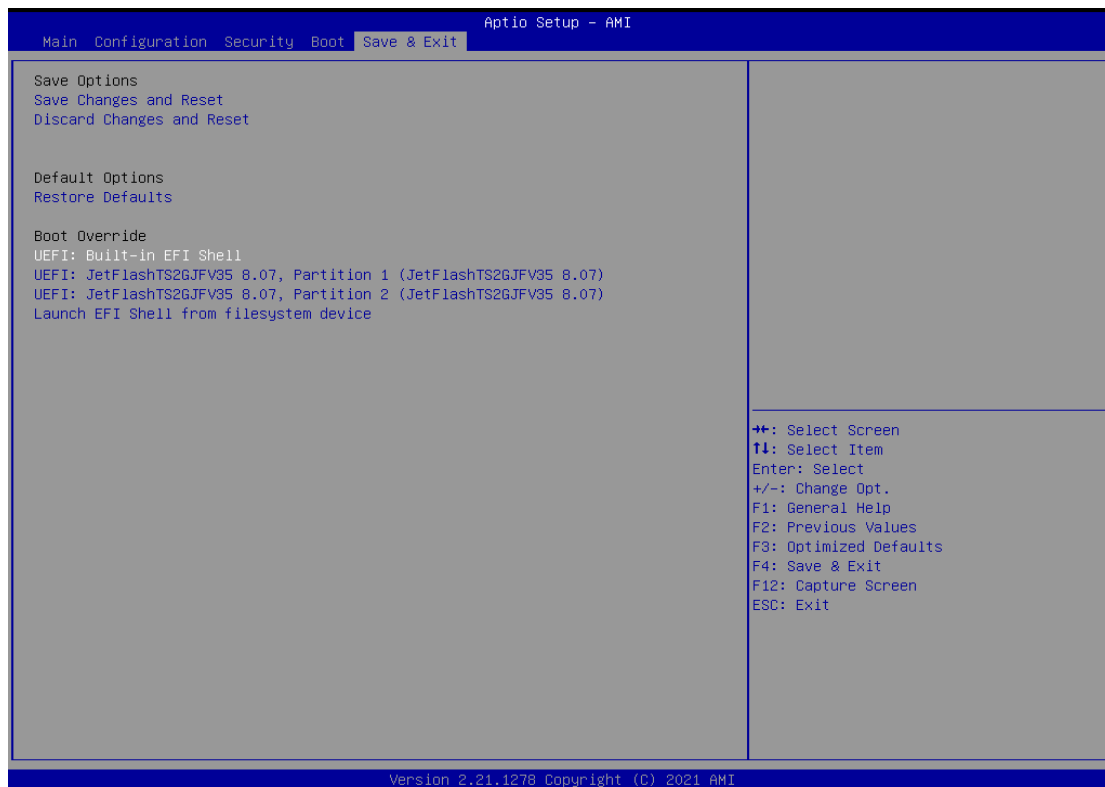
Feature	Description	Options
Save Changes and Reset	Reset the system after saving the changes.	
Discard Changes and Reset	Reset system setup without saving any changes.	
Restore Defaults	Restore/Load Default values for all the setup options.	
UEFI: Built-in EFI Shell		
Launch EFI Shell from filesystem device	Attempts to Launch EFI Shell application (Shell.efi) from one of the available filesystem devices.	

NANO-6064 BIOS / EC UEFI Update SOP process under UEFI Shell

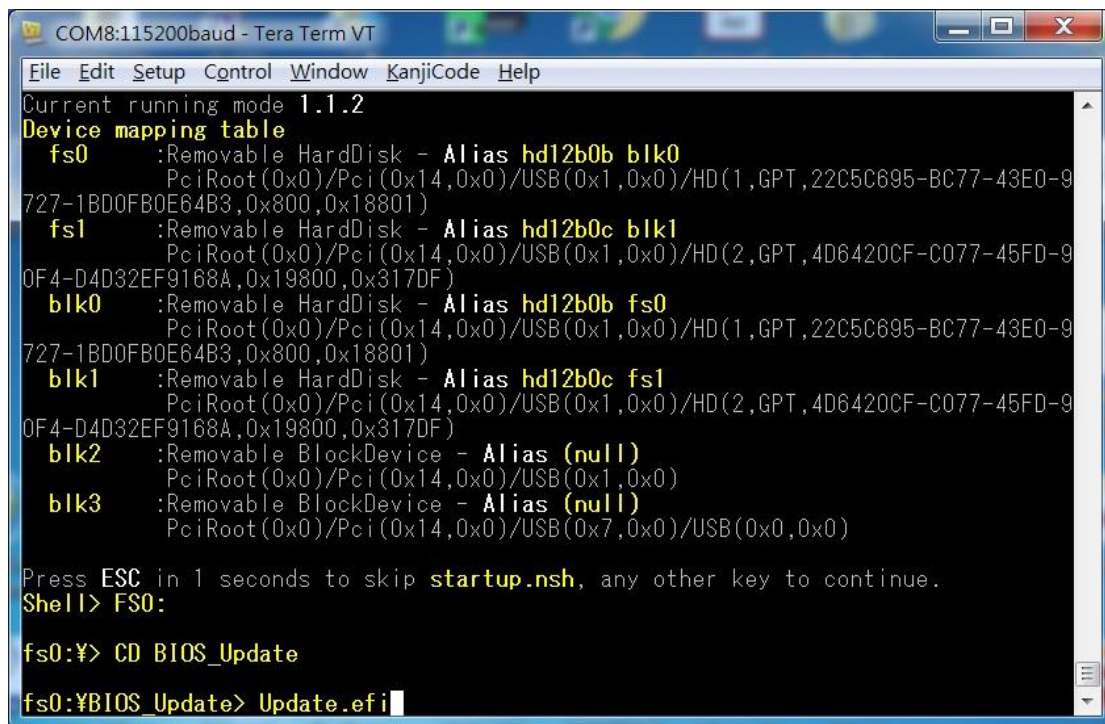
Step 1. Prepare a USB DOK.

Step 2. Unzip BIOS update file to the USB DOK.

Step 3. Plug the USB DOK into the target system and then boot in UEFI Shell by selecting UEFI: Built-in EFI Shell in the BIOS Save & Exit page.



Step 4. Under the UEFI shell, direct to your USB DOK, below picture is an example using fs0. Then direct to the folder with BIOS / EC updated file and then enter command: "Update.efi" to start updating BIOS / EC.



```

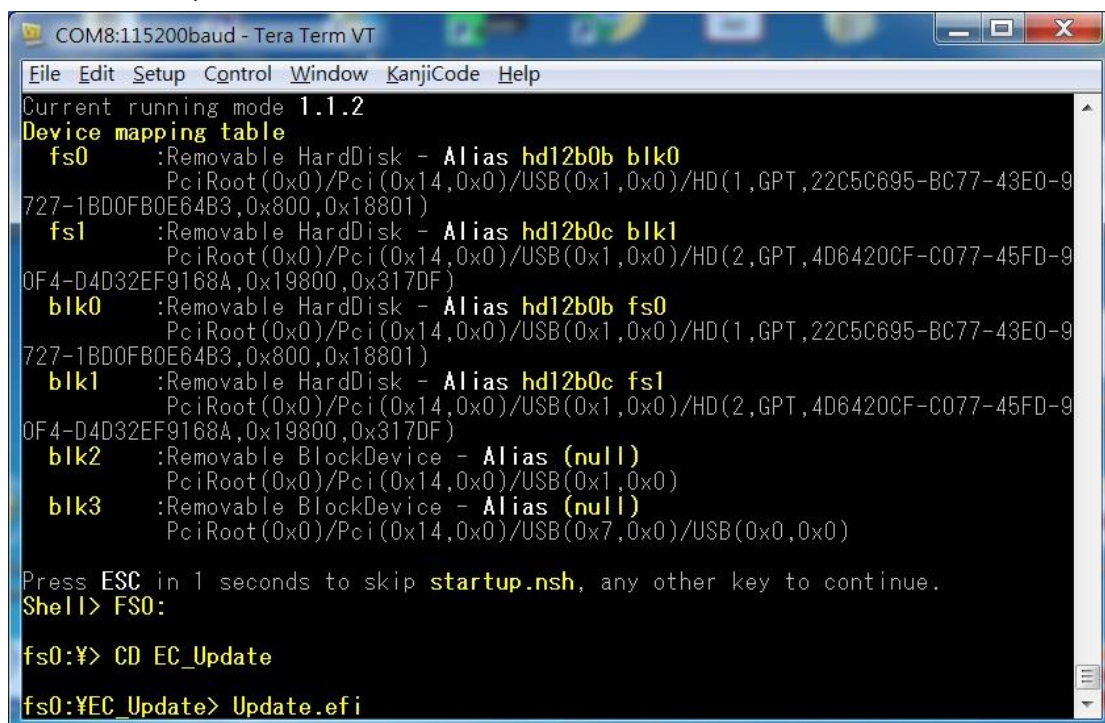
COM8:115200baud - Tera Term VT
File Edit Setup Control Window KanjiCode Help
Current running mode 1.1.2
Device mapping table
fs0 :Removable HardDisk - Alias hd12b0b blk0
      PciRoot(0x0)/Pci(0x14,0x0)/USB(0x1,0x0)/HD(1,GPT,22C5C695-BC77-43E0-9
727-1BD0FB0E64B3,0x800,0x18801)
fs1 :Removable HardDisk - Alias hd12b0c blk1
      PciRoot(0x0)/Pci(0x14,0x0)/USB(0x1,0x0)/HD(2,GPT,4D6420CF-C077-45FD-9
0F4-D4D32EF9168A,0x19800,0x317DF)
blk0 :Removable HardDisk - Alias hd12b0b fs0
      PciRoot(0x0)/Pci(0x14,0x0)/USB(0x1,0x0)/HD(1,GPT,22C5C695-BC77-43E0-9
727-1BD0FB0E64B3,0x800,0x18801)
blk1 :Removable HardDisk - Alias hd12b0c fs1
      PciRoot(0x0)/Pci(0x14,0x0)/USB(0x1,0x0)/HD(2,GPT,4D6420CF-C077-45FD-9
0F4-D4D32EF9168A,0x19800,0x317DF)
blk2 :Removable BlockDevice - Alias (null)
      PciRoot(0x0)/Pci(0x14,0x0)/USB(0x1,0x0)
blk3 :Removable BlockDevice - Alias (null)
      PciRoot(0x0)/Pci(0x14,0x0)/USB(0x7,0x0)/USB(0x0,0x0)

Press ESC in 1 seconds to skip startup.nsh, any other key to continue.
Shell> FS0:

fs0:¥> CD BIOS_Update
fs0:¥BIOS_Update> Update.efi

```

(BIOS File Update)



```

COM8:115200baud - Tera Term VT
File Edit Setup Control Window KanjiCode Help
Current running mode 1.1.2
Device mapping table
fs0 :Removable HardDisk - Alias hd12b0b blk0
      PciRoot(0x0)/Pci(0x14,0x0)/USB(0x1,0x0)/HD(1,GPT,22C5C695-BC77-43E0-9
727-1BD0FB0E64B3,0x800,0x18801)
fs1 :Removable HardDisk - Alias hd12b0c blk1
      PciRoot(0x0)/Pci(0x14,0x0)/USB(0x1,0x0)/HD(2,GPT,4D6420CF-C077-45FD-9
0F4-D4D32EF9168A,0x19800,0x317DF)
blk0 :Removable HardDisk - Alias hd12b0b fs0
      PciRoot(0x0)/Pci(0x14,0x0)/USB(0x1,0x0)/HD(1,GPT,22C5C695-BC77-43E0-9
727-1BD0FB0E64B3,0x800,0x18801)
blk1 :Removable HardDisk - Alias hd12b0c fs1
      PciRoot(0x0)/Pci(0x14,0x0)/USB(0x1,0x0)/HD(2,GPT,4D6420CF-C077-45FD-9
0F4-D4D32EF9168A,0x19800,0x317DF)
blk2 :Removable BlockDevice - Alias (null)
      PciRoot(0x0)/Pci(0x14,0x0)/USB(0x1,0x0)
blk3 :Removable BlockDevice - Alias (null)
      PciRoot(0x0)/Pci(0x14,0x0)/USB(0x7,0x0)/USB(0x0,0x0)

Press ESC in 1 seconds to skip startup.nsh, any other key to continue.
Shell> FS0:

fs0:¥> CD EC_Update
fs0:¥EC_Update> Update.efi

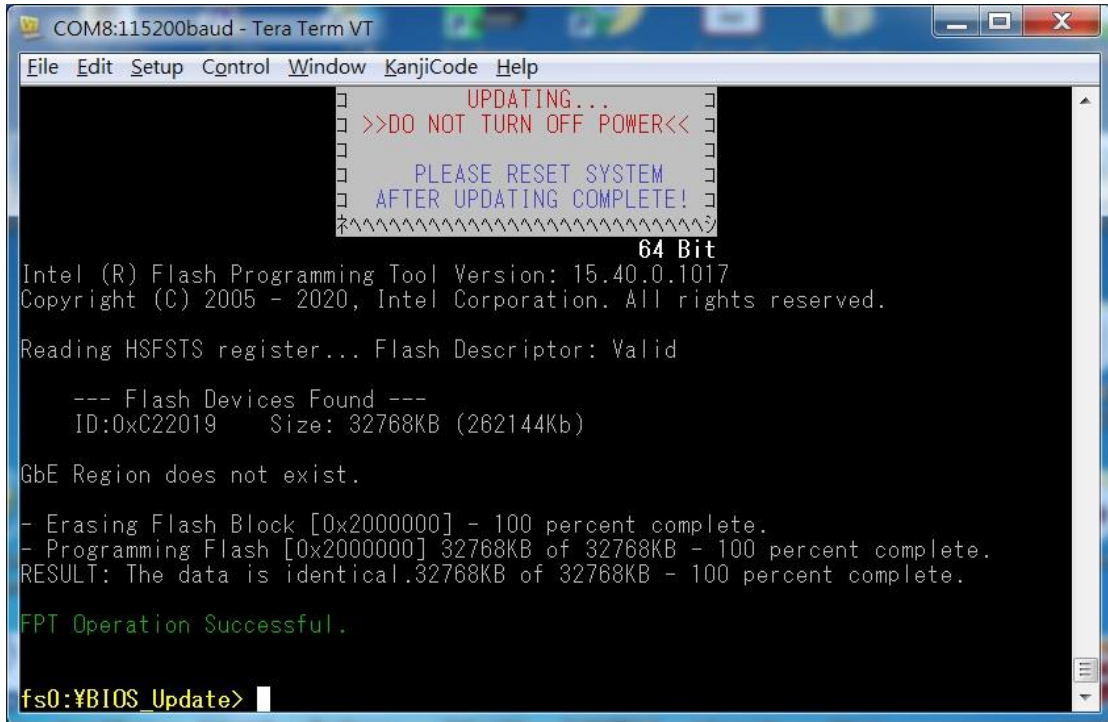
```

(EC File Update)

Step 5. The updating process will start and you can see the updating progress.

When you see the following pictures, which means the BIOS / EC update processes finished.

Please cut the AC power off and wait for 10 seconds before powering on.



```

COM8:115200baud - Tera Term VT
File Edit Setup Control Window KanjiCode Help

  UPDATING...
  >>DO NOT TURN OFF POWER<<
  PLEASE RESET SYSTEM
  AFTER UPDATING COMPLETE!
  ~~~~~
                                64 Bit
Intel (R) Flash Programming Tool Version: 15.40.0.1017
Copyright (C) 2005 - 2020, Intel Corporation. All rights reserved.

Reading HSFSTS register... Flash Descriptor: Valid

--- Flash Devices Found ---
ID:0xC22019   Size: 32768KB (262144Kb)

GbE Region does not exist.

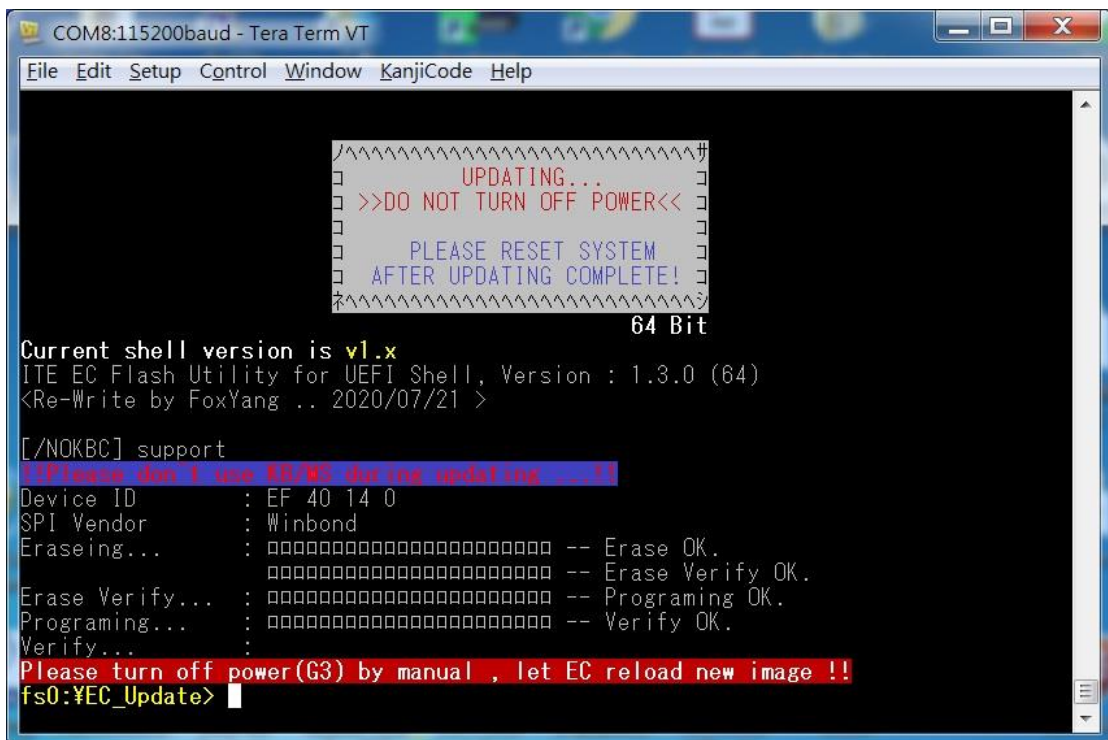
- Erasing Flash Block [0x20000000] - 100 percent complete.
- Programming Flash [0x20000000] 32768KB of 32768KB - 100 percent complete.
RESULT: The data is identical.32768KB of 32768KB - 100 percent complete.

FPT Operation Successful.

fs0:¥BIOS_Update>

```

(BIOS update finished)



```

COM8:115200baud - Tera Term VT
File Edit Setup Control Window KanjiCode Help

  UPDATING...
  >>DO NOT TURN OFF POWER<<
  PLEASE RESET SYSTEM
  AFTER UPDATING COMPLETE!
  ~~~~~
                                64 Bit
Current shell version is v1.x
ITE EC Flash Utility for UEFI Shell, Version : 1.3.0 (64)
<Re-Write by FoxYang .. 2020/07/21 >

[/NOKBC] support
Please don't use ER/WS during updating ....!!
Device ID       : EF 40 14 0
SPI Vendor      : Winbond
Erasing...      : ~~~~~ -- Erase OK.
                  ~~~~~ -- Erase Verify OK.
Erase Verify... : ~~~~~ -- Programing OK.
Programming...  : ~~~~~ -- Verify OK.
Verify...       : ~~~~~
Please turn off power(G3) by manual , let EC reload new image !!
fs0:¥EC_Update>

```

(EC update finished)

Chapter 7

Overview

- 7 System Resources
- 7.1 Intel® Alder/ Amston Lake SoC
- 7.2 Main Memory
- 7.3 Installing the Single Board Computer

7 System Resources

7.1 Intel® Alder Lake N/ Amston Lake SoC

Intel® Atom® Core™ i3-N305 1.80GHz

Intel® Atom® x7425E 1.5GHz

Intel® Atom® x7213E 1.7GHz

Intel® Atom® x7211E 1.0GHz

Intel® Atom® x7835RE 1.3GHz

Intel® Atom® x7433RE 1.5GHz

Intel® Atom® x7213RE 2.0GHz

Intel® Atom® x7211RE 1.0GHz

7.2 Main Memory

NANO-6064 provides 1 x 260-pin SO-DIMM sockets which supports DDR4 non-ECC memory. The maximum memory can be up to 16GB. Memory clock and related settings can be detected by BIOS via SPD interface.

Watch out the contact and lock integrity of memory module with socket, it will impact on the system reliability. Follow normal procedures to install memory module into memory socket. Before locking, make sure that all modules have been fully inserted into the card slots.

7.3 Installing the Single Board Computer

To install your NANO-6064 into standard chassis or proprietary

environment, please perform the following:

Step 1 : Check all jumpers setting on proper position

Step 2 : Install and configure memory module on right position

Step 3 : Place NANO-6064 into the dedicated position in the system

Step 4 : Attach cables to existing peripheral devices and secure it

WARNING

Please ensure that motherboard is properly inserted and fixed by mechanism.

Note:

Please refer to section 6.3 to install Graphic/LAN

7.3.1 Chipset Component Driver

The NANO-6064 build with Intel Atom® processor x7000E/x7000RE series and Intel® Core™ i3 N305. It's a new chipset that some old operating systems might not be able to recognize. To overcome this compatibility issue, for Windows Operating Systems such as Windows 8, please install its INF before any of other Drivers are installed. You can find very easily this chipset component driver in NANO-6064 CD-title

7.3.2 Chipset Component Driver

NANO-6064 has integrated Intel® Gen 12HD Graphics. Processor Graphics indicates graphics processing circuitry integrated into the processor, providing the graphics, compute, media, and display capabilities.

NANO-6064 supports HDMI, DP, LVDS display output. This combination makes NANO-6064 an excellent performance hardware.

Drivers Support

The driver supports Windows 10 IoT Enterprise LTSC 2021(64bit).

Chapter 8

Overview

- 8 Troubleshooting
- 8.1 Hardware Quick Installation
- 8.2 BIOS Setting
- 8.3 FAQ

8 Troubleshooting

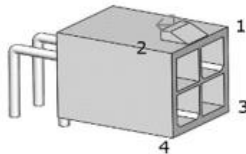
This chapter provides a few useful tips to quickly get NANO-6064 running with success. As basic hardware installation has been addressed in Chapter 2, this chapter will focus on system integration issues, in terms of BIOS setting, and OS diagnostics.

8.1 Hardware Quick Installation

ATX Power Setting

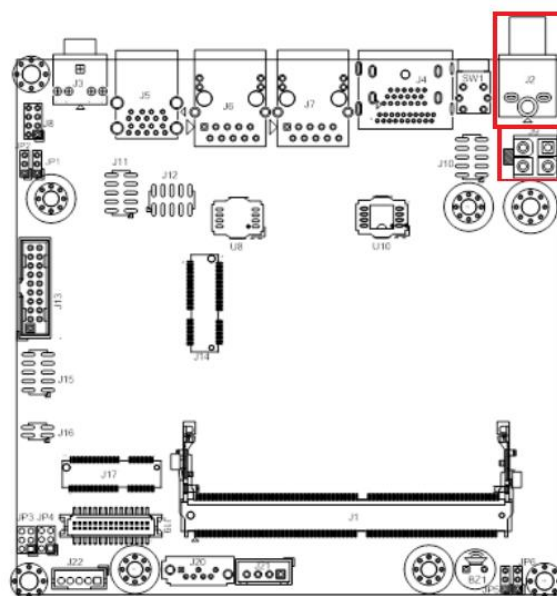
There are two methods to connect the power of NANO-6064 which are 12V DC Jack (J2) & 4 Pins 12V DC input (J9). It's able to be chosen either one for NANO-6064.

J9: ATX 4 Pin



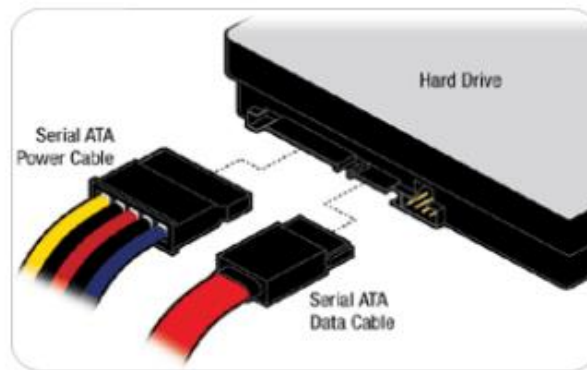
PIN No.	Signal Description
1	+12V
2	+12V
3	Ground
4	Ground

Connector

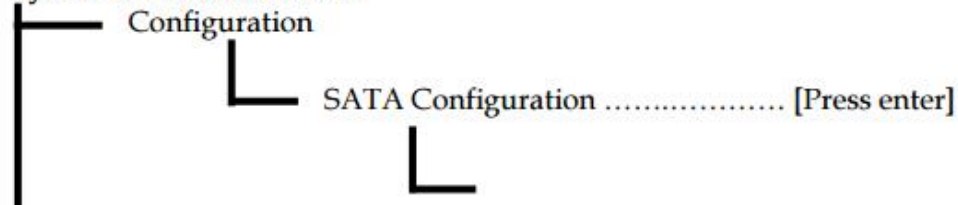


Serial ATA

Serial ATA Hard Disk Setting for SATA Speed Selection



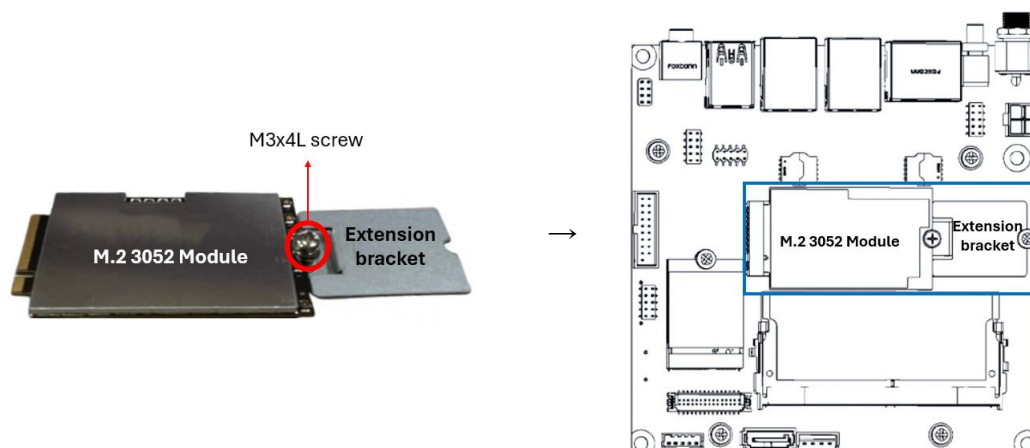
System BIOS Main Menu



SATA Speed Selection [Auto, Gen1, Gen2, Gen3]

Extension bracket

The NANO-6064 only has a boss-standoff for M.2 Key B slots at the 2280 position. To accommodate M.2 3052 modules, we've included an extension bracket. Please refer to the below image for installation instructions. Fasten with M3x4L screws.



8.2 BIOS Setting

It is assumed that users have correctly adopted modules and connected all the devices cables required before turning on ATX power.

260-pin DDR4 3200MT/sSO-DIMM Memory, keyboard, mouse, SATA hard disk, VGA connector, device power cables, ATX accessories are good examples that deserve attention. With no assurance of properly and correctly accommodating these modules and devices, it is very possible to encounter system failures that result in malfunction of any device.

To make sure that you have a successful start with NANO-6064, it is recommended, when going with the boot-up sequence, to hit “DEL” and “ESC” key and enter the BIOS setup menu to tune up a stable BIOS configuration so that you can wake up your system far well.

Loading the default optimal setting

When prompted with the main setup menu, please scroll down to “**RestoreDefaults**”, press “**Enter**” and select “**Yes**” to load default optimal BIOS setup. This will force your BIOS setting back to the initial factory configurations. It is recommended to do this so you can be sure the system is running with the BIOS setting that Portwell has highly endorsed. As a matter of fact, users can load the default BIOS setting at any time when system appears to be unstable in boot up sequence.

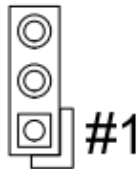
8.3 FAQ

Information & Support

Question: I forgot my password of system BIOS, what am I supposed to do?

Answer: You can switch off your power supply then find the JP6 on the NANO-6064 to set it from 1-2 short to 2-3 short and wait 5 seconds to clean your password.

JP6 : CMOS Clear



PIN No.	Signal Description
1-2 Short	Clear CMOS
2-3 Short	n/a

Question: How to update the BIOS file of NANO-6064?

Answer: 1. Please visit web site of Portwell download center as below hyperlink

http://www.portwell.com.tw/support/download_center.php

Registering an account in advance is a must. (The E-Mail box should be an existing Company email address that you check regularly.)

<http://www.portwell.com.tw/member/newmember.php>

2. Type in your Username and password and log in the download center.
3. Select “Search download” and type the keyword “NANO-6064”.
4. Find the “BIOS “page and download the ROM file and flash utility.
5. Unzip file to bootable USB flash drive which can boot to shell mode. Then execute the “update.efi ”. It will start to update BIOS.
6. When you see the “FPT Operation Passed” message, which means the BIOS update processes finished. Please cut the AC power off and wait for 10 seconds before powering on.

http://www.portwell.com.tw/support/download_center.php

If you have other additional technical information or request which is not covered in this manual, please fill in the technical request form as below hyperlink.

http://www.portwell.com.tw/support/problem_report.php

We will do our best to provide a suggestion or solution for you.

Thanks

Chapter 9

Overview

9 Portwell Software Service

9 Portwell Software Service

Portwell Evaluation Tool (PET)

The Portwell Evaluation Tool (PET) is an API which Portwell's customers can access the GPIO, I2C, SMBus, etc under Windows and Linux OS. For more information, please contact Portwell.

Portwell BIOS web Tool (PBT)

The Portwell BIOS web Tool (PBT) is a brand-new on-line utility which innovated by Portwell. PBT now is available for Portwell's premiere customers who are able to add customized BIOS logo and change BIOS default settings on American Megatrends (AMI) BIOS. Please contact Portwell for more information.

Portwell EC Auto Test Tool (PECAT)

The Portwell EC Auto Test Tool (PECAT) is a brand-new utility which innovated by Portwell. PECAT now is available for Portwell's premiere customers, who are able to Test Embedded Controller Function in UEFI Mode. Please contact Portwell for more information.



Please verify specifications before quoting. This guide is intended for reference purposes only. All product specifications are subject to change without notice. No part of this publication may be reproduced in any form or by any means, such as electronically, by photocopying, recording, or otherwise, without prior written permission from the publisher. All brand and product names are trademarks or registered trademarks of their respective companies



Portwell, Inc. Headquarters

No. 242, Bo'AI St., Shu-Lin Dist,
New Taipei City 238, Taiwan
Tel: +886-2-7731-8888
Fax: +886-2-7731-9888
E-mail: info@portwell.com.tw
www.portwell.com.tw

American Portwell

(Fremont, CA)
Tel: +1-510-403-3399
E-mail: info@portwell.com
www.portwell.com

Portwell UK Ltd.

Tel: +44(0)1235-750-760
E-mail: info@portwell.eu
www.portwell.eu

Portwell Japan, Inc.

(Tokyo)
Tel: +81-3-6902-9225
E-mail: info@portwell.co.jp
www.portwell.co.jp

Portwell Japan, Inc.

(Osaka)
Tel: +81-6-4807-7721
E-mail: info@portwell.co.jp
www.portwell.co.jp

European Portwell

Tel: +31-252-620790
E-mail: info@portwell.eu
www.portwell.eu

KIOSK Embedded Systems GmbH

Tel: +49-8152-3962-500
E-mail: info@portwell.eu
www.portwell.de

Shanghai Portwell

Tel: +86-21-5771-2505
E-mail: info@portwell.com.cn
www.portwell.com.cn

Portwell Korea, Inc.

Tel: +82-31-450-3043
E-mail: info@portwell.co.kr
www.portwell.co.kr

Portwell India Technology Private Limited

Tel: +91-80-4168-4255
E-mail: enquiry@portwell.in
www.portwell.in