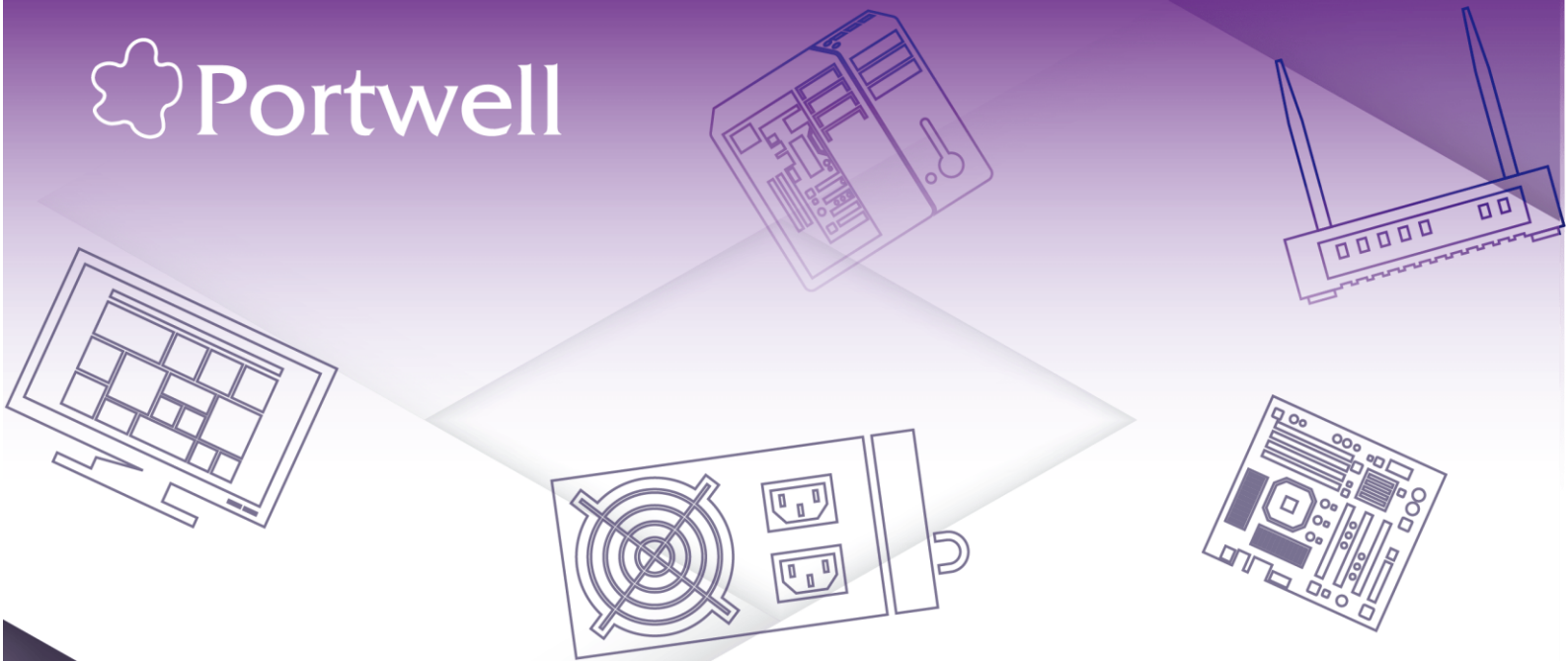
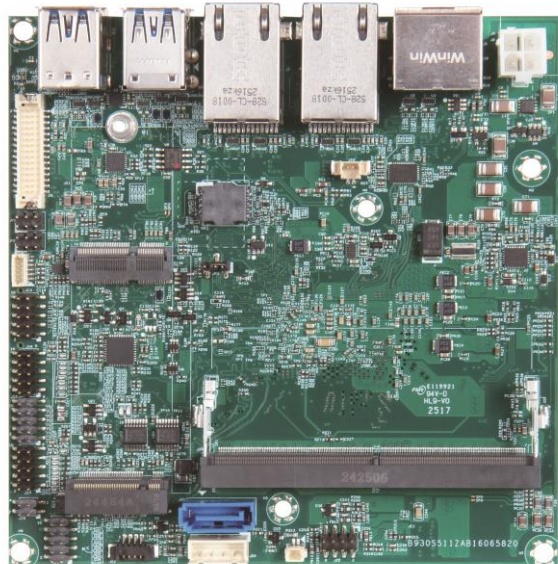




NANO-6065 Series

NANO-ITX Embedded Board

User Manual

Version R1.0

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Revision History

R1.0	Official Released R1.0

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Chapter 1

Overview

1 Introduction

1. Introduction

The NANO-6065 series utilizes the NANO-ITX form factor and is powered by the Intel Core 3 processor N355/Intel processor N150/Intel Atom x7835RE. It supports one DDR5 SO-DIMM socket with up to 16GB capacity, one M.2 E key socket, and one M.2 B key socket. The integrated Intel Gen 12 Graphics with up to 32 EUs support triple independent displays via HDMI, Type C (support DP 1.4) and LVDS*. Additionally, it features Dual 2.5GbE port, one SD socket, and four USB 3.2 Gen2 ports.

The NANO-6065 series is versatile, compact and powerful, making it ideal for diverse applications such as industrial automation, robotic control systems, automated test equipment, medical equipment, gateways, digital signage, and more.

Chapter 2

Overview

- 2 Specifications
- 2.1 Supported Operating Systems
- 2.2 Mechanical Dimension
- 2.3 Power Consumption

2. Specifications

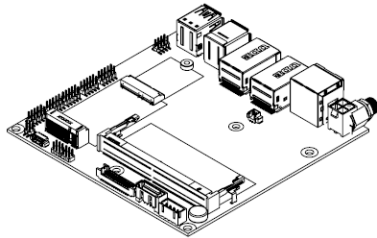
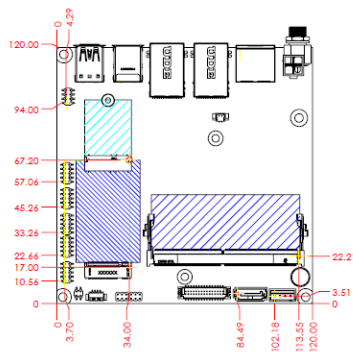
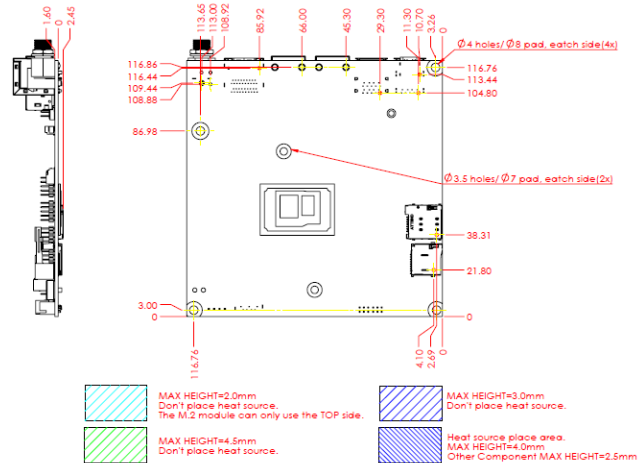
Main Processor	Intel Core 3 processor N355 Intel processor N150 Intel Atom x7835RE
System BIOS	AMI UEFI BIOS
Main Memory	1x non-ECC DDR5 4800MT/s SO-DIMM up to 16GB 1DPC, 1-channel Support In-Band ECC
Graphics	Intel Graphics Gen12 with up to 32 EUs HDMI: 2x HDMI port on rear I/O (HDMI 2.0b, 4096 x 2160 @ 60Hz) DP: Type C port on rear I/O (DP 1.4, 4096 x 2304 @ 60Hz) *LVDS: 1x LVDS on board connector (Dual channel, 24bit, 1920 x 1200 @60Hz) (*Optional, available upon request with MOQ requirement)
Expansion Interface	1x M.2 E key2230 (PCIe / USB) 1x M.2 B Key 3052/2280 (SATA / PCIe / USB)
Storage Interface	1x SATA III port (SATA 6Gb/s) 1xMicro SD socket
Input/Output	2x RS-232/422/485 on-board pin header (selectable via BIOS) 3x USB 3.2 Gen2 Type A on rear I/O 1x USB 3.2 Gen1 Type C on rear I/O Audio Interface: on-board pin header (Line-in, Line-out, Mic-in) 1x Nano SIM socket
Ethernet	2x 2.5 GbE (Intel I226) with RJ45 connector on rear I/O
High Drive GPIO	1x pin-header for GPIO(8bit)
Mechanical and environmental specifications	Board size: 120mm x 120 mm (4.72" x 4.72") Operating temperature: 0 ~ 60° C (Twin Lake SKU) -40 ~ 85° C (Amston Lake SKU) Storage temperature: -40 ~ 85° C Humidity: 5 ~ 95% non-condensing Power supply voltage: 12 ~24 V DC in
Certification	CE/FCC/UKCA

2.1 Supported Operating Systems

The NANO-6065 supports the following operating systems.

	Windows IoT Enterprise	Ubuntu	Red Hat (RHEL)
Twin Lake	Windows 11 LTSC (24H2)	24.04	9.6/10.0
Amston Lake	Windows 10 LTSC (21H2) Windows 11 LTSC (24H2)	22.04/24.04	NA

2.2 Mechanical Dimensions



2.3 Power Consumption

Test Configuration	
CPU Type	Intel®Core™ 3 N355 1.90GHz L3:6MB
SBC BIOS	Potrwell Inc.NANO-6065 BIOS Rev.:0.0.4 (06122025)
Memory	Innodisk 16GB DDR5 4800 SODIMM(SEC 149 K4RAH08 6VB BCQK*8)*1
Graphic Card	Onboard Intel®Graphics
Graphic Driver	Intel®Graphics,version:32.0.101.6314
LAN Card #1	Onboard Intel®Ethernet Controller I226-V
LAN Driver #1	Intel® Ethernet Controller I226-V,Version:1.1.4.42
LAN Card #2	Onboard Intel®Ethernet Controller I226-V #2
LAN Driver #2	Intel® Ethernet Controller I226-V,Version:1.1.4.42
Audio Card	Onboard High Definition Audio Device
Audio Driver	High Definition Audio Device,Version:10.0.26100.3624
Chip Driver	Onboard Intel® Chipset Device Software,Version:10.1.19899.8597
USB 2.0 Driver	USB Composite Device,Driver Version:10.26100.3912
USB 3.0 Driver	Intel® USB 3.20 eXtensible Host Controller – 1.20 (Microsoft),Version:10.0.26100.4202
OS Edition	Windows 11Pro (24H2)
Hard Drive	Crucal BX500 2.5 SSD (CT500BX500SSD1)
Power Supply	Switching Power Adapter (FSP120-AHAN1)

Power consumption(12V)

Item	Power On	Full Loading 10Min
CPU DC in (+12V)	1.74A	2.46A
USB 3.2 Gen1 Port J3_up	<u>4.82</u> V/ <u>0.93</u> A	
USB 3.2 Gen1 Port J4_up	<u>4.86</u> V/ <u>0.92</u> A	
USB 3.2 Gen1 Port J4_down	<u>4.88</u> V/ <u>0.93</u> A	
Full USB port Loading Test (x2)	USB 3.2 Gen1 Port J4_up : <u>4.84</u> V/ <u>0.90</u> mA	

2.4 Environmental Specifications

Storage Temperature: -40~85° C

Operation Temperature: 0~60° C (Twin Lake SKU)、-40~85° C (Amston Lake SKU)

Storage Humidity: 5~95%, non-condensing

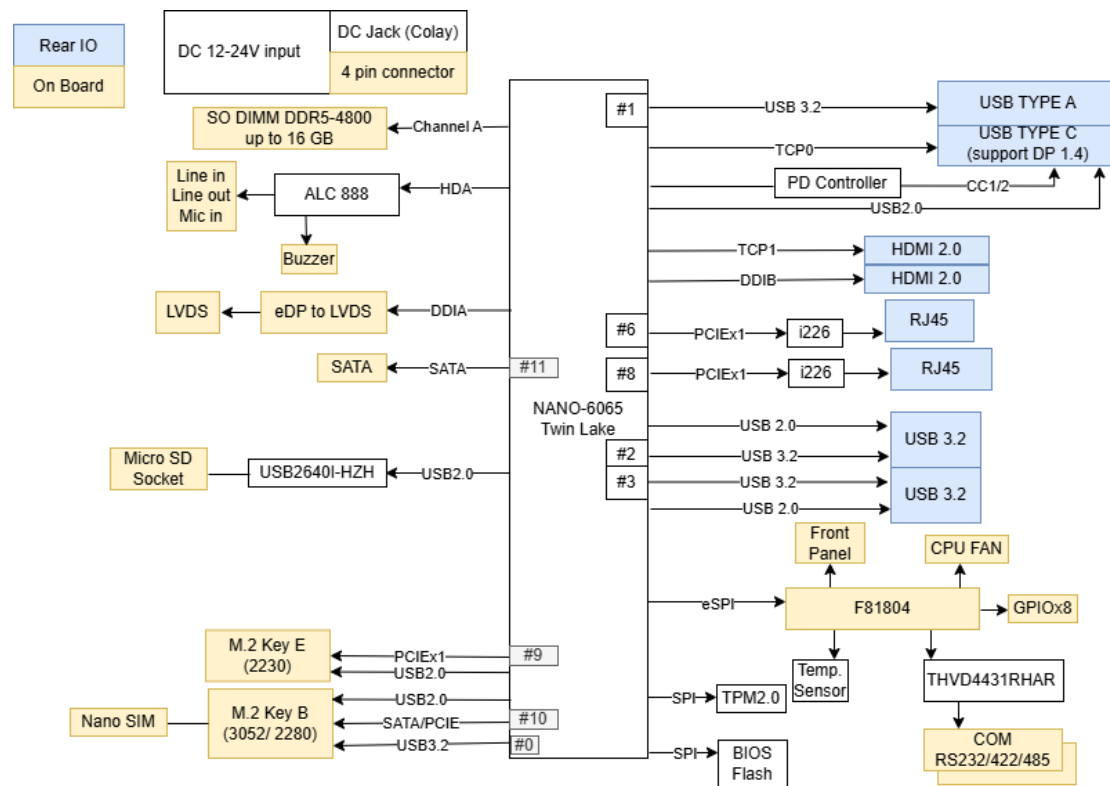
Operation Humidity: 5~95%, non-condensing

Chapter 3

Overview

3 Block Diagram

3 Block Diagram



Chapter 4

Overview

- 4 Hardware Configuration
- 4.1 Jumpers and Connectors
- 4.2 Jumper Settings

4 Hardware Configuration

4.1 Jumpers and Connectors

Figure 1, NANO-6065 Top View

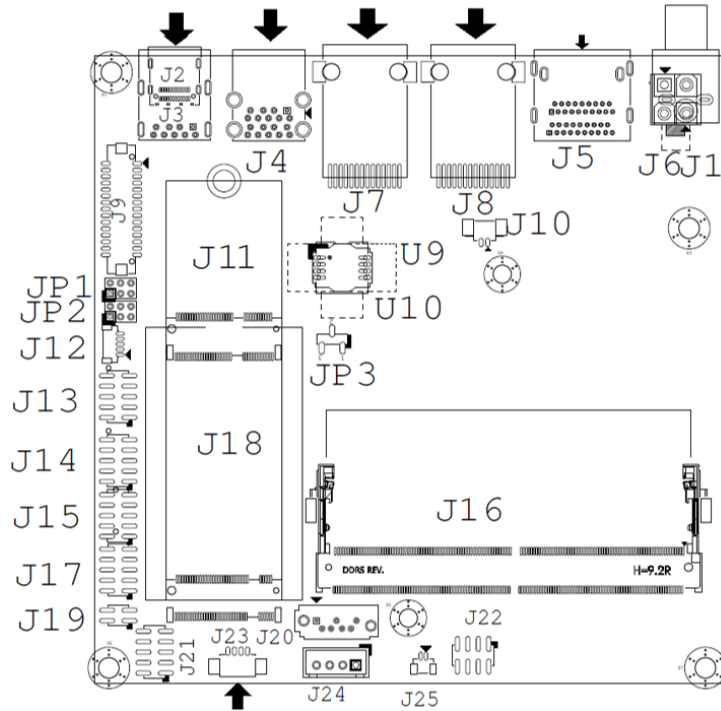
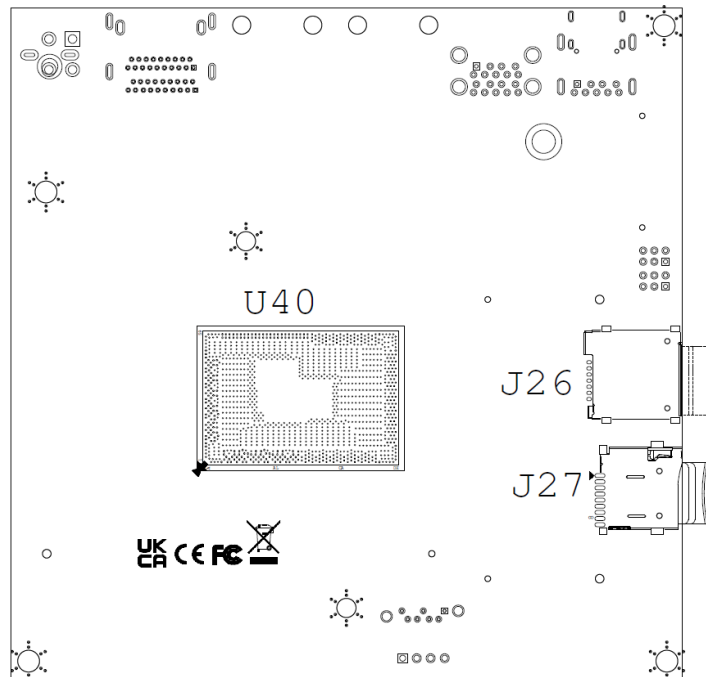


Figure 2, NANO-6065 Bottom View



4.2 Jumper Settings

For users to customize NANO-6065's features. In the following sections, short means covering a jumper cap over jumper pins; Open or N/C (Not Connected) means removing a jumper cap from jumper pins. Users can refer to Figure 1 for the Jumper allocations.

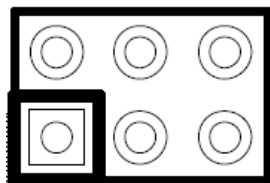
Jumper Table

The jumper settings are schematically depicted in this manual as follows:

Jump Function List:

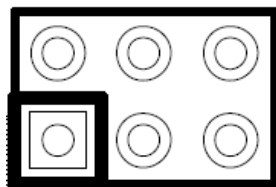
Header	Function	Remark
JP1	LVDS Power	
JP2	LVDS Backlight Enable Power	
JP3	ATX/AT mode Select	

JP1: LVDS Power



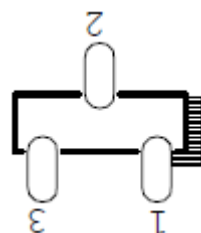
PIN No.	Signal Description
1-3 ★	LVDS_channel_PWR use +3.3V.
4-3	LVDS_channel_PWR use +12V.
5-3	LVDS_channel_PWR use +5V.

JP2: LVDS Backlight Enable Power



PIN No.	Signal Description
1-3, 2-4 ★	+5V, Active High
1-3, 4-6	+12V, Active High
3-5, 2-4	+5V, Active Low
3-5, 4-6	+12V, Active Low

JP3: ATX/AT mode Select



PIN No.	Signal Description
1-2 ★	ATX mode
2-3	AT mode

4.3 Connector Settings

Users can refer to Figure 1 & 2 for the connector allocations.

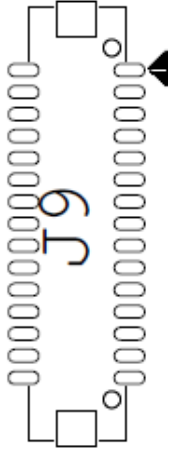
Connector Function List:

Jump	Function	Remark
J1	DC Jack	Optional, available upon request with MOQ requirement
J2	USB Type-C	
J3	USB Type-A	
J4	USB Type-A x2	
J5	HDMI *2	
J6	ATX Power 4P	
J7	RJ45	
J8	RJ45	
J9	LVDS Connector	Optional, available upon request with MOQ requirement
J10	Battery Connector	
J11	M.2 Key-E	
J12	LVDS Backlight Control	Optional, available upon request with MOQ requirement
J13	Debug Port (80 Port)	
J14	RS232/422/485 Port-1	
J15	General-purpose Input/Output	
J16	DDR5 SO-DIMM	
J17	RS232/422/485 Port-2	
J18	M.2 Key-B	
J19	Wireless Wide Area Network Card Select	
J20	SATA Connector	
J21	Front Pin	
J22	AUDIO Pin	
J23	Smart FAN	
J24	SATA Power	
J25	Buzzer	
J26	Nano SIM Socket	
J27	Micro SD Card Slot	

J6: ATX 4 Pin

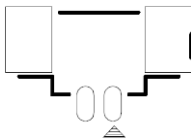
PIN No.	Signal Description
1	+12V
2	+12V
3	Ground
4	Ground

J9: LVDS Connector



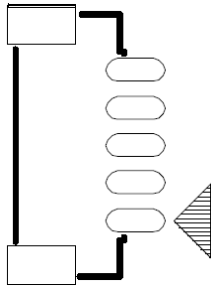
PIN No.	Signal Description	PIN No.	Signal Description
2	VDD(See JP1)	1	VDD (See JP1)
4	LVDS_CHA_TX_N_0	3	LVDS_CHA_TX_P_0
6	LVDS_CHA_TX_N_1	5	LVDS_CHA_TX_P_1
8	LVDS_CHA_TX_N_2	7	LVDS_CHA_TX_P_2
10	LVDS_CHA_TX_N_3	9	LVDS_CHA_TX_P_3
12	LVDS_CHA_CLK_N	11	LVDS_CHA_CLK_P
14	LVDS_DDC_DATA	13	LVDS_DDC_CLK
16	GND	15	GND
18	LVDS_CHB_TX_N_0	17	LVDS_CHB_TX_P_0
20	LVDS_CHB_TX_N_1	19	LVDS_CHB_TX_P_1
22	LVDS_CHB_TX_N_2	21	LVDS_CHB_TX_P_2
24	LVDS_CHB_TX_N_3	23	LVDS_CHB_TX_P_3
26	LVDS_CHB_CLK_N	25	LVDS_CHB_CLK_P
28	N/C	27	N/C
30	GND	29	GND

J10: Battery Connector



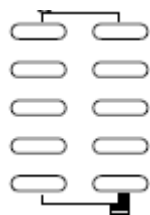
PIN No.	Signal Description
1	Positive(+)
2	Negative(-)

J12: Backlight Connector



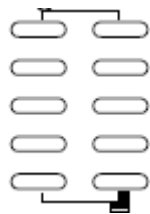
PIN No.	Signal Description
1	+5V
2	EDP_BKLCTRL
3	+12V
4	GND
5	BL_ENABLE

J14 : RS232/422/485 Port-1



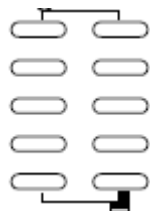
PIN No.	Signal Description	PIN No.	Signal Description
1	DCD#/DT-	2	RXD#/DT+
3	TXD#/422R+	4	DTR#/422R-
5	GND	6	DSR#
7	RTS#	8	CTS#
9	RI#	10	N/A

J15: General Purpose I/O Connector



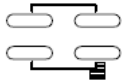
PIN No.	Signal Description	PIN No.	Signal Description
1	GPO0	2	GPI0
3	GPO1	4	GPI1
5	GPO2	6	GPI2
7	GPO3	8	GPI3
9	GND	10	+3.3V

J17: RS232/422/485 Port-2



PIN No.	Signal Description	PIN No.	Signal Description
1	DCD#/DT-	2	RXD#/DT+
3	TXD#/422R+	4	DTR#/422R-
5	GND	6	DSR#
7	RTS#	8	CTS#
9	RI#	10	N/A

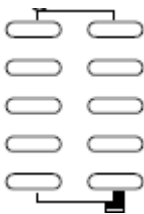
J19: Wireless Wide Area Network Card Select



PIN No.	Signal Description	PIN No.	Signal Description
1	Pull-Up(+5V)	2	GND
3	Pull-Up(+5V)	4	GND

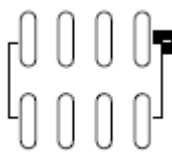
Pin Short	Description
1-2, 3-4	M.2 Spec. Pin out
3-4	Thales 5G
1-2	Sierra 4G
N/C ★	Sierra 5G

J21: Front Panel Pin HDR



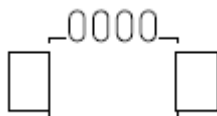
PIN No.	Signal Description	PIN No.	Signal Description
1	GND	2	N/A
3	PowerLED+	4	PowerLED-
5	SATALED+	6	SATALED-
7	Reset+	8	Reset-
9	PowerBTN-	10	PowerBTN+

J22: Audio Pin



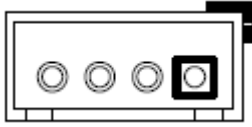
PIN No.	Signal Description	PIN No.	Signal Description
1	MIC-L	2	LINEIN-L
3	GND	4	LINEIN-R
5	LINEOUT-L	6	GND
7	LINEOUT-R	8	MIC-R

J23: Smart Fan



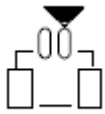
PIN No.	Signal Description
1	GND
2	+12V
3	TACHIN
4	PWM

J24: SATA Power Connector



PIN No.	Signal Description
1	+12V
2	GND
3	GND
4	+5V

J25: Buzzer



PIN No.	Signal Description	PIN No.	Signal Description
1	Positive(+)	2	Negative(-)

Chapter 5

Overview

- 5 Sample Code
- 5.1 Watch Dog Timer
- 5.2 Signal GPIO Signal

5 Sample Code

5.1 Watch Dog Timer

```
//F81804 WDT Sample Code
#define SIO_Port_Index      0x2E
#define SIO_Port_Data      0x2F
#define WDT_LDN            0x07
#define WDT_Config_offset  0xF5
#define WDT_Time_offset    0xF6
#define Time_Unit          0x00    //Time unit, 0=1 second, 1=60 second
#define Time                0x05    //Time, 5 second for example.
```

```
void Enter_F81804_SIO() {
    IoWrite8(SIO_Port_Index, 0x87);
    IoWrite8(SIO_Port_Index, 0x87);
    //Enter F81804 SIO
}
```

```
void Set_WDT_LDN() {
    IoWrite8(SIO_Port_Index, 0x07);
    IoWrite8(SIO_Port_Data, WDT_LDN);
}
```

```
void Set_Register(UINT8 offset, UINT8 And_Value, UINT8 OR_value) {
    UINT8 Temp;
    IoWrite8(SIO_Port_Index, offset);
    Temp=(IoRead8(SIO_Port_Data) & And_Value) | OR_Value;
    IoWrite8(SIO_Port_Data, Temp);
}
```

```
Byte Get_Register(UINT8 offset) {
```

```

    UINT8 Temp;
    IoWrite8(SIO_Port_Index, offset);
    Temp=IoRead8(SIO_Port_Data);
    return Temp;
}

void main()
{
    UINT8 Count_Time;

    Enter_F81804_SIO();
    Set_WDT_LDN();
    Set_Register(WDT_Config_offset,0xBF,0x40);          //Bit6:
    WDTMOUT_STS, Write 1 to clear Watchdog timeout event.
    Set_Register(WDT_Config_offset,0xF7,(Time_Unit<3)); //Bit3:
    Set Time Unit, 0=1 second, 1=60 second
    Set_Register(WDT_Time_offset,0x00,Time);           //Set Time.
    Set_Register(WDT_Config_offset,0xDF,0x20);         //Bit5: 0=Disable
    WDT , 1=Enable WDT.
    Count_Time=Get_Register(WDT_Time_offset);          //Read watchdog
    timer.
}

```

5.2 Signal GPIO Signal

```

//F81804 GPIO Sample Code
#define SIO_Port_Index  0x2E
#define SIO_Port_Data   0x2F
#define GPIO_LDN        0x06
#define GPIO_IOSpace    0x0A00

#define GP00_Output     0x00 //GP00 Output Mode,  0:Output    Low,
                          1:Output High

```

```
#Define GPO1_Output    0x00 //GPO1 Output Mode,    0:Output    Low,
                        1:Output High
#Define GPO2_Output    0x00 //GPO2 Output Mode,    0:Output    Low,
                        1:Output High
#Define GPO3_Output    0x00 //GPO3 Output Mode,    0:Output    Low,
                        1:Output High
#Define GPIO_Offset 0x06 //GPIO offset
#Define GPI1_Offset 0x07 //GPI1 offset
#Define GPI3_Offset 0x03 //GPI3 offset
```

```
void Enter_F81804_SIO() {
    IoWrite8(SIO_Port_Index, 0x87);
    IoWrite8(SIO_Port_Index, 0x87);
    //Enter F81804 SIO
}
```

```
void Set_GPIO_LDN() {
    IoWrite8(SIO_Port_Index, 0x07);
    IoWrite8(SIO_Port_Data, GPIO_LDN);
}
```

```
void Set_Register(UINT8 offset, UINT8 And_Value, UINT8 OR_value) {
    UINT8 Temp;
    IoWrite8(SIO_Port_Index, offset);
    Temp=(IoRead8(SIO_Port_Data) & And_Value) | OR_Value;
    IoWrite8(SIO_Port_Data, Temp);
}
```

```
Byte Get_Register(UINT8 offset, UINT8 And_Value) {
    UINT8 Temp;
    IoWrite8(SIO_Port_Index, offset);
    Temp=IoRead8(SIO_Port_Data) & And_Value;
    return Temp;
}
```

```
}

void main()
{
    UINT8 GPIO0;
    UINT8 GPIO1;
    UINT8 GPIO2;
    UINT8 GPIO3;

    Enter_F81804_SIO();
    Set_GPIO_LDN();

    //GPO Output and setting
    //GPO0 Setting
    Set_Register(0x99, 0xFB, (GPO0_Output<<2)); //Bit2: GPO0 status, 0:
Low 1: High

    //GPO1 Setting
    Set_Register(0x99, 0xF7, (GPO1_Output<<3)); //Bit3: GPO1 status, 0:
Low 1: High

    //GPO2 Setting
    Set_Register(0x99, 0xEF, (GPO2_Output<<4)); //Bit4: GPO2 status, 0:
Low 1: High

    //GPO3 Setting
    Set_Register(0x99, 0x7F, (GPO3_Output<<7)); //Bit7: GPO3 status, 0:
Low 1: High

    //GPI Input and get status
    GPIO0= IoRead8(GPIO_IOSpace+GPIO_Offset); //Bit0: GPIO status, 0:
Low 1: High
```

```
GPI1= IoRead8(GPIO_IOSpace+GPI1_Offset); //Bit6: GPI1 status, 0:  
Low 1: High
```

```
GPI2= Get_Register(0x9A,0x02);           //Bit1: GPI2 status, 0: Low  
1: High
```

```
GPI3= IoRead8(GPIO_IOSpace+GPI3_Offset); //Bit0: GPI3 status, 0:  
Low 1: High  
}
```

Chapter 6

Overview

- 6 BIOS Setup Items
- 6.1 Entering Setup -- Launch System Setup
- 6.2 Main
- 6.3 Configuration

6 BIOS Setup Items

NANO-6065 is equipped with the AMI BIOS stored in Flash ROM. The BIOS has a built-in Setup program that allows users to modify the basic system configuration easily. This type of information is stored in SPI Flash so that it is retained during power-off periods. When the system is turned on, NANO-6065 communicates with peripheral devices and checks its hardware resources against the configuration information stored in the CMOS memory. If any error is detected, or the CMOS parameters need to be initially defined, the diagnostic program will prompt the user to enter the SETUP program. Some errors are significant enough to abort the start up.

6.1 Entering Setup -- Launch System Setup

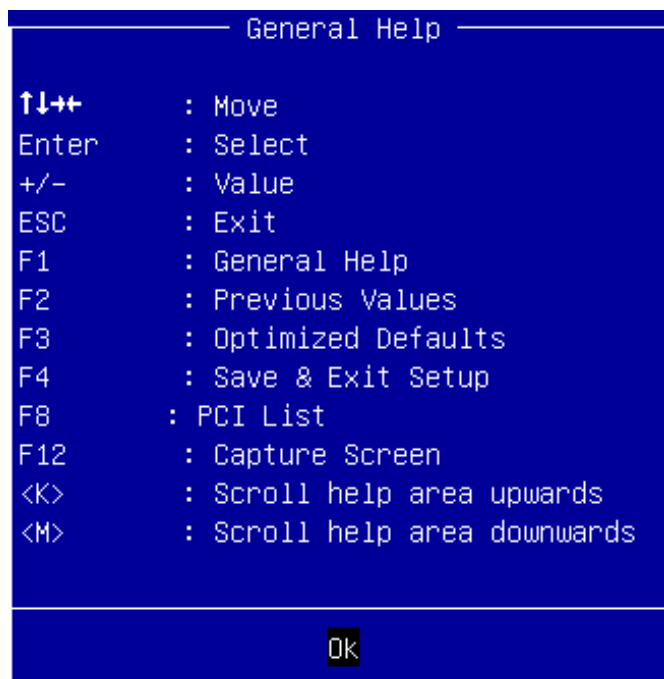
Power on the computer and the system will start POST (Power On Self-Test) process. When the message below appears on the screen, press key will enter BIOS setup screen.

Press to enter SETUP

If the message disappears before responding and still wish to enter Setup, please restart the system by turning it OFF and On or pressing the RESET button. It can be also restarted by pressing <Ctrl>, <Alt>, and <Delete> keys on keyboard simultaneously.

Press <F1> to Run General Help or Resume

The BIOS setup program provides a General Help screen. The menu can be easily called up from any menu by pressing <F1>. The Help screen lists all the possible keys to use and the selections for the highlighted item. Press <Esc> to exit the Help screen.



6.2 Main

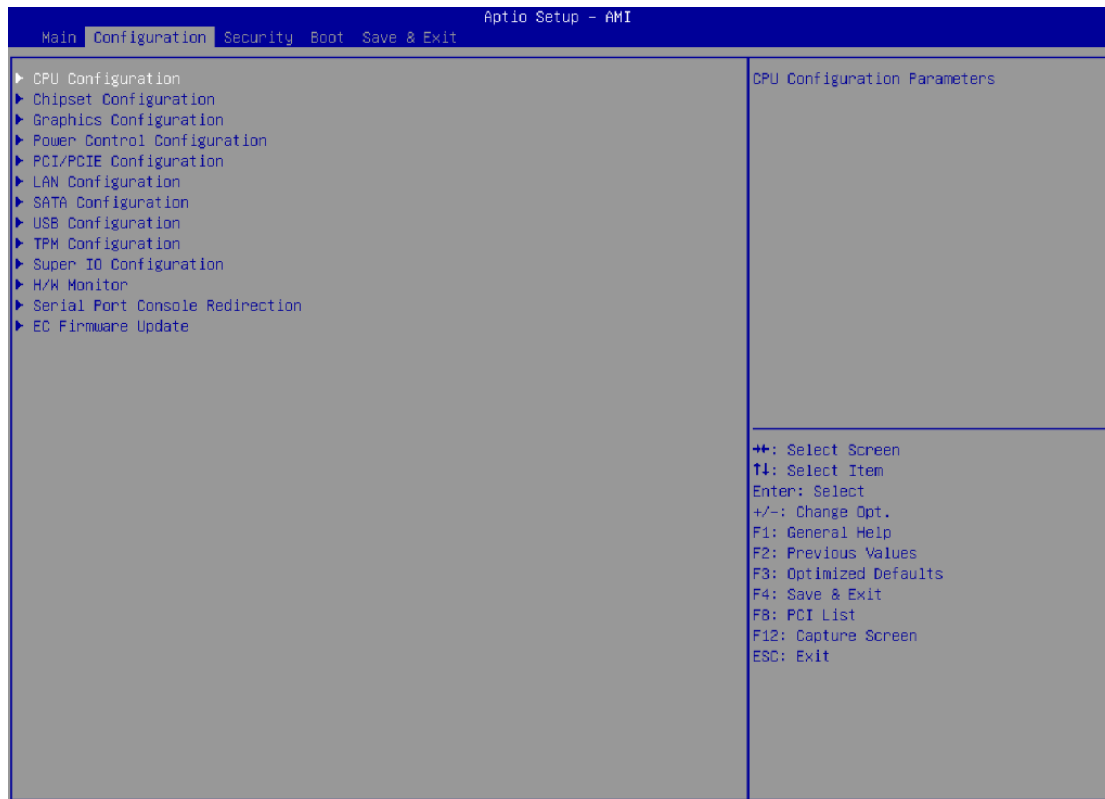


Feature	Description	Options
System Date	The date format is <Day>, <Month><Date><Year>. Use [+] or [-] to configure system Date.	
System Time	The time format is <Hour><Minute><Second>. Use [+] or [-] to configure system Time.	

Detailed System Information

Main	
Aptio Setup - AMI	
FSP Information	
FSP version	0C.02.81.70
RC version	0C.00.81.70
Build Date	08:27 07/25/2022
FSP Mode	Dispatch Mode
Board Information	
Board Name	NANO-6064
Processor Information	
Name	AlderLake ULX
Type	Intel(R) Core(TM) i3-N305
Speed	1800 MHz
ID	0xB06E0
Stepping	A0
Package	Not Implemented Yet
Number of Efficient-cores	8Core(s) / 8Thread(s)
Microcode Revision	B
GT Info	0x46D0
eDRAM Size	N/A
IGFX GOP Version	
IGFX GOP Version	21.0.1056
Memory RC Version	0.0.4.33
Total Memory	8192 MB
Memory Frequency	2400 MHz
MC 0 Ch 0 DIMM 0	Populated & Enabled
Size	8192 MB (DDR4)
PCH Information	
Name	PCH-N
Stepping	A0
ChipsetInit Base Revision	2
ChipsetInit OEM Revision	0
Package	Not Implemented Yet
TXT Capability of Platform/PCH	Unsupported
Production Type	Production
Dual Output Fast Read support	
Dual Output Fast Read support	Supported
Read ID/Status Clock Freq	50 MHz
Write and Erase Clock Freq	50 MHz
Fast Read Clock Freq	50 MHz
Fast Read support	Supported
Number of Components	1 Component
SPI Component 0 Density	32 MB
eSPI Flash Sharing Mode	
eSPI Flash Sharing Mode	G3
EC PECI Mode	Legacy PECI mode
ME FW Version	16.50.0.1215
ME Firmware SKU	Consumer SKU
PMC FW Version	160.50.0.1008

6.3 Configuration



6.3.1 CPU Configuration

Configuration Aptio Setup - AMI		
CPU Configuration		
Type	Intel(R) Core(TM) i3-N305	Number of E-cores to enable in each processor package. Note: Number of Cores and E-cores are looked at together. When both are {0,0}, Pcode will enable all cores.
ID	0x806E0	
Speed	1800 MHz	
L1 Data Cache	32 KB x 8	
L1 Instruction Cache	64 KB x 8	
L2 Cache	2048 KB x 2	
L3 Cache	6 MB	
VMX	Supported	
SMX/TXT	Not Supported	
Active Efficient-cores	[All]	
Boot performance mode	[Turbo Performance]	++: Select Screen T1: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit F8: PCI List F12: Capture Screen ESC: Exit
Intel (VMX) Virtualization Technology	[Enabled]	
Intel(R) SpeedStep(tm)	[Enabled]	
Intel(R) Speed Shift Technology	[Enabled]	
Turbo Mode	[Enabled]	
C states	[Enabled]	
Enhanced C-states	[Enabled]	
C-State Auto Demotion	[C1]	
C-State Un-demotion	[C1]	
Package C-State Demotion	[Enabled]	
Package C-State Un-demotion	[Enabled]	
CState Pre-Wake	[Enabled]	
ID MWAIT Redirection	[Disabled]	
Package C State Limit	[Auto]	

Feature	Description	Options
Active Efficient-Cores	Number of E-cores to enable in each processor package. Note: Number of Cores and E-cores are looked at together, When both are {0,0}, Pcode will enable all cores.	★All, 1, 2, 3, 4, 5, 6, 7
Boot performance mode	Select the performance state that the BIOS will set starting from reset vector	★Turbo Performance Max Battery Max Non-Turbo Performance
Intel (VMX) Virtualization Technology	When enabled, a VMM can utilize the additional hardware capabilities provided by Vander pool Technology.	Disabled, ★Enabled
Intel®Speed Step™	Allows more than two frequency ranges to be supported.	Disabled, ★Enabled

Intel® Speed Shift Technology	Enable/Disable Intel® Speed Shift Technology support. Enabling will expose the CPPC v2 interface to allow for hardware controlled P-states	Disabled, ★Enabled
Turbo Mode	Enable/Disable processor Turbo Mode (requires EMTTM enabled too). AUTO means enabled.	Disabled, ★Enabled
C states	Enable/disable CPU Power Management. Allows CPU to go to C states when it's not 100% utilized	Disabled, ★Enabled
Enhanced C-states	Enable/Disable C1E. When enabled, CPU will switch to minimum speed when all cores enter C-state	Disabled, ★Enabled
C-State Auto Demotion	Configure C-State Auto Demotion	Disable, ★C1
C-State Un-demotion	Configure C-State Un-demotion	Disable, ★C1
Package C State Demotion	Package C-State Demotion	Disabled, ★Enabled
Package C State Un-demotion	Package C-State Un-demotion	Disabled, ★Enabled
CState Pre-Wake	Disable – Sets bit 30 of POWER_CTL MSR(0x1FC) to 1 to disable the Cstate Pre-Wake	Disabled, ★Enabled
IO MWAIT Redirection	When set, will map IO_read instructions sent to IO registers PMG_IO_BASE_ADDRBASE+offset to MWAIT(offset)	★Disabled, Enabled
Package C State Limit	Maximum Package C State Limit Setting. CPU Default: Leaves to Factory default value. Auto: Initializes to deepest available Package C States Limit	C0/C1,C2,C3,C6,C7,C7S,C8,C9,C10,Cpu Default, ★Auto

6.3.2 Chipset Configuration



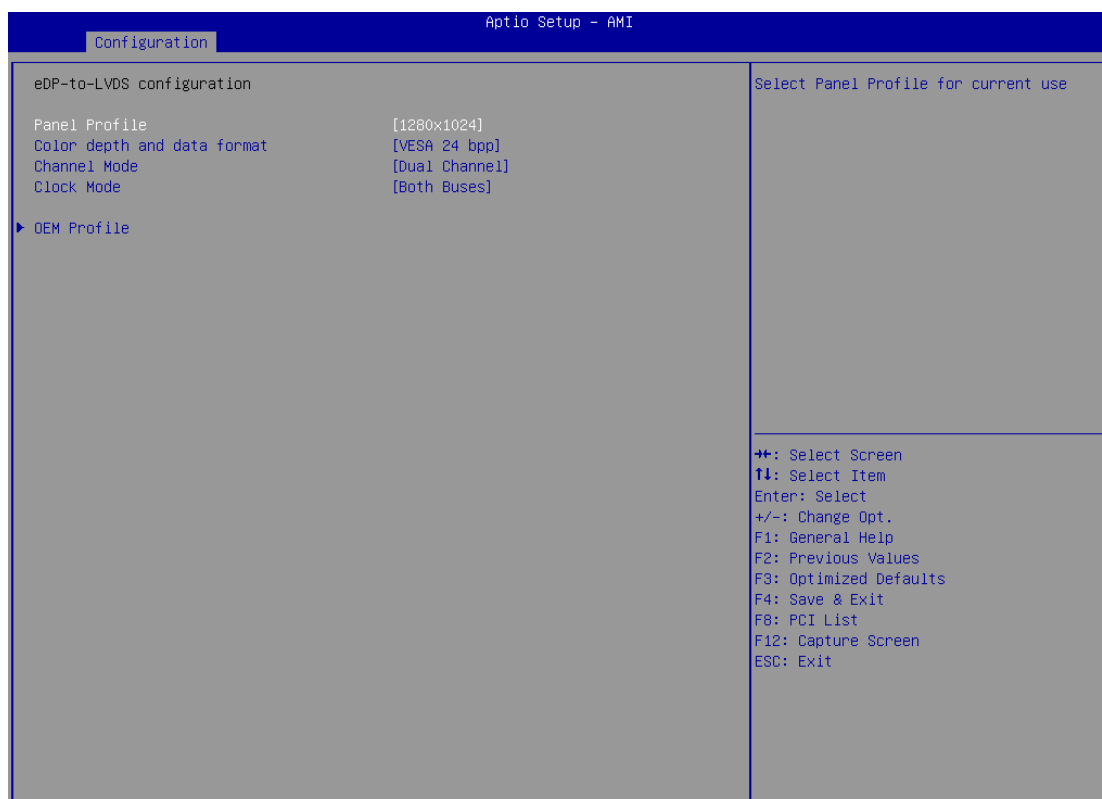
Feature	Description	Options
VT-d	VT-d Capability	★Enabled ,Disabled
Above 4GB MMIO BIOS assignment	Enable/Disable above 4GB Memory Mapped IO BIOS assignment	Enabled ,★Disabled
	This is enabled automatically when Aperture Size is set to 2048MB	
HD Audio	Control Detection of the HD-Audio device.	★Enabled ,Disabled
	Disabled = HDA will be unconditionally disabled	
	Enabled = HDA will be unconditionally enabled	
Port 80h Redirection	Control when the Port 80h cycles are sent.	★LPC Bus, PCIE Bus
Me FW Image Re-Flash	Enable/Disable Me FW Image Re-Flash function.	★Disabled, Enabled

6.3.3 Graphics Configuration



Feature	Description	Options
Primary Display	Select which of IGFX/PEG/PCI Graphics device should be Primary Display Or Select HG for Hybrid Gfx.	★Auto, IGFX, PEGSlot, PCH PCI
Internal Graphics	Keep IGFX enable based on the setup options.	★Auto, Disable, Enable
DVMT Pre-Allocated	Select DVMT 5.0 Pre-Allocated (Fixed) Graphics Memory size used by the Internal Graphics Device.	32M,64M, 96M, 128M, 160M, 12M, 16M,20M, 24M, 28M, 32M/F7,36M,40M,44M,48M,52M,56M, ★60M
DVMT Total Gfx Mem	Select DVMT5.0 Total Graphic Memory size used by the Internal Graphics Device	★256M, 128M, MAX
VBT Select	Select VBT for GOP Driver Select vbt to 'No LVDS' if no need LVDS	★Standard, No LVDS
eDP-to-LVDS configuration	eDP-to-LVDS(PTN3460)	

eDP-to-LVDS configuration



Feature	Description	Options
Panel Profile	Select Panel Profile for current use	640x480, 800x480, 800x600, 1024x768, 1280x800, ★1280x1024, 1366x768, 1440x900, 1920x1080, OEM Profile
Color depth and data format	Select Color depth and data format.	★VESA 24 bpp, JEIDA 24 bpp, VESA and JEIDA 18 bpp
Channel Mode	Select LVDS Channel Mode	Single Channel ★Dual Channel
Clock Mode	Select clock output for LVDS.	Even Bus, Odd Bus, ★Both Buses
OEM Profile	PANEL 1 Help	

OEM Profile: PANEL 1 Configuration

Configuration		Aptio Setup - AMI	
PANEL 1 Configuration Profile Name : empty Rename Profile Color depth and data format [VESA and JEIDA 18 bpp] Channel Mode [Single Channel] Clock Mode [Even Bus] Pixel Clock 0.000 Mhz 2500 H Active Pixels 0 640 H Blank Pixels 0 160 H Offset Pixels 0 16 H Width Pixels 0 96 V Active Lines 0 480 V Blank Lines 0 45 V Offset Lines 0 10 V Width Lines 0 2 H & V sync Signal Polarity [Postive]			
++: Select Screen ↑↓: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit F8: PCI List F12: Capture Screen ESC: Exit			

Feature	Description	Options
Rename Profile	Rename Profile name	
Color depth and data format	Select Color depth and data format.	VESA 24 bpp JEIDA 24 bpp ★VESA and JEIDA 18 bpp
Channel Mode	Select LVDS Channel Mode.	Dual channel ★Single channel
Clock Mode	Select Clock output for LVDS.	Both Buses, ★Even Bus, Odd Bus
Pixel Clock	Pixel Clock (10Khz)	★ 2500
H Active Pixels	H Active Pixels (Pixel)	★ 640
H Blank Pixels	H Blank Pixels (Pixel)	★ 160
H Offset Pixels	H Offset Pixels (Pixel)	★ 16
H Width Pixels	H Width Pixels (Pixel)	★ 96
V Active Lines	V Active Lines (Line)	★ 480
V Blank Lines	V Blank Lines (Line)	★ 45
V Offset Lines	V Offset Lines (Line)	★ 10
V Width Lines	V Width Lines (Line)	★ 2
H & V sync Signal Polarity	Flag: 0x1E Signal Polarity is Postive; 0x18 Signal Polarity is Non-Postive	★ Postive, Non-Postive

6.3.4 Power Control Configuration

Configuration Aptio Setup - AMI		
<div> <div>Power Control Configuration</div> <div> <div>Enable Hibernation</div> <div>ACPI Sleep State</div> <div>Restore AC Power Loss</div> </div> <div> <div>[Enabled]</div> <div>[S3 (Suspend to RAM)]</div> <div>[Power Off]</div> </div> <div> <div>Enables or Disables System ability to Hibernate (OS/S4 Sleep State). This option may not be effective with some operating systems.</div> <div> <div>→: Select Screen</div> <div>↑↓: Select Item</div> <div>Enter: Select</div> <div>+/-: Change Opt.</div> <div>F1: General Help</div> <div>F2: Previous Values</div> <div>F3: Optimized Defaults</div> <div>F4: Save & Exit</div> <div>F8: PCI List</div> <div>F12: Capture Screen</div> <div>ESC: Exit</div> </div> </div> </div>		
Feature	Description	Options
Enable Hibernation	Enables or Disables System ability to Hibernate (OS/S4 Sleep State). This option may not be effective with some operating systems.	★Enabled, Disabled
ACPI Sleep State	Select the highest ACPI sleep state the system will enter when the SUSPEND button is pressed.	★S3 (Suspend to RAM), Suspend Disabled
Restore AC Power Loss	Specify what state to go to when power is re-applied after a power failure (G3 state)	★Power Off, Power On, Last State

6.3.5 PCI/PCIE Configuration

Configuration Aptio Setup - AMI

PCI/PCIE Configuration

POH PCI Express Root Port

- ▶ PCI Express Root Port 7
- ▶ PCI Express Root Port 9
- ▶ PCI Express Root Port 10

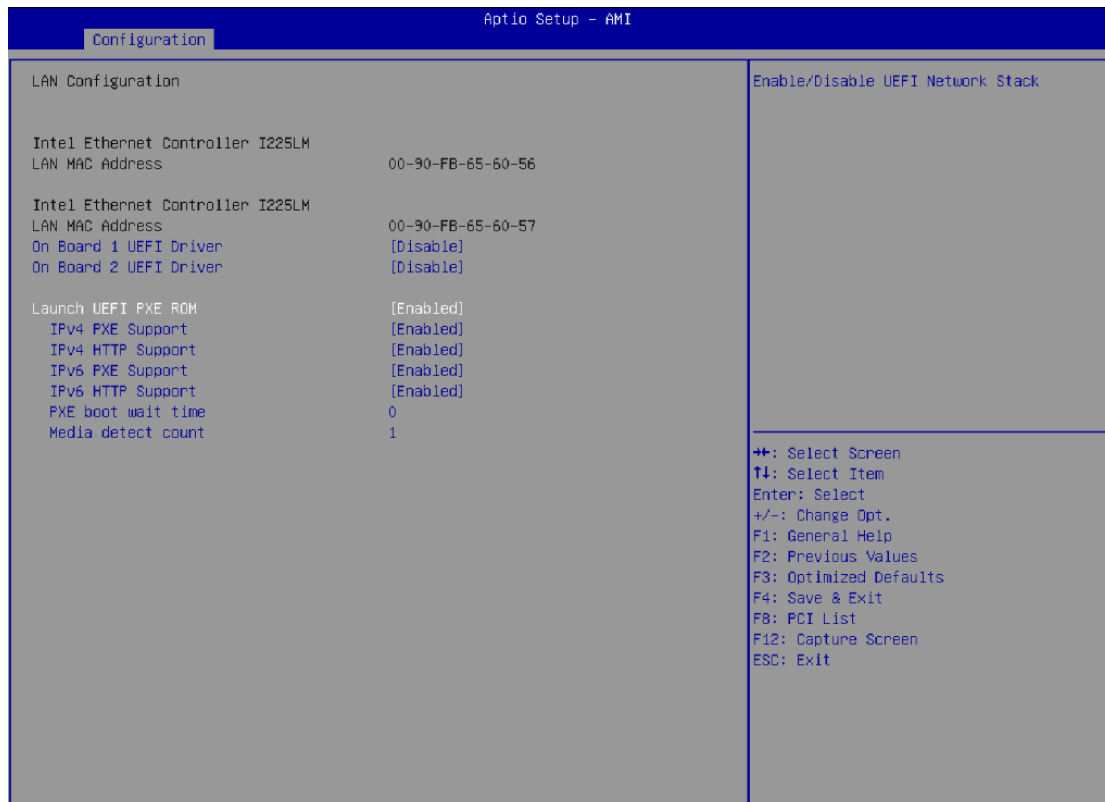
PCI Express Root Port Settings.

←→: Select Screen
 ↑↓: Select Item
 Enter: Select
 +/-: Change Opt.
 F1: General Help
 F2: Previous Values
 F3: Optimized Defaults
 F4: Save & Exit
 F8: PCI List
 F12: Capture Screen
 ESC: Exit

Feature	Description	Options
PCI Express Root Port 7, 9, 10	PCI Express Root Port Setting	

Feature	Description	Options
PCI Express Root Port	Control the PCI Express Root Port.	★Enabled ,Disabled
ASPM	Set the ASPM Level: Force L0s – Force all links to L0s State AUTO-BIOS auto configure DISABLE – Disables ASPM	★Disabled, L1, Auto
PCIe Speed	Configure PCIe Speed	★Auto, Gen1, Gen2, Gen3

6.3.6 LAN Configuration



Feature	Description	Options
On Board 1 UEFI Driver	Control On Board LAN UEFI Driver Disabled or Enabled.	Enabled, ★ Disabled
On Board 2 UEFI Driver	Control On Board LAN UEFI Driver Disabled or Enabled.	Enabled, ★ Disabled
Launch UEFI PXE ROM	Enable/Disable UEFI Network Stack	Enabled, ★ Disabled
Launch UEFI PXE ROM (Enabled)		
IPv4 PXE Support	Enable/Disable IPv4 PXE boot support. If disabled, IPv4 PXE boot support will not be available.	★ Enabled, Disabled
IPv4 HTTP Support	Enable/Disable IPv4 HTTP boot support. If disabled, IPv4 HTTP boot support will not be available.	★ Enabled, Disabled
IPv6 PXE Support	Enable/Disable IPv6 PXE boot support. If disabled, IPv6 PXE boot support will not be available.	★ Enabled, Disabled
IPv6 HTTP Support	Enable/Disable IPv6 HTTP boot support. If disabled, IPv6 HTTP boot support will not be available.	★ Enabled, Disabled
PXE boot wait time	Wait time in seconds to press ESC key to abort the PXE boot. Use either +/- or numeric keys to set the value.	★ 0
Media detect count	Number of times the presence of media will be checked. Use either +/- or numeric keys to set the value.	★ 1

6.3.7 SATA Configuration

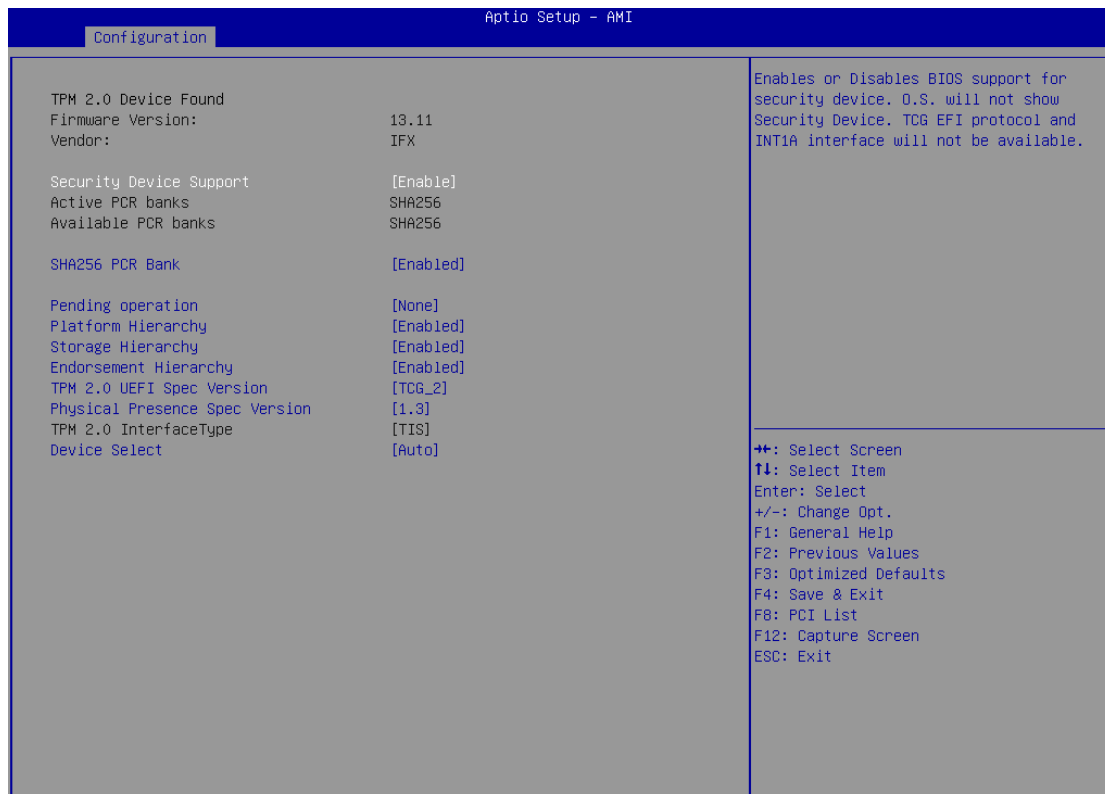


Feature	Description	Options
SATA Controller(s)	Enable/Disable SATA Device	★Enabled , Disabled
Serial ATAPort 0		
Port 0	Enabledor Disabled SATA Port	★Enabled , Disabled
Hot plug	Designates this port as Hot pluggable.	★Disabled, Enabled
SATA Device Type	Identify the SATA port is connected to Solid State Drive or Hard Disk Drive.	Hard Disk Drive, Solid State Drive
SerialATAPort1		
Port 1	Enabledor Disabled SATA Port	★Enabled , Disabled
Hot plug	Designates this port as Hot pluggable.	★Disabled, Enabled
SATA Device Type	Identify the SATA port is connected to Solid State Drive or Hard Disk Drive.	Hard Disk Drive, Solid State Drive

6.3.8 USB Configuration

Configuration		
<div>USB Configuration</div> <div>USB Controllers: 2 XHCIs</div> <div>USB Devices: 2 Drives, 1 Keyboard, 1 Hub</div> <div>USB SS Physical Connector #0 [Enabled] USB SS Physical Connector #1 [Enabled] USB SS Physical Connector #2 [Enabled] USB SS Physical Connector #3 [Enabled]</div> <div>USB HS Physical Connector #0 [Enabled] USB HS Physical Connector #1 [Enabled] USB HS Physical Connector #2 [Enabled] USB HS Physical Connector #3 [Enabled] USB HS Physical Connector #4 [Enabled] USB HS Physical Connector #5 [Enabled] USB HS Physical Connector #6 [Enabled] USB HS Physical Connector #7 [Enabled]</div> <div>XHCI Hand-off [Enabled] USB Mass Storage Driver Support [Enabled]</div> <div>On Board USB Power [Connector] USB3 Port 3 Route [Enable] USB Port0/1 Power [Enable] USB Port2/3 Power [Enable]</div> <div>Mass Storage Devices: Generic Ultra HS-SD/MMC [Auto] USB [Auto]</div>		<div>Enable/Disable this USB Physical Connector (physical port). Once disabled, any USB devices plug into the connector will not be detected by BIOS or OS.</div> <div>+/: Select Screen f1: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit FB: PCI List F12: Capture Screen ESC: Exit</div>
Feature	Description	Options
USB SS Physical Connector #0 ~ #3	Enable/Disable this USB Physical connector (Physical port). Once disabled, any USB devices plug into the connector will not be detected by BIOS or OS.	★Enabled ,Disabled,
USB HS Physical Connector #0 ~ #7	Enable/Disable this USB Physical connector (Physical port). Once disabled, any USB devices plug into the connector will not be detected by BIOS or OS.	★Enabled ,Disabled
XHCI Hand-off	This is a workaround for OSeS without XHCI hand-off support. The XHCI ownership change should be claimed by XHCI driver	★Enabled ,Disabled
USB Mass Storage Driver Support	Enable/Disable USB Mass Storage Driver Support	★Enabled ,Disabled
USB3 Port 3 Route	Control USB3 Port3 Route to M2 or Connector	★Connector, M.2
USB Port0/1 Power	Control USB Port Power Enable or Disable	★Enabled ,Disabled
USB Port2/3 Power	Control USB Port Power Enable or Disable	★Enabled ,Disabled
Generic Ultra HS-SD/MMC	Mass storage device emulation type. ‘AUTO’ enumerates devices according to their media format. Optical drives are emulated as ‘CDROM’; drives with no media will be emulated according to a drive type.	★Auto, Floppy, Forced FDD, Hard Disk, CD-ROM

6.3.9 TPM Configuration: TPM 2.0 Device Found



Feature	Description	Options
Security Device Support	Enables or Disables BIOS support for security device. O.S. will not show Security Device. TCG EFI protocol and INT1A Interface will not be available.	★Enabled, Disabled
SHA256 PCR Bank	Enables or Disables SHA256 PCR Bank.	★Enabled, Disabled
Pending operation	Schedule an Operation for the Security Device. Note: Your Computer will reboot during restart in order to change State of Security Device.	★None, TPM Clear
Platform Hierarchy	Enables or Disables Platform Hierarchy.	★Enabled, Disabled
Storage Hierarchy	Enables or Disables Storage Hierarchy.	★Enabled, Disabled
Endorsement Hierarchy	Enables or Disables Endorsement Hierarchy.	★Enabled, Disabled
TPM2.0 UEFI Spec Version	Select the TCG2 Spec Version Support.	★TCG_2, TCG_1_2
	TCG_1_2: the Compatible mode for Win8/Win10.	
	TCG_2: Support new TCG2 protocol and event format for Win10 or later.	

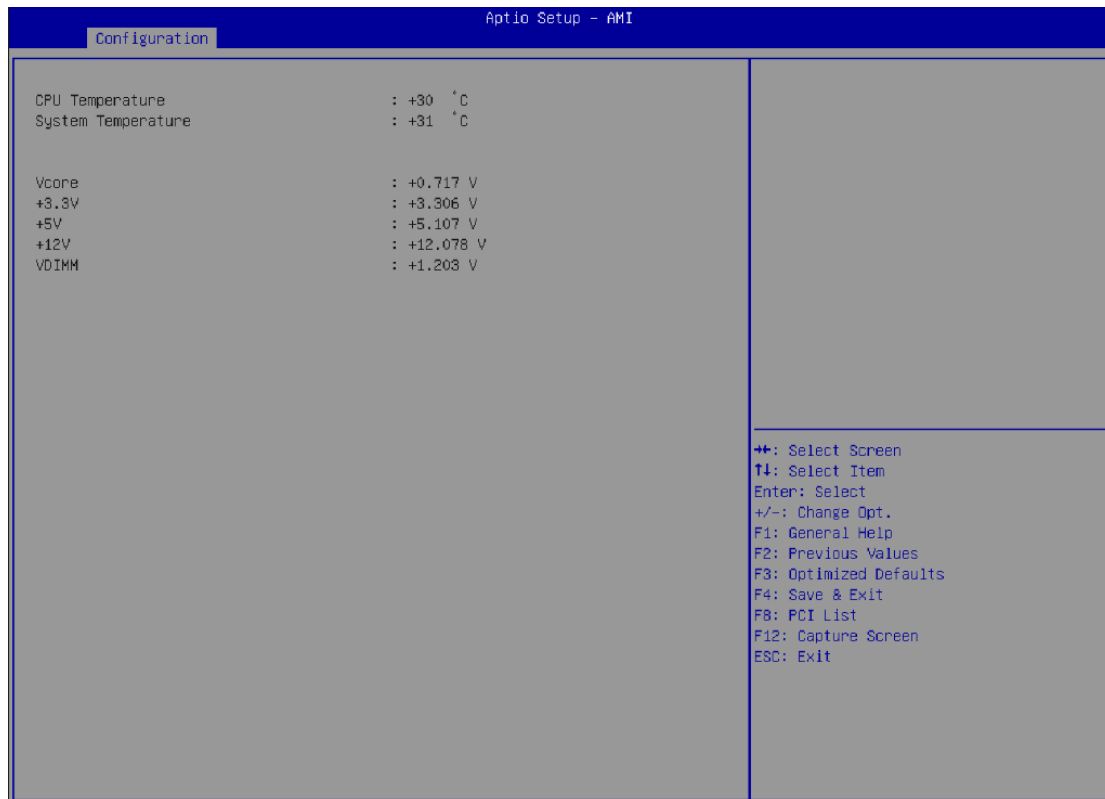
Physical Presence Spec Version	Select to Tell O.S. to Support PPI Spec Version 1.2 or 1.3. Not some HCK tests might not support 1.3.	★1.3, 1.2
Device Select	TPM 1.2 will restrict support to TPM 1.2 devices, TPM 2.0 will restrict support to TPM 2.0 devices, Auto will support both with the default set to TPM 2.0 devices if not found, TPM 1.2 devices will be enumerated.	★Auto, TPM 1.2, TPM 2.0

6.3.10 Super IO Configuration



Feature	Description	Options
ModuleSerialPort 1	Enable or Disable Serial Port (COM)	★Enabled, Disabled
RS-232/422/485 Control Option	SerialPort 3 RS-232/422/485 Control Option	★RS-232, RS-485 HALF DUPLEX, RS-422 FULL DUPLEX,
Watch Dog Timer	Enable/Disable Watch Dog Timer	★Disabled, Enabled
Watch Dog Timer [Enabled]		
Timer Unit	Select Timer count unit of WDT	★Second, Minute
Timer value	Set WDT Timer value seconds / minutes	★20

6.3.11 HW Monitor



6.3.12 Serial Port Console Redirection

Configuration Aptio Setup - AMI

Serial Port Console Redirection

COM0
 Console Redirection [Disabled]
 ▶ Console Redirection Settings

Console Redirection Enable or Disable.

←→: Select Screen
 ↑↓: Select Item
 Enter: Select
 +/-: Change Opt.
 F1: General Help
 F2: Previous Values
 F3: Optimized Defaults
 F4: Save & Exit
 F12: Capture Screen
 ESC: Exit

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Feature	Description	Options
Console Redirection	Console Redirection Enable or Disable	★Disabled, Enabled

COM0 Console Redirection Settings:

Configuration
Aptio Setup - AMI

COM0
Console Redirection Settings

Terminal Type [VT100Plus]
 Bits per second [115200]
 Data Bits [8]
 Parity [None]
 Stop Bits [1]
 Flow Control [None]
 VT-UTF8 Combo Key Support [Enabled]
 Recorder Mode [Disabled]
 Resolution 100x31 [Disabled]
 Putty KeyPad [VT100]

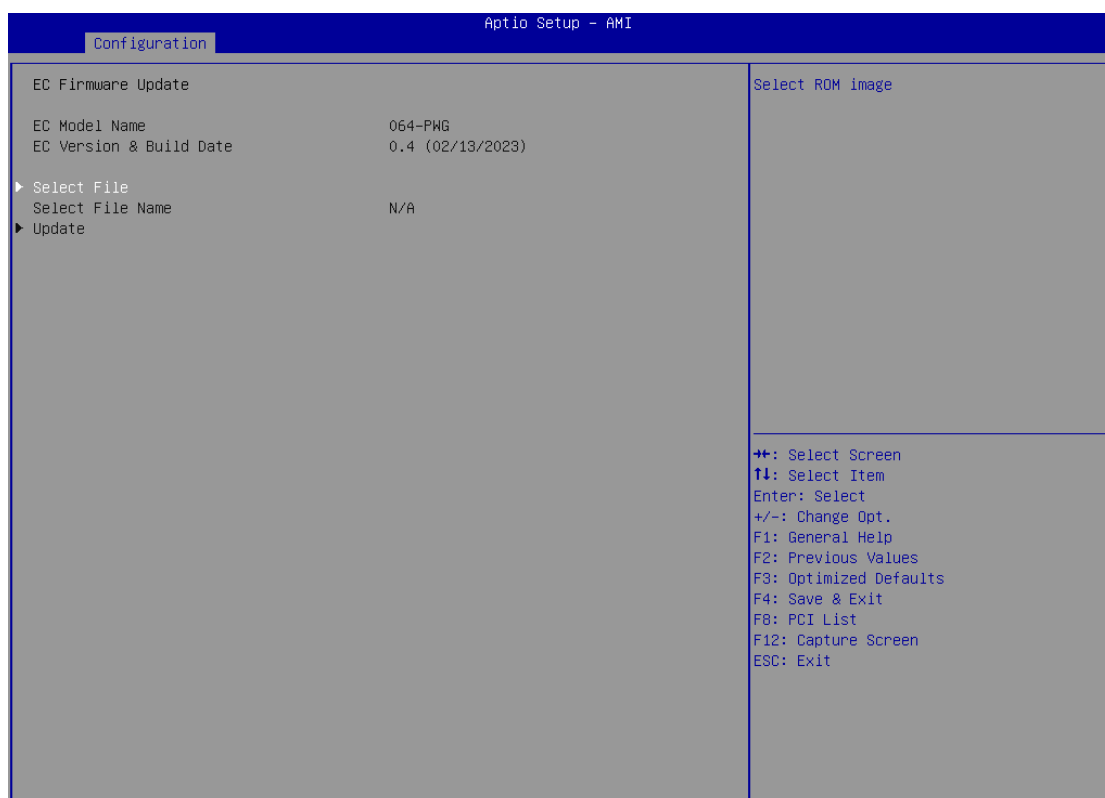
Emulation: ANSI: Extended ASCII char set. VT100: ASCII char set. VT100Plus: Extends VT100 to support color, function keys, etc. VT-UTF8: Uses UTF8 encoding to map Unicode chars onto 1 or more bytes.

** : Select Screen
 ↑↓ : Select Item
 Enter : Select
 +/- : Change Opt.
 F1 : General Help
 F2 : Previous Values
 F3 : Optimized Defaults
 F4 : Save & Exit
 F8 : PCI List
 F12 : Capture Screen
 ESC : Exit

Feature	Description	Options
Terminal Type	Emulation: ANSI: Extended ASCII char set. VT100: ASCII char set. VT100Plus: Extends VT100 to support color, function keys, etc. VT-UTF8: Uses UTF8 encoding to map Unicode chars onto 1 or more bytes.	★VT100Plus, ANSI, VT100, VT-UTF8
Bits per second	Select Serial port transmission speed. The speed must be matched on other side. Long or noisy lines may require lower speeds.	★115200, 9600, 19200, 38400, 57600
Data bits	Data bits	★8, 7
Parity	A parity bit can be sent with the data bits to detect some transmission errors. Even: parity bit is 0 if the num of 1's in the data bits is even. Odd: parity bit is 0 if num of 1's in the data bits is odd. Mark: parity bit is always 1. Space parity bit is always 0. Mark and Space Parity do not allow for error detection. They can be used as an additional data bit.	★None, Even, Odd, Mark, Space
Stop Bits	Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may require more than 1 stop bit.	★1,2
Flow Control	Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signal.	★None, Hardware RTS/CTS

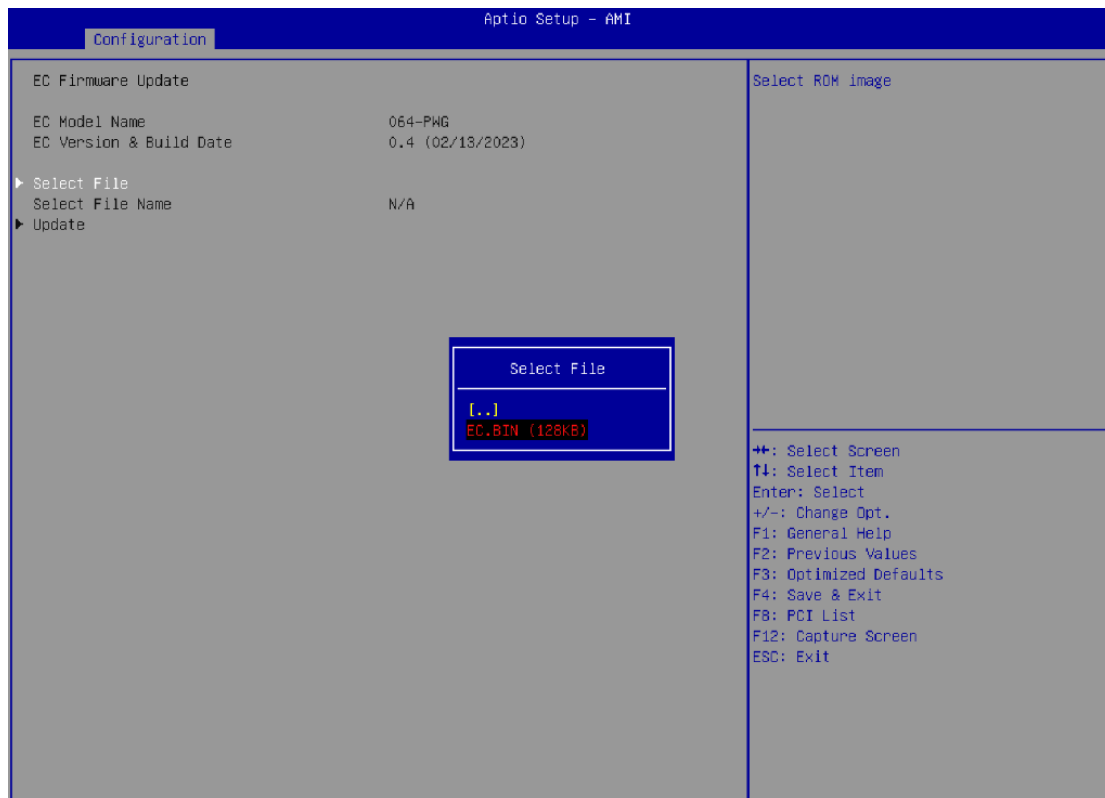
VT-UTF8 Combo Key Support	Enable VT-UTF8 Combination Key Support for ANSI/VT100 terminals	★Enabled, Disabled
Recorder Mode	With this mode enabled only text will be sent. This is to capture Terminal data.	★Disabled, Enabled
Resolution 100x31	Enables or disables extended terminal resolution	★Disabled, Enabled
Putty KeyPad	Select FunctionKey and KeyPad on Putty	★VT100, LINUX,XTERMR6, SCO,ESCN,VT400

6.3.13 EC Firmware Update

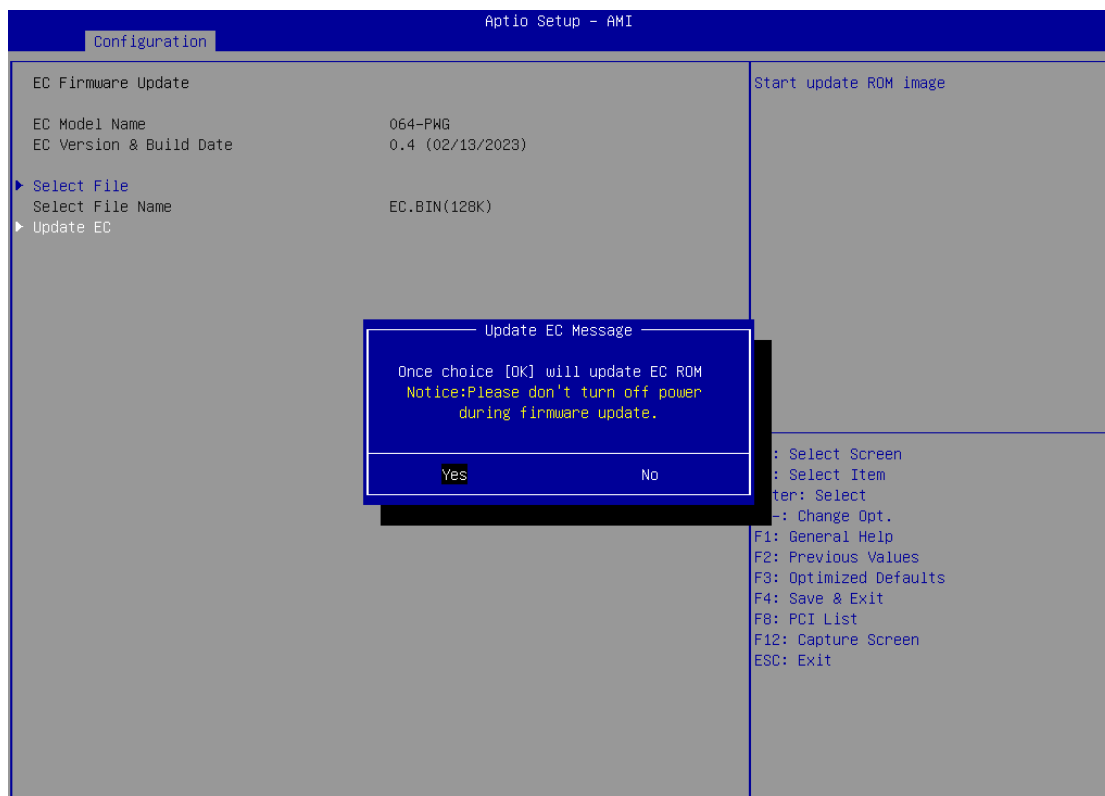


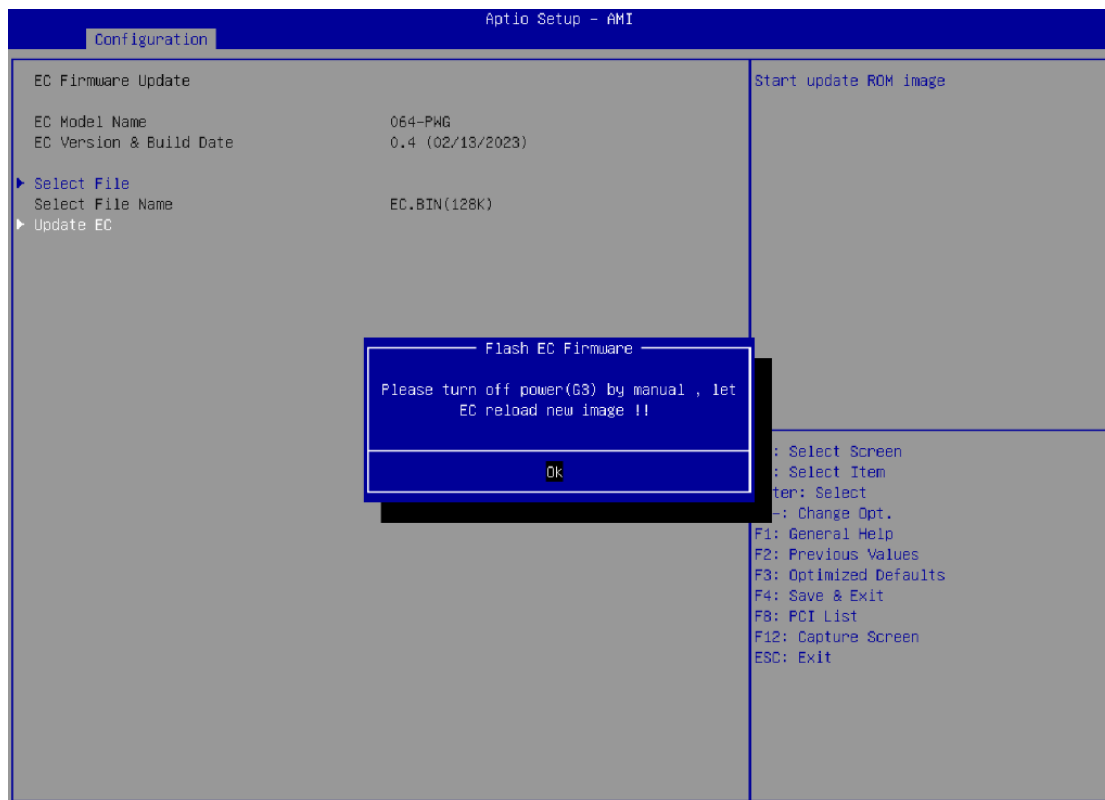
Feature	Description	Options
Select File	Select BIOS BIN file in (USB) drive to update	
Update	Start update ROM image	

Select file

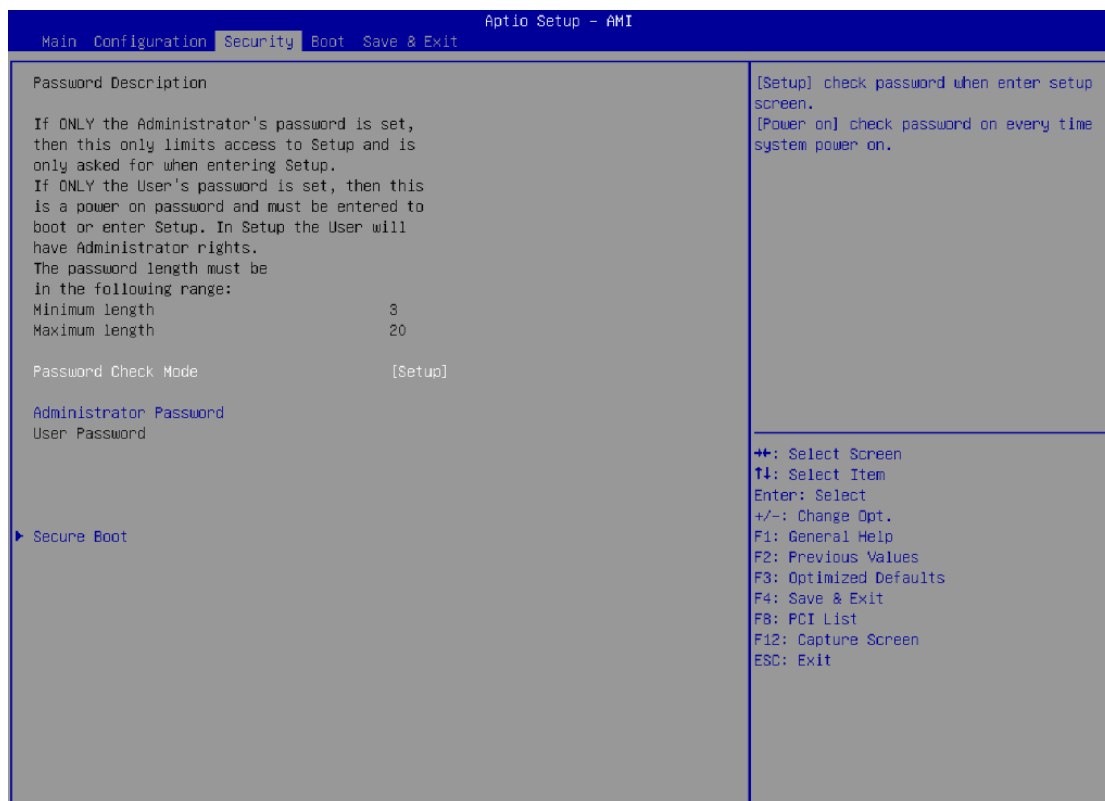


6.3.14 Update EC





6.3.15 Security



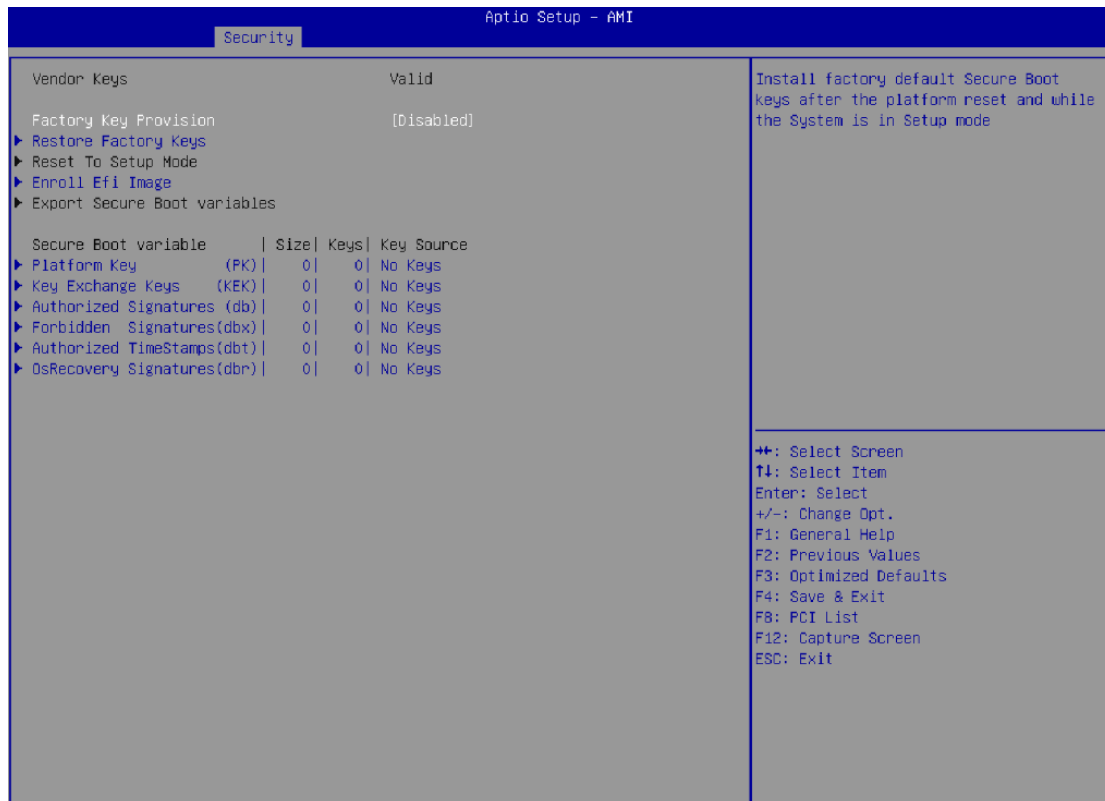
Feature	Description	Options
Password Check Mode	[Setup] check password when enter setup screen. [Power on] check password on every time system power on.	★Setup, Power On
Administrator Password	Set Administrator Password	
Secure Boot	Secure Boot configuration	

Secure Boot



Feature	Description	Options
Secure Boot	Secure Boot feature is Active if Secure Boot is Enabled, Platform Key (PK) is enrolled and the System is in User mode. The mode change requires platform reset.	★Disabled, Enabled
Secure Boot Mode	Secure Boot Mode options: Standard or Custom. In Custom mode, Secure Boot Policy variables can be configured by a physically present user without full authentication	★Custom, Standard
Restore Factory keys	Force System to User Mode. Install factory default Secure Boot key databases	Yes, No
Key Management	Enables expert users to modify Secure Boot Policy variables without variable authentication	

Key Management



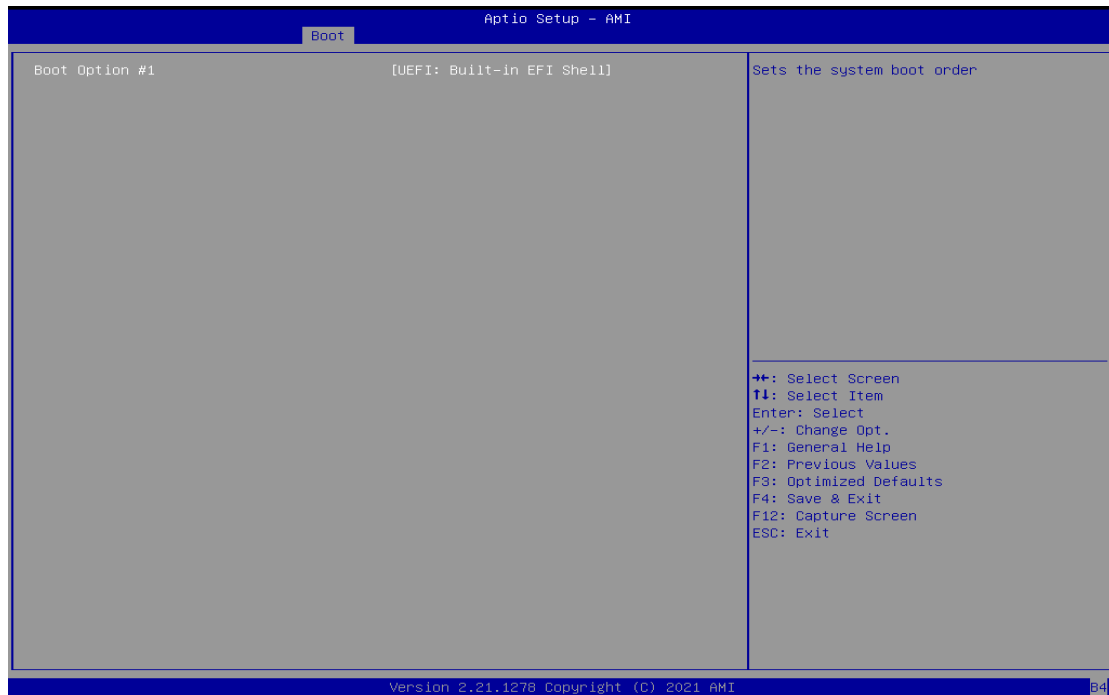
Feature	Description	Options
Factory keys Provision	Install factory default Secure Boot key after the platform reset and while the System is in Setup mode.	★Disabled, Enabled
Restore Factory keys	Force System to User Mode. Install factory default Secure Boot key databases	Yes, No
Enroll Efi Image	Allow Efi image to run in Secure Boot mode. Enroll SHA256 Hash certificate of a PE image into Authorized Signature Database (db)	
Platform Key(PK)	Enroll Factory Defaults or load certificates from a file:	
	1.Public Key Certificate:	
	a)EFI_SIGNATURE_LIST	
	b) EFI_CERT_X509 (DER)	
	c) EFI_CERT_RSA2048 (bin)	
Key Exchange Keys(KEK)	d)EFI_CERT_SHAXXX	
Authorized Signatures(db)	2.Authenticated UEFI Variable	
Forbidden Signatures(dbx)	3.EFI PE/COFF Image(SHA256)	
Authorized TimeStamps(dbt)	Key Source:	
OsRecovery Signatures(dbr)	Factory, Modified, Mixed	

6.3.16 Boot

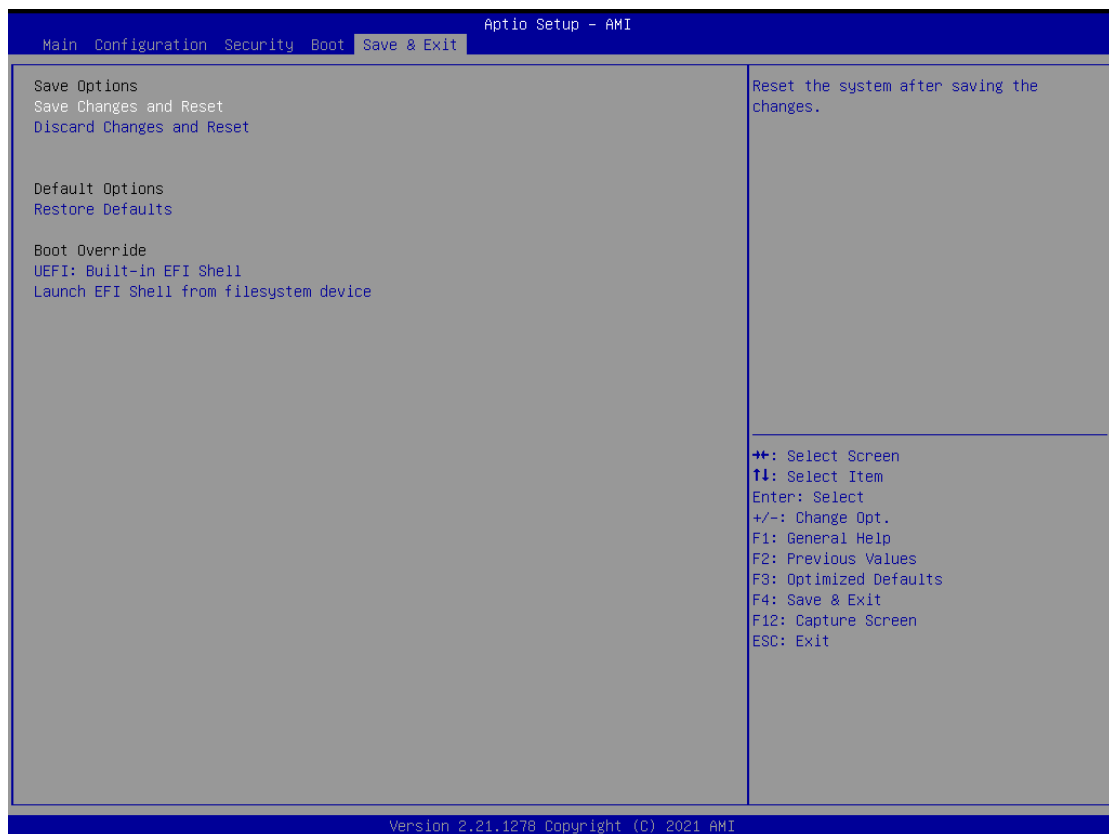


Feature	Description	Options
Setup Prompt Timeout	Number of seconds to wait for setup activation key. 65535(0xFFFF) means indefinite waiting.	★1
BootupNumLockState	Select the keyboard NumLock state.	★On, Off
Full Screen LOGO	Enables or disables Quiet Boot option and Full screen Logo.	★Disabled, Enabled
Boot Option #1 ~ #5	Sets the system boot order	Hard Disk, UEFI AP: UEFI: Built-in EFI Shell, CD/DVD, USB Device; Network, Disabled
UEFI Application Boot Priorities	Specifies the Boot Device Priority sequence from available UEFI Application	

UEFI Application Boot Priorities:



6.3.17 Save & Exit



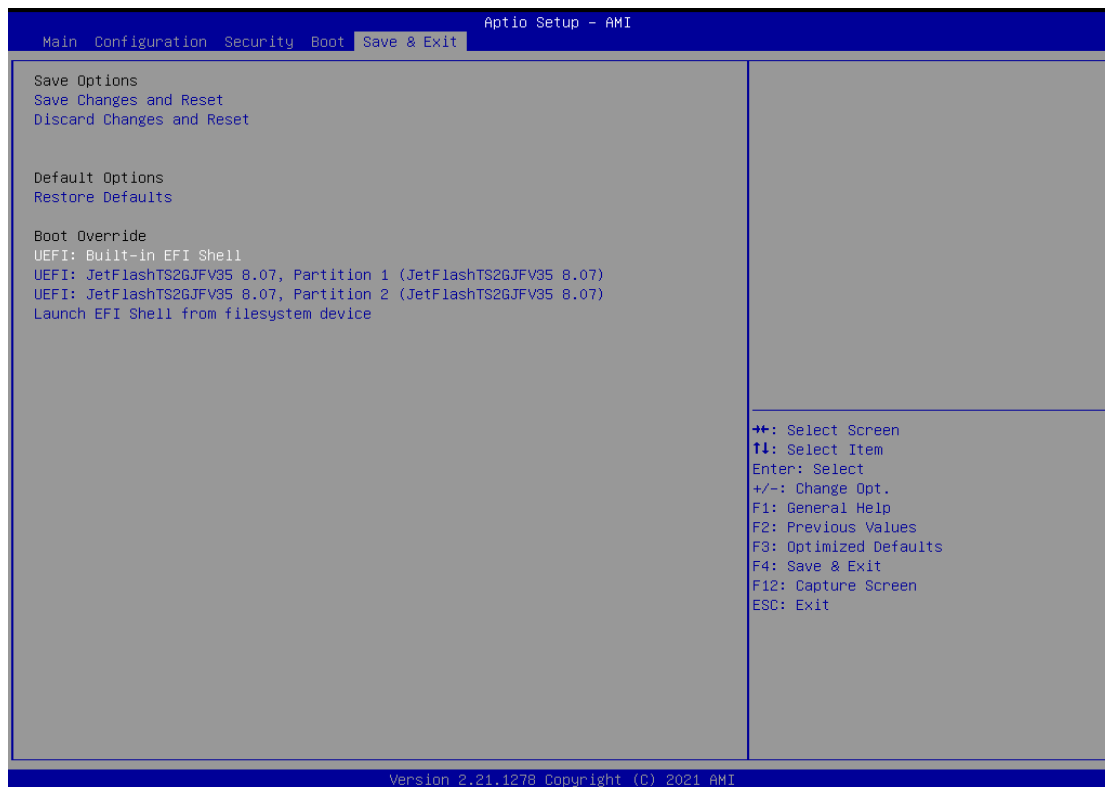
Feature	Description	Options
Save Changes and Reset	Reset the system after saving the changes.	
Discard Changes and Reset	Reset system setup without saving any changes.	
Restore Defaults	Restore/Load Default values for all the setup options.	
UEFI: Built-in EFI Shell		
Launch EFI Shell from filesystem device	Attempts to Launch EFI Shell application (Shell.efi) from one of the available filesystem devices.	

NANO-6065 BIOS / EC UEFI Update SOP process under UEFI Shell

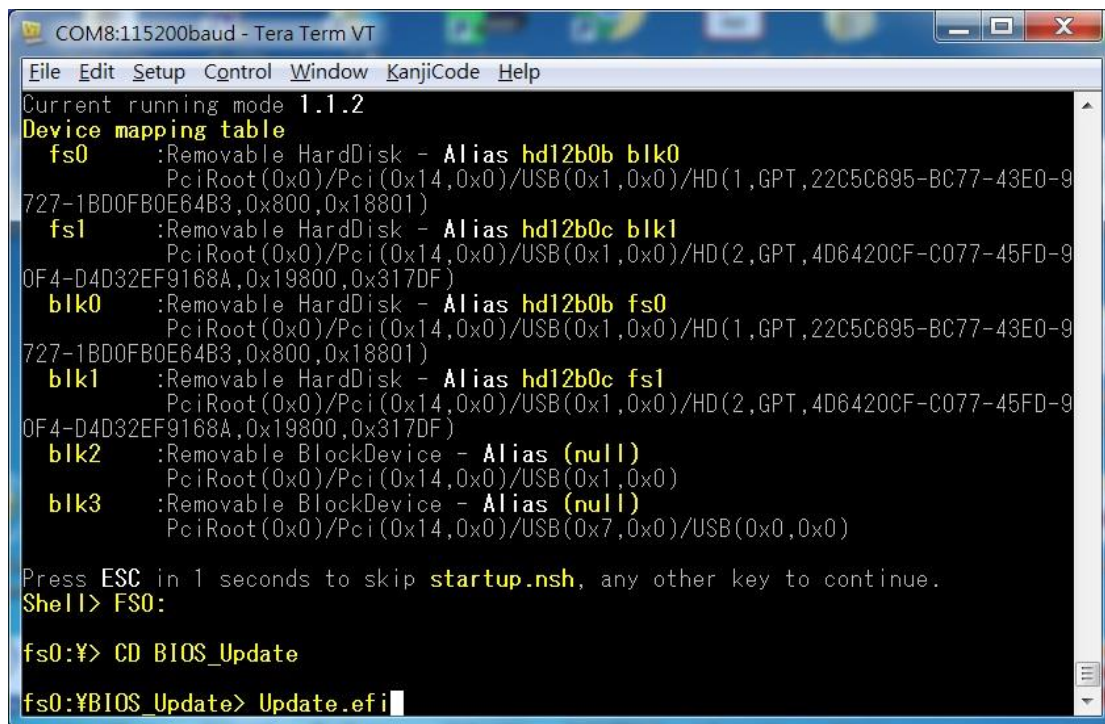
Step 1. Prepare a USB DOK.

Step 2. Unzip BIOS update file to the USB DOK.

Step 3. Plug the USB DOK into the target system and then boot in UEFI Shell by selecting UEFI: Built-in EFI Shell in the BIOS Save & Exit page.



Step 4. Under the UEFI shell, direct to your USB DOK, below picture is an example using fs0. Then direct to the folder with BIOS / EC updated file and then enter command: "Update.efi" to start updating BIOS / EC.



```

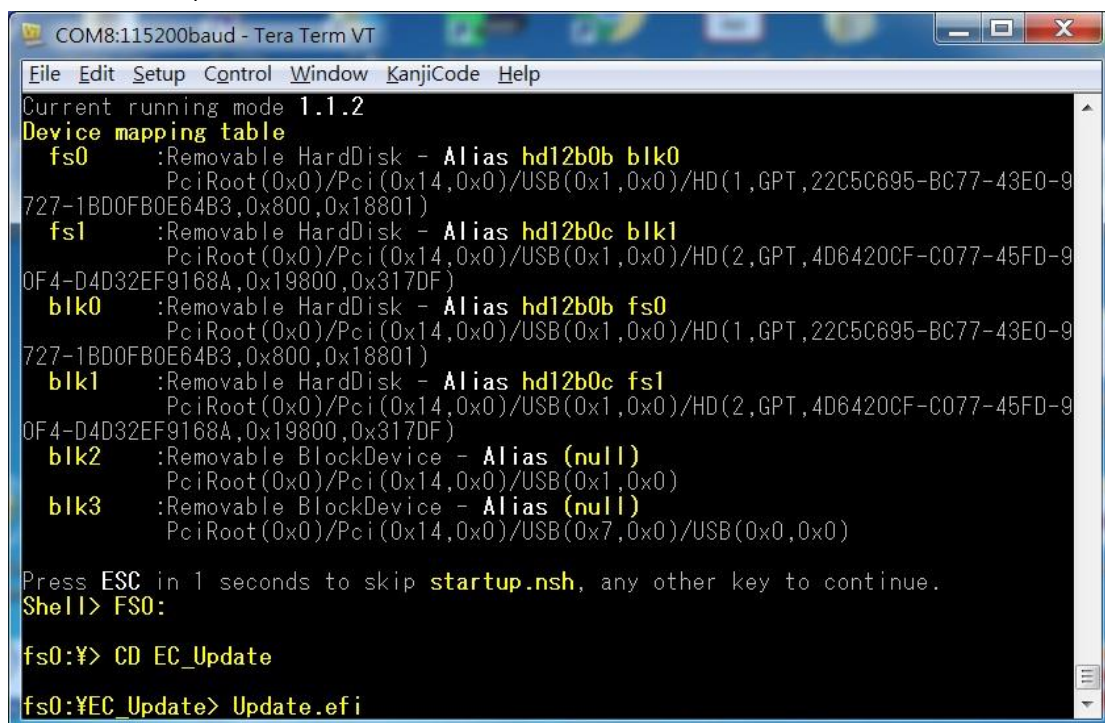
COM8:115200baud - Tera Term VT
File Edit Setup Control Window KanjiCode Help
Current running mode 1.1.2
Device mapping table
fs0 :Removable HardDisk - Alias hd12b0b blk0
      PciRoot(0x0)/Pci(0x14,0x0)/USB(0x1,0x0)/HD(1,GPT,22C5C695-BC77-43E0-9
727-1BD0FB0E64B3,0x800,0x18801)
fs1 :Removable HardDisk - Alias hd12b0c blk1
      PciRoot(0x0)/Pci(0x14,0x0)/USB(0x1,0x0)/HD(2,GPT,4D6420CF-C077-45FD-9
0F4-D4D32EF9168A,0x19800,0x317DF)
blk0 :Removable HardDisk - Alias hd12b0b fs0
      PciRoot(0x0)/Pci(0x14,0x0)/USB(0x1,0x0)/HD(1,GPT,22C5C695-BC77-43E0-9
727-1BD0FB0E64B3,0x800,0x18801)
blk1 :Removable HardDisk - Alias hd12b0c fs1
      PciRoot(0x0)/Pci(0x14,0x0)/USB(0x1,0x0)/HD(2,GPT,4D6420CF-C077-45FD-9
0F4-D4D32EF9168A,0x19800,0x317DF)
blk2 :Removable BlockDevice - Alias (null)
      PciRoot(0x0)/Pci(0x14,0x0)/USB(0x1,0x0)
blk3 :Removable BlockDevice - Alias (null)
      PciRoot(0x0)/Pci(0x14,0x0)/USB(0x7,0x0)/USB(0x0,0x0)

Press ESC in 1 seconds to skip startup.nsh, any other key to continue.
Shell> FS0:

fs0:¥> CD BIOS_Update
fs0:¥BIOS_Update> Update.efi

```

(BIOS File Update)



```

COM8:115200baud - Tera Term VT
File Edit Setup Control Window KanjiCode Help
Current running mode 1.1.2
Device mapping table
fs0 :Removable HardDisk - Alias hd12b0b blk0
      PciRoot(0x0)/Pci(0x14,0x0)/USB(0x1,0x0)/HD(1,GPT,22C5C695-BC77-43E0-9
727-1BD0FB0E64B3,0x800,0x18801)
fs1 :Removable HardDisk - Alias hd12b0c blk1
      PciRoot(0x0)/Pci(0x14,0x0)/USB(0x1,0x0)/HD(2,GPT,4D6420CF-C077-45FD-9
0F4-D4D32EF9168A,0x19800,0x317DF)
blk0 :Removable HardDisk - Alias hd12b0b fs0
      PciRoot(0x0)/Pci(0x14,0x0)/USB(0x1,0x0)/HD(1,GPT,22C5C695-BC77-43E0-9
727-1BD0FB0E64B3,0x800,0x18801)
blk1 :Removable HardDisk - Alias hd12b0c fs1
      PciRoot(0x0)/Pci(0x14,0x0)/USB(0x1,0x0)/HD(2,GPT,4D6420CF-C077-45FD-9
0F4-D4D32EF9168A,0x19800,0x317DF)
blk2 :Removable BlockDevice - Alias (null)
      PciRoot(0x0)/Pci(0x14,0x0)/USB(0x1,0x0)
blk3 :Removable BlockDevice - Alias (null)
      PciRoot(0x0)/Pci(0x14,0x0)/USB(0x7,0x0)/USB(0x0,0x0)

Press ESC in 1 seconds to skip startup.nsh, any other key to continue.
Shell> FS0:

fs0:¥> CD EC_Update
fs0:¥EC_Update> Update.efi

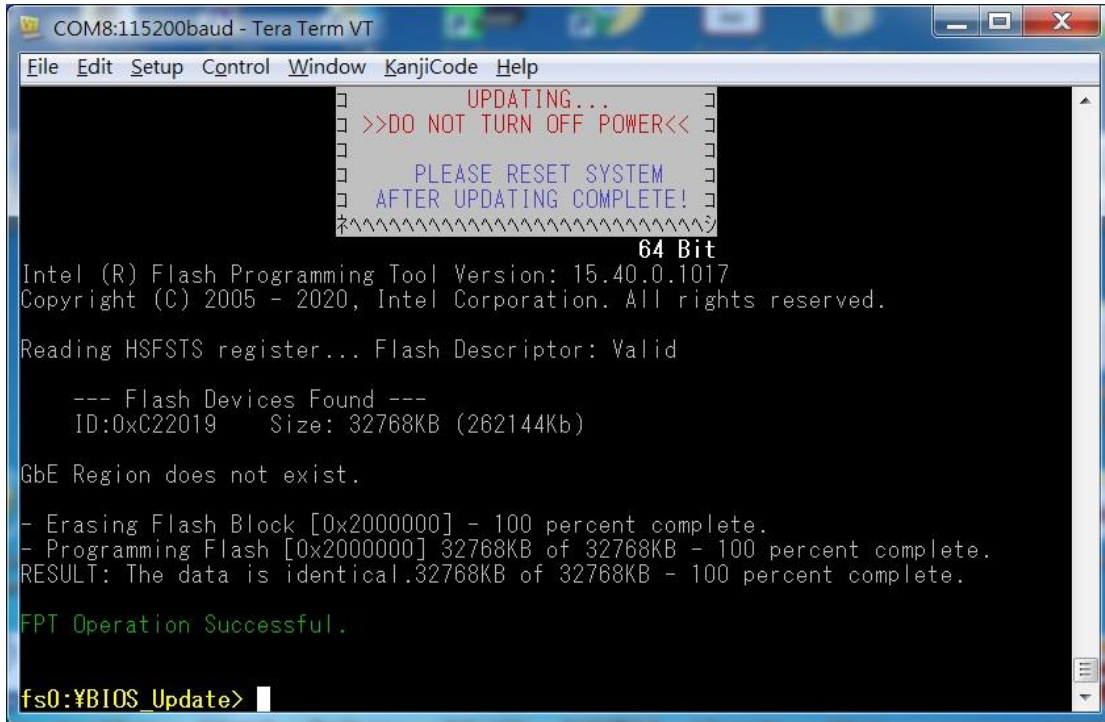
```

(EC File Update)

Step 5. The updating process will start and you can see the updating progress.

When you see the following pictures, which means the BIOS / EC update processes finished.

Please cut the AC power off and wait for 10 seconds before powering on.



```

COM8:115200baud - Tera Term VT
File Edit Setup Control Window KanjiCode Help

UPDATING...
>>DO NOT TURN OFF POWER<<

PLEASE RESET SYSTEM
AFTER UPDATING COMPLETE!

64 Bit
Intel (R) Flash Programming Tool Version: 15.40.0.1017
Copyright (C) 2005 - 2020, Intel Corporation. All rights reserved.

Reading HSFSTS register... Flash Descriptor: Valid

--- Flash Devices Found ---
ID:0xC22019 Size: 32768KB (262144Kb)

GbE Region does not exist.

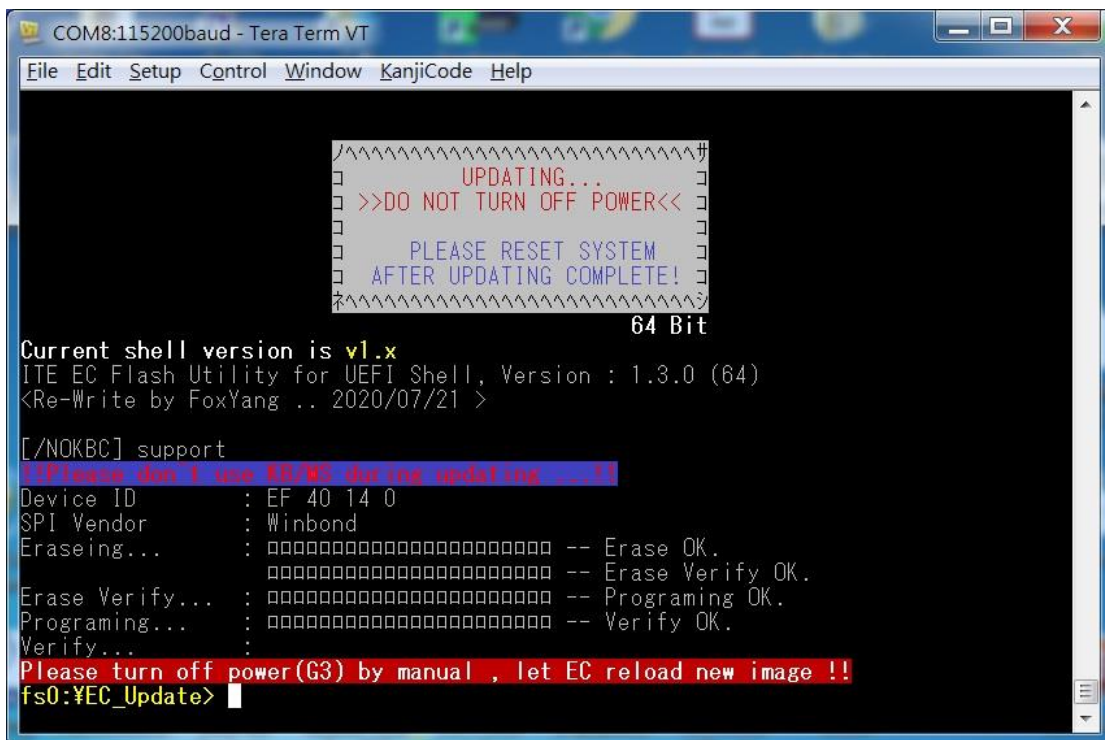
- Erasing Flash Block [0x20000000] - 100 percent complete.
- Programming Flash [0x20000000] 32768KB of 32768KB - 100 percent complete.
RESULT: The data is identical. 32768KB of 32768KB - 100 percent complete.

FPT Operation Successful.

fs0:¥BIOS_Update>

```

(BIOS update finished)



```

COM8:115200baud - Tera Term VT
File Edit Setup Control Window KanjiCode Help

UPDATING...
>>DO NOT TURN OFF POWER<<

PLEASE RESET SYSTEM
AFTER UPDATING COMPLETE!

64 Bit
Current shell version is v1.x
ITE EC Flash Utility for UEFI Shell, Version : 1.3.0 (64)
<Re-Write by FoxYang .. 2020/07/21 >

[/NOKBC] support
Please don't use ER/WS during updating ...!!

Device ID : EF 40 14 0
SPI Vendor : Winbond
Eraseing... : Erase OK.
Erase Verify... : Erase Verify OK.
Programing... : Programing OK.
Verify... : Verify OK.

Please turn off power(G3) by manual , let EC reload new image !!

fs0:¥EC_Update>

```

(EC update finished)

Chapter 7

Overview

- 7 System Resources
- 7.1 Intel® Amston/ Twin Lake SoC
- 7.2 Main Memory
- 7.3 Installing the Single Board Computer

7 System Resources

7.1 Intel® Amston/ Twin Lake SoC

Intel® Core 3 processor N355

Intel® processor N150

Intel® Atom® x7835RE 1.3GHz

7.2 Main Memory

NANO-6065 provides one 260-pin SO-DIMM socket which supports DDR5 non-ECC memory. The maximum memory can be up to 16GB. Memory clock and related settings can be detected by BIOS via SPD interface.

Watch out the contact and lock integrity of memory module with socket, it will impact on the system reliability. Follow normal procedures to install the memory module into memory socket. Before locking, make sure that all modules have been fully inserted into the card slots.

7.3 Installing the Single Board Computer

To install your NANO-6065 into a standard chassis or proprietary environment, please perform the following:

Step 1: Check all jumpers setting on proper position

Step 2: Install and configure memory module on right position

Step 3: Place NANO-6065 into the dedicated position in the system

Step 4: Attach cables to existing peripheral devices and secure it

WARNING

Please ensure that the motherboard is properly inserted and fixed by

the mechanism.

Note:

Please find drivers in the NANO-6065 of Portwell's download center.

The driver supports Windows 10/11.

Chapter 8

Overview

- 8 Troubleshooting
- 8.1 Hardware Quick Installation
- 8.2 BIOS Setting
- 8.3 FAQ

8 Troubleshooting

This chapter provides a few useful tips to quickly get NANO-6065 running with success.

8.1 Hardware Quick Installation

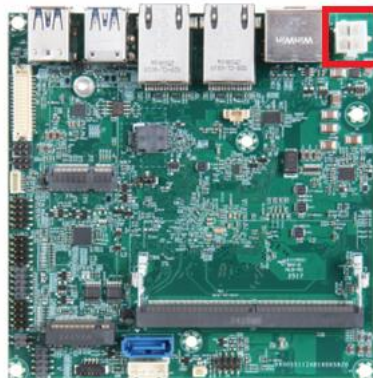
ATX Power Setting

To connect the power to the NANO-6065, which uses an ATX 4-pin connector (J6).

J6: ATX 4 Pin

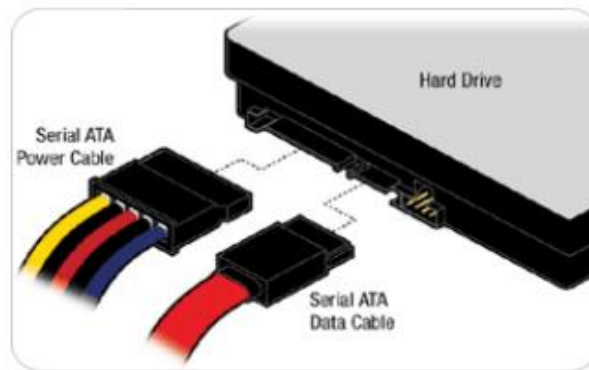
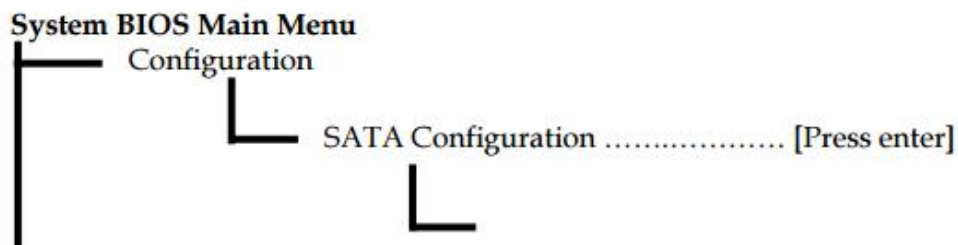
PIN No.	Signal Description
1	+12V
2	+12V
3	Ground
4	Ground

Connector



Serial ATA

Serial ATA Hard Disk Setting for SATA Speed Selection



SATA Speed Selection [Auto, Gen1, Gen2, Gen3]

Install M.2 devices

M.2 B Key and E Key share the same mounting hole.

If you plan to install both M.2 devices, install the E Key device first and secure it using the accessory standoff.

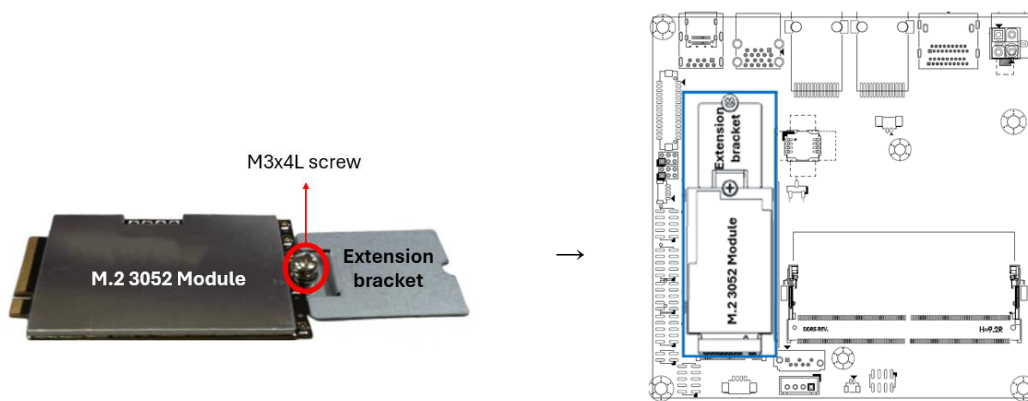
Then, install the B Key device and fasten it with the provided screw.

Additionally, if your B Key device uses the 3052-form factor, an extension bracket will be required to reach the 2280 mounting hole.

Extension bracket

The NANO-6065 only has a boss-standoff for M.2 Key B slots at the 2280 position. To accommodate M.2 3052 modules, we've included an extension bracket. Please refer to the image below for installation instructions.

Fasten with M3x4L screws.



Other installation precautions

1. Unplug the power cord before touching any components.
2. To avoid damage caused by static electricity, do not place the motherboard directly on carpet or similar surfaces. Always wear a grounded wrist strap or touch a grounded object before handling components.
3. Hold components by their edges and avoid touching the ICs.
4. When uninstalling any component, place it on a grounded antistatic pad or store it in the original antistatic packaging.
5. A system-level thermal solution should be designed and implemented separately. When the CPU TDP exceeds 10W, an active cooler is recommended to ensure optimal performance and stability.

8.2 BIOS Setting

It is assumed that users have correctly adopted modules and connected all the devices & cables required before turning on ATX power.

262-pin DDR5 4800MT/s SO-DIMM Memory, keyboard, mouse, SATA hard disk, HDMI connector, device power cables, ATX accessories are good examples that deserve attention. With no assurance of properly and correctly accommodating these modules and devices, it is very possible to encounter system failures that result in malfunction of any device.

To make sure that you have a successful start with NANO-6065, it is recommended, when going with the boot-up sequence, to hit “DEL” and” ESC” key and enter the BIOS setup menu to tune up a stable BIOS configuration so that you can wake up your system far well.

Loading the default optimal setting

When prompted with the main setup menu, please scroll down to “**RestoreDefaults**”, press “**Enter**” and select “**Yes**” to load default optimal BIOS setup.

This will force your BIOS setting back to the initial factory configurations. It is recommended to do this so you can be sure the system is running with the BIOS setting that Portwell has highly endorsed. As a matter of fact, users can load the default BIOS setting at any time when system appears to be unstable in boot up sequence.

8.3 FAQ

Information & Support

- Question: I forgot my password for system BIOS, what am I supposed to do?

Answer: You can switch off your power supply then find the RTC Battery on NANO-6065. Then remove the RTC battery and wait 5 seconds to clean your password then to switch on your power supply.

- Question: How to update the BIOS file of NANO-6065?

Answer:

1. Please visit the web site of Portwell download center as below hyperlink <https://download.portwell.tw/>
2. Select “Search download” and type the keyword “NANO-6065”.
3. Find the “BIOS” page and download the ROM file and flash utility.
4. Unzip file to bootable USB flash drive which can boot to shell mode. Then execute the “update.efi”. It will start to update BIOS.
5. When you see the “FPT Operation Passed” message, which means the BIOS update processes finished. Please cut the AC power off and wait for 10 seconds before powering on.
6. If you have other additional technical information or requests which are not covered in this manual, please fill in the technical request form as below hyperlink.

<https://www.portwell.com.tw/support-center/technical-request/>

We will do our best to provide a suggestion or solution for you.

Chapter 9

Overview

9 Portwell Software Service

9 Portwell Software Service

1. If you have customized requirements of BIOS, you can contact people from our company or branch.
2. If you have requirements of WDT、GPIO APP, you can contact our headquarter or branch, and we can render your assistance on developing.

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American Portwell Technology (USA)	E-mail: info@portwell.com
European Portwell Technology (Netherlands)	E-mail: info@portwell.eu
Portwell UK Ltd. (UK)	E-mail: info@portwell.eu
KIOSK Embedded Systems GmbH	E-mail: info@portwell.eu
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Portwell Korea, Inc. (Korea)	E-mail: info@portwell.co.kr



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