

COM Express Carrier Design Guide

Carrier design guideline for PCOM-B659

Rev. R0.2

Revision history

Rev.	Date	Note
R0.1	6 th . May.2024	1st Draft
R0.2	16 th March 2026	Add RTC Ref Design

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1 Introduction

The Carrier Design Guide provides the guideline of designing your own carrier board based on Portwell's COM Express Modular product PCOM-B659. PCOM-B659 is a Type 6, 95x95mm Modular board, more information is included in PCOM-B659 User's Guide and can be downloaded from Portwell download center (Or contact your Portwell sales representative for acquiring PCOM-B659 User's Guide). This carrier design guide is dedicated for the designers designing a COM Express Type 6 carrier board which will have a excellent compatibility with Portwell's PCOM-B659 modular product.

The layout guideline provided are 8 PCB layer stack up, each interface has three sections, which are detail PCOM-B659 pin out, pin name, power rail, PU/PD, AC couple capacitor and etc. information are included. Second part contains PCB layout guide, impedance, maximum trace, trace width, and trace spacing etc. Third section provides the available trace length of which designers are able to optimize the high speed signals such as PCIE, SATA, USB etc.

2 PCOM-B659

2.1 PCOM-B659 Block Diagram

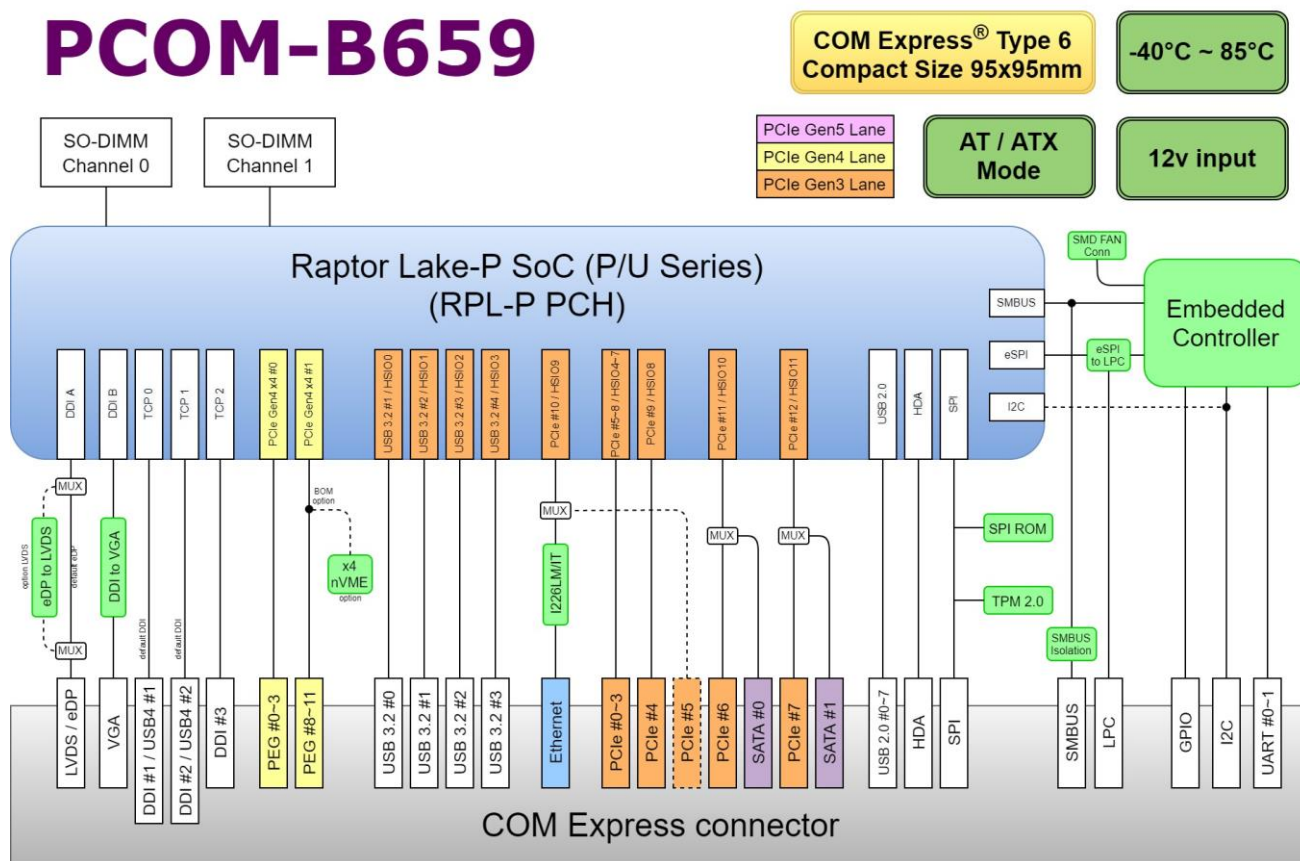


Figure 1 PCOM-B659 Block Diagram

2.2 PCOM-B659 Pin-out

PCOM-B659 Type6 Pin-Out							
Pin	Row A	Pin	Row B	Pin	Row C	Pin	Row D
A1	GND(FIXED)	B1	GND(FIXED)	C1	GND(FIXED)	D1	GND(FIXED)
A2	GBE0_MDI3-	B2	GBE0_ACT#	C2	GND	D2	GND
A3	GBE0_MDI3+	B3	LPC_FRAME#	C3	USB_SSRX0-	D3	USB_SSTX0-
A4	GBE0_LINK_1000#	B4	LPC_AD0	C4	USB_SSRX0+	D4	USB_SSTX0+
A5	GBE0_LINK_2500#	B5	LPC_AD1	C5	GND	D5	GND
A6	GBE0_MDI2-	B6	LPC_AD2	C6	USB_SSRX1-	D6	USB_SSTX1-
A7	GBE0_MDI2+	B7	LPC_AD3	C7	USB_SSRX1+	D7	USB_SSTX1+
A8	GBE0_LINK#	B8	N/C	C8	GND	D8	GND
A9	GBE0_MDI1-	B9	ESPT_ALERT#	C9	USB_SSRX2-	D9	USB_SSTX2-
A10	GBE0_MDI1+	B10	LPC_CLK	C10	USB_SSRX2+	D10	USB_SSTX2+
A11	GND(FIXED)	B11	GND(FIXED)	C11	GND(FIXED)	D11	GND(FIXED)
A12	GBE0_MDI0-	B12	PWRBTN#	C12	USB_SSRX3-	D12	USB_SSTX3-
A13	GBE0_MDI0+	B13	SMB_CK	C13	USB_SSRX3+	D13	USB_SSTX3+
A14	N/C	B14	SMB_DAT	C14	GND	D14	GND
A15	SUS_S3#	B15	SMB_ALERT#	C15	USB4_1_LSTX	D15	DDI1_CTRLCLK_AUX+
A16	SATA0_TX+	B16	SATA1_TX+	C16	USB4_1_LSRX	D16	DDI1_CTRLCLK_AUX-
A17	SATA0_TX-	B17	SATA1_TX-	C17	USB4_RT_ENA	D17	USB4_PD_I2C_ALERT#
A18	SUS_S4#	B18	SUS_STAT	C18	GND	D18	PMCALERT#
A19	SATA0_RX+	B19	SATA1_RX+	C19	PCIE_RX6+	D19	PCIE_TX6+
A20	SATA0_RX-	B20	SATA1_RX-	C20	PCIE_RX6-	D20	PCIE_TX6-
A21	GND(FIXED)	B21	GND(FIXED)	C21	GND(FIXED)	D21	GND(FIXED)
A22	N/C	B22	N/C	C22	PCIE_RX7+	D22	PCIE_TX7+
A23	N/C	B23	N/C	C23	PCIE_RX7-	D23	PCIE_TX7-
A24	SUS_S5#	B24	PWR_OK	C24	DDI1_HPD	D24	GND
A25	N/C	B25	N/C	C25	SML0_CLK	D25	GND
A26	N/C	B26	N/C	C26	SML0_DAT	D26	DDI1_PAIR0+
A27	BATLOW#	B27	WDT	C27	SML1_CLK	D27	DDI1_PAIR0-
A28	(S)ATA_ACT#	B28	AC/HDA_SDIN2	C28	SML1_DAT	D28	GND
A29	AC/HDA_SYNC	B29	AC/HDA_SDIN1	C29	USB4_PD_I2C_CLK	D29	DDI1_PAIR1+
A30	AC/HDA_RST#	B30	AC/HDA_SDIN0	C30	USB4_PD_I2C_DAT	D30	DDI1_PAIR1-
A31	GND(FIXED)	B31	GND(FIXED)	C31	GND(FIXED)	D31	GND(FIXED)
A32	AC/HDA_BITCLK	B32	SPKR	C32	DDI2_CTRLCLK_AUX+	D32	DDI1_PAIR2+
A33	AC/HDA_SDOUT	B33	I2C_CK	C33	DDI2_CTRLCLK_AUX-	D33	DDI1_PAIR2-
A34	BIOS_DIS0#	B34	I2C_DAT	C34	DDI2_DDC_AUX_Y_SEL	D34	DDI1_DDC_AUX_Y_SEL
A35	THRMTRIP#	B35	THRM#	C35	DDI2_CLK	D35	DDI2_DATA
A36	USB6-	B36	USB7-	C36	DDI3_CTRLCLK_AUX+	D36	DDI1_PAIR3+
A37	USB6+	B37	USB7+	C37	DDI3_CTRLCLK_AUX-	D37	DDI1_PAIR3-
A38	USB_6_7_OC#	B38	USB_4_5_OC#	C38	DDI3_DDC_AUX_Y_SEL	D38	GND
A39	USB4-	B39	USB5-	C39	DDI3_PAIR0+	D39	DDI2_PAIR0+

A40	USB4+	B40	USB5+	C40	DDI3_PAIR0-	D40	DDI2_PAIR0-
A41	GND(FIXED)	B41	GND(FIXED)	C41	GND(FIXED)	D41	GND(FIXED)
A42	USB2-	B42	USB3-	C42	DDI3_PAIR1+	D42	DDI2_PAIR1+
A43	USB2+	B43	USB3+	C43	DDI3_PAIR1-	D43	DDI2_PAIR1-
A44	USB_2_3_OC#	B44	USB_0_1_OC#	C44	DDI3_HPD	D44	DDI2_HPD
A45	USB0-	B45	USB1-	C45	N/C	D45	GND
A46	USB0+	B46	USB1+	C46	DDI3_PAIR2+	D46	DDI2_PAIR2+
A47	VCC_RTC	B47	ESPI_EN#	C47	DDI3_PAIR2-	D47	DDI2_PAIR2-
A48	RSMRST_OUT#	B48	USB0_HOST_PPSNT	C48	N/C	D48	GND
A49	GBE0_SDP	B49	SYS_RESET#	C49	DDI3_PAIR3+	D49	DDI2_PAIR3+
A50	LPC_SERIRQ	B50	CB_RESET#	C50	DDI3_PAIR3-	D50	DDI2_PAIR3-
A51	GND(FIXED)	B51	GND(FIXED)	C51	GND(FIXED)	D51	GND(FIXED)
A52	PCIE_TX5+	B52	PCIE_RX5+	C52	PEG_RX0+	D52	PEG_TX0+
A53	PCIE_TX5-	B53	PCIE_RX5-	C53	PEG_RX0-	D53	PEG_TX0-
A54	GPI0	B54	GPO1	C54	TYPE0#	D54	PEG_LANE_K_V#
A55	PCIE_TX4+	B55	PCIE_RX4+	C55	PEG_RX1+	D55	PEG_TX1+
A56	PCIE_TX4-	B56	PCIE_RX4-	C56	PEG_RX1-	D56	PEG_TX1-
A57	GND	B57	GPO2	C57	TYPE1#	D57	TYPE2#
A58	PCIE_TX3+	B58	PCIE_RX3+	C58	PEG_RX2+	D58	PEG_TX2+
A59	PCIE_TX3-	B59	PCIE_RX3-	C59	PEG_RX2-	D59	PEG_TX2-
A60	GND(FIXED)	B60	GND(FIXED)	C60	GND(FIXED)	D60	GND(FIXED)
A61	PCIE_TX2+	B61	PCIE_RX2+	C61	PEG_RX3+	D61	PEG_TX3+
A62	PCIE_TX2-	B62	PCIE_RX2-	C62	PEG_RX3-	D62	PEG_TX3-
A63	GPI1	B63	GPO3	C63	GND	D63	GND
A64	PCIE_TX1+	B64	PCIE_RX1+	C64	GND	D64	GND
A65	PCIE_TX1-	B65	PCIE_RX1-	C65	N/C	D65	N/C
A66	GND	B66	WAKE0#	C66	N/C	D66	N/C
A67	GPI2	B67	WAKE1#	C67	RAPID_SHUTDOW_N	D67	GND
A68	PCIE_TX0+	B68	PCIE_RX0+	C68	N/C	D68	N/C
A69	PCIE_TX0-	B69	PCIE_RX0-	C69	N/C	D69	N/C
A70	GND(FIXED)	B70	GND(FIXED)	C70	GND(FIXED)	D70	GND(FIXED)
A71	LVDS_A0+/eDP_IY2+	B71	LVDS_B0+	C71	N/C	D71	N/C
A72	LVDS_A0-/eDP_IY2-	B72	LVDS_B0-	C72	N/C	D72	N/C
A73	LVDS_A1+/eDP_IY1+	B73	LVDS_B1+	C73	GND	D73	GND
A74	LVDS_A1-/eDP_IY1-	B74	LVDS_B1-	C74	N/C	D74	N/C
A75	LVDS_A2+/eDP_IY0+	B75	LVDS_B2+	C75	N/C	D75	N/C
A76	LVDS_A2-/eDP_IY0-	B76	LVDS_B2-	C76	GND	D76	GND
A77	LVDS_VDD_LV/eDP_VDD_EN	B77	LVDS_B3+	C77	GND	D77	GND
A78	LVDS_A3+	B78	LVDS_B3-	C78	PEG_RX8+	D78	PEG_TX8+
A79	LVDS_A3-	B79	LVDS_BKLT_EN/eDP_BKLT	C79	PEG_RX8-	D79	PEG_TX8-
A80	GND(FIXED)	B80	GND(FIXED)	C80	GND(FIXED)	D80	GND(FIXED)
A81	LVDS_A_CK+	B81	LVDS_B_CK+	C81	PEG_RX9+	D81	PEG_TX9+
A82	LVDS_A_CK-	B82	LVDS_B_CK-	C82	PEG_RX9-	D82	PEG_TX9-
A83	LVDS_I2C_CK/eDP_AUX+	B83	LVDS_BKLT_CTR/eDP_BKLT	C83	GND	D83	GND
A84	LVDS_I2C_DATA/eDP_AUX-	B84	VCC_5V_SBY	C84	GND	D84	GND

A84	LVDS_I2C_DAT/e DP_AUX	B84	VCC_5V_SBY	C84	GND	D84	GND
A85	GPI3	B85	VCC_5V_SBY	C85	PEG_RX10+	D85	PEG_TX10+
A86	N/C	B86	VCC_5V_SBY	C86	PEG_RX10-	D86	PEG_TX10-
A87	eDP_HPD	B87	VCC_5V_SBY	C87	GND	D87	GND
A88	PCIE_CLK_REF+	B88	BIOS_DIS1#	C88	PEG_RX11+	D88	PEG_TX11+
A89	PCIE_CLK_REF-	B89	VGA_RED	C89	PEG_RX11-	D89	PEG_TX11-
A90	GND(FIXED)	B90	GND(FIXED)	C90	GND(FIXED)	D90	GND(FIXED)
A91	SPI_POWER	B91	VGA_GRN	C91	N/C	D91	N/C
A92	SPI_MISO	B92	VGA_BLU	C92	N/C	D92	N/C
A93	GPO0	B93	VGA_HSYNC	C93	GND	D93	GND
A94	SPI_CLK	B94	VGA_VSYNC	C94	N/C	D94	N/C
A95	SPI_MOSI	B95	VGA_I2C_CK	C95	N/C	D95	N/C
A96	N/C	B96	VGA_I2C_DAT	C96	GND	D96	GND
A97	TYPE10#	B97	SPI_CS#	C97	GND	D97	GND
A98	SER0_TX	B98	N/C	C98	N/C	D98	N/C
A99	SER0_RX	B99	N/C	C99	N/C	D99	N/C
A100	GND(FIXED)	B100	GND(FIXED)	C100	GND(FIXED)	D100	GND(FIXED)
A101	SER1_TX	B101	FAN_PWNOUT	C101	N/C	D101	N/C
A102	SER1_RX	B102	FAN_TACHIN	C102	N/C	D102	N/C
A103	LID#	B103	SLEEP#	C103	GND	D103	GND
A104	VCC_12V	B104	VCC_12V	C104	VCC_12V	D104	VCC_12V
A105	VCC_12V	B105	VCC_12V	C105	VCC_12V	D105	VCC_12V
A106	VCC_12V	B106	VCC_12V	C106	VCC_12V	D106	VCC_12V
A107	VCC_12V	B107	VCC_12V	C107	VCC_12V	D107	VCC_12V
A108	VCC_12V	B108	VCC_12V	C108	VCC_12V	D108	VCC_12V
A109	VCC_12V	B109	VCC_12V	C109	VCC_12V	D109	VCC_12V
A110	GND(FIXED)	B110	GND(FIXED)	C110	GND(FIXED)	D110	GND(FIXED)

Table 1 PCOM-B659 Pin-Out

3 COM Express Interface

3.1 PCIe / PEG

PCOM-B659 PCIe

Pin#	Pin Name	COMe 3.0/3.1 Specification (Signals Requiring Module Termination)	Pin Typ	B659 Module	Pwr Rail /Tolerance(Volt)
B68	PCIE_RX0+	AC coupled off the Module.	I PCIE	PCH to Com Express Row connector.	AC coupled off Module
B69	PCIE_RX0-				
B64	PCIE_RX1+				
B65	PCIE_RX1-				
B61	PCIE_RX2+				
B62	PCIE_RX2-				
B58	PCIE_RX3+				
B59	PCIE_RX3-				
B55	PCIE_RX4+				
B56	PCIE_RX4-				
B52	PCIE_RX5+				
B53	PCIE_RX5-				
C19	PCIE_RX6+				
C20	PCIE_RX6-				
C22	PCIE_RX7+				
C23	PCIE_RX7-				
A68	PCIE_TX0+	AC coupled on the Module	O PCIE	0.22uF AC coupled on the Module(Gen3).	AC coupled on Module
A69	PCIE_TX0-				
A64	PCIE_TX1+				
A65	PCIE_TX1-				
A61	PCIE_TX2+				
A62	PCIE_TX2-				
A58	PCIE_TX3+				
A59	PCIE_TX3-				
A55	PCIE_TX4+				
A56	PCIE_TX4-				
A52	PCIE_TX5+				
A53	PCIE_TX5-				
D19	PCIE_TX6+				
D20	PCIE_TX6-				

Table 2 B659 PCI Express Lanes Signals, Pin Types, and Descriptions

Pin#	Pin Name	COMe 3.0/3.1 Specification (Signals Requiring Module Termination)	Pin Typ	B659 Module	Pwr Rail /Tolerance(Volt)
C52	PEG_RX0+	AC coupled off Module.	I PCIE	AC coupled off Module.	AC coupled off Module
C53	PEG_RX0-				
C55	PEG_RX1+				
C56	PEG_RX1-				
C58	PEG_RX2+				
C59	PEG_RX2-				
C61	PEG_RX3+				
C62	PEG_RX3-				
C78	PEG_RX8+				
C79	PEG_RX8-				
C81	PEG_RX9+				
C82	PEG_RX9-				
C85	PEG_RX10+				
C86	PEG_RX10-				
C88	PEG_RX11+				
C89	PEG_RX11-				

Pin#	Pin Name	COMe 3.0/3.1 Specification (Signals Requiring Module Termination)	Pin Typ	B659 Module	Pwr Rail /Tolerance(Volt)
D52	PEG_TX0+	AC coupled on Module.	O PCIE	0.22uF AC coupled on the Module(Gen3).	AC coupled on Module
D53	PEG_TX0-				
D55	PEG_TX1+				
D56	PEG_TX1-				
D58	PEG_TX2+				
D59	PEG_TX2-				
D61	PEG_TX3+				
D62	PEG_TX3-				
D78	PEG_TX8+				
D79	PEG_TX8-				
D81	PEG_TX9+				
D82	PEG_TX9-				
D85	PEG_TX10+				
D86	PEG_TX10-				
D88	PEG_TX11+				
D89	PEG_TX11-				

Table 3 B659 PEG Signals, Pin Types, and Descriptions

Pin#	Pin Name	COMe 3.0/3.1 Specification (Signals Requiring Module Termination)	Pin Typ	B659 Module	Pwr Rail /Tolerance(Volt)
D54	PEG_LANE_ RV#		I CMOS	PU 1k ohm to V3P3S .	3.3V / 3.3V
A88	PCIE_CLK_ REF+		O PCIE	PCH to Com Express Row connector.	PCIE
A89	PCIE_CLK_ REF-		O PCIE	PCH to Com Express Row connector.	PCIE
B50	CB_RESET#		O CMOS	EC to Com Express Row connector.	3.3VSuspend/ 3.3V
B66	WAKE0#	Pulled up to 3.3V standby on module with a 10K resistor	I CMOS	PCH to Com Express Row connector.	3.3VSuspend/ 3.3V

Table 4 B659 PCI Express Lanes Signals, Pin Types, and Descriptions (2)

PCIE / PEG AC Coupling : Device Down

The diagram illustrates the connection between a COM Express Module and a PCIe Add-in Device. The COM Express Module is on the left, and the PCIe Add-in Device is on the right. They are connected via a Device Down interface. The connection is labeled "Device Down" and "COM Express Carrier Board". The COM Express Module has pins TX+, TX-, RX+, and RX-. The PCIe Add-in Device has pins RX+, RX-, TX+, and TX-. The connections are as follows: TX+ to RX+, TX- to RX-, RX+ to TX+, and RX- to TX-.

PCIE / PEG AC Coupling : Add-In Card



The diagram illustrates the connection between a COM Express Module and an Add-In Card. On the left, the COM Express Module is shown with a connector labeled TX+, TX-, RX+, and RX-. These pins are connected to a central Connector block. The Connector block is then connected to the Add-In Card, which has pins labeled RX+, RX-, TX+, and TX-. The Add-In Card is also connected to a PCIe Add-in Device. The entire system is housed within a COM Express Carrier Board.

Via design

Long via stub degrades overall signal integrity margin. Specific via stub length requirements may be defined within the interface design guideline chapters. For MS to SL/DSL routing recommendation on this platform, routing recommendation has covered via stub length as below.

- PEG <=10 mils
- DMI /DP/PCH IO <=25 mils

3.1.2 PCB layout guideline - PCIe/PEG

Parameter	PCIe Gen2	PCIe Gen3	PEG Gen4
Bandwidth	5 G	8 G	16 G
Maximum signal line length (coupled traces) TX and RX	12.0/10 inches	8 inches (Add In Card/ Device Down)	6.9 inches (Add In Card/ Device Down)
Differential impedance	85 Ω +/-15%	85 Ω +/-15%	85 Ω +/-15%
Single-ended Impedance	50 Ω +/-15%	50 Ω +/-15%	50 Ω +/-15%
Trace width (W)	3.5 mil PCB stack-up dependent	3.5 mil PCB stack-up dependent	3.5 mil PCB stack-up dependent
Spacing between differential pairs (intra-pair) (S)	15 mil PCB stack-up dependent	15 mil PCB stack-up dependent	15 mil PCB stack-up dependent
Spacing between RX and TX pairs (inter-pair) (s)	Min. 20mils	Min. 20mils	Min. 20mils
Length matching between differential pairs (intra-pair)	Max. 5mils	Max. 5mils	Max. 5mils
Reference plane	GND referenced preferred	GND referenced preferred	GND referenced preferred
Spacing from edge of plane	Min. 10*W mils (W=trace width)	Min. 10*W mils (W=trace width)	Min. 10*W mils (W=trace width)
Via Usage	Max. 2 vias per TX trace Max. 4 vias per RX trace	Max. 1 vias per TX trace Max. 1 vias per RX trace	Max. 1vias per TX trace Max.1 vias per RX trace

Table 5 PCIe/PEG Layout information

3.1.3 Passive Devices

AC Cap value (Gen1/Gen2/Gen4)	Min = 75nf Max = 265nf	PCOM-B659 AC Cap value 220nF
AC Cap value (Gen3)	Min = 176nf Max = 265nf	

Table 6 PCIe/PEG AC coupling capacitor value

3.1.4 Reference schematic - PCOM-C60B R0

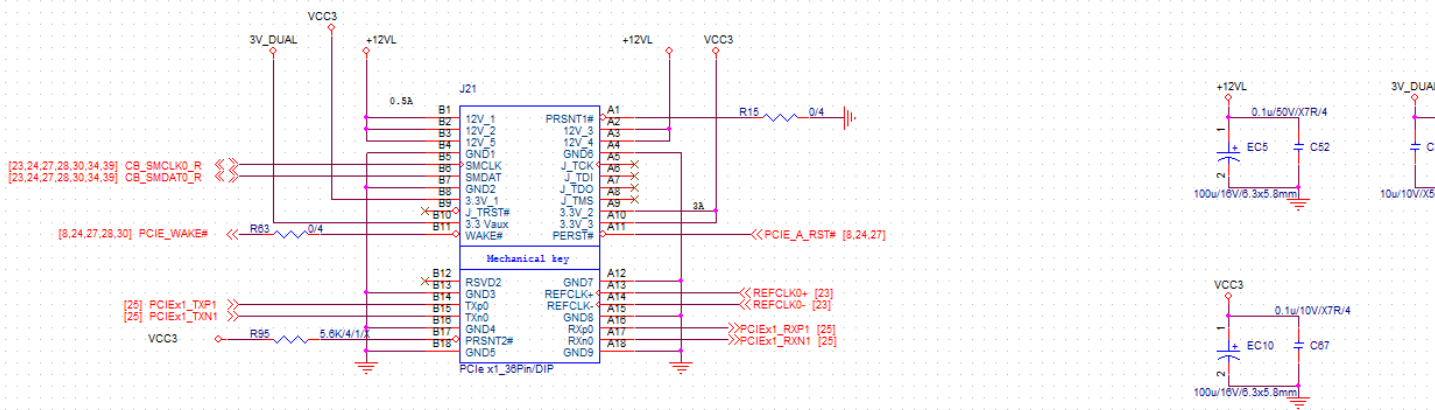


Figure 4 PCIe x1 reference schematic

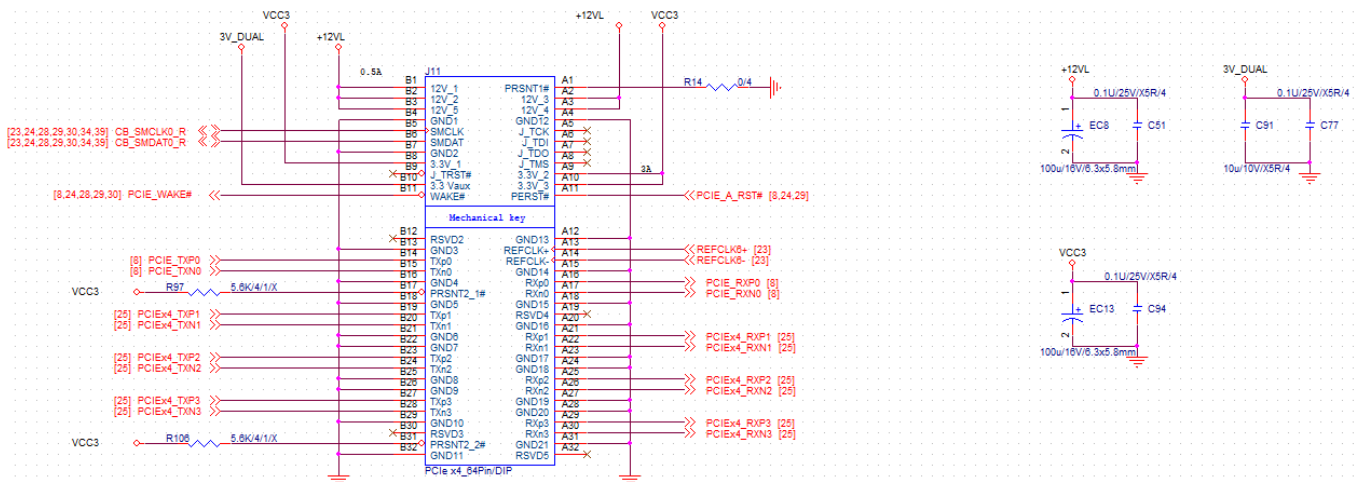
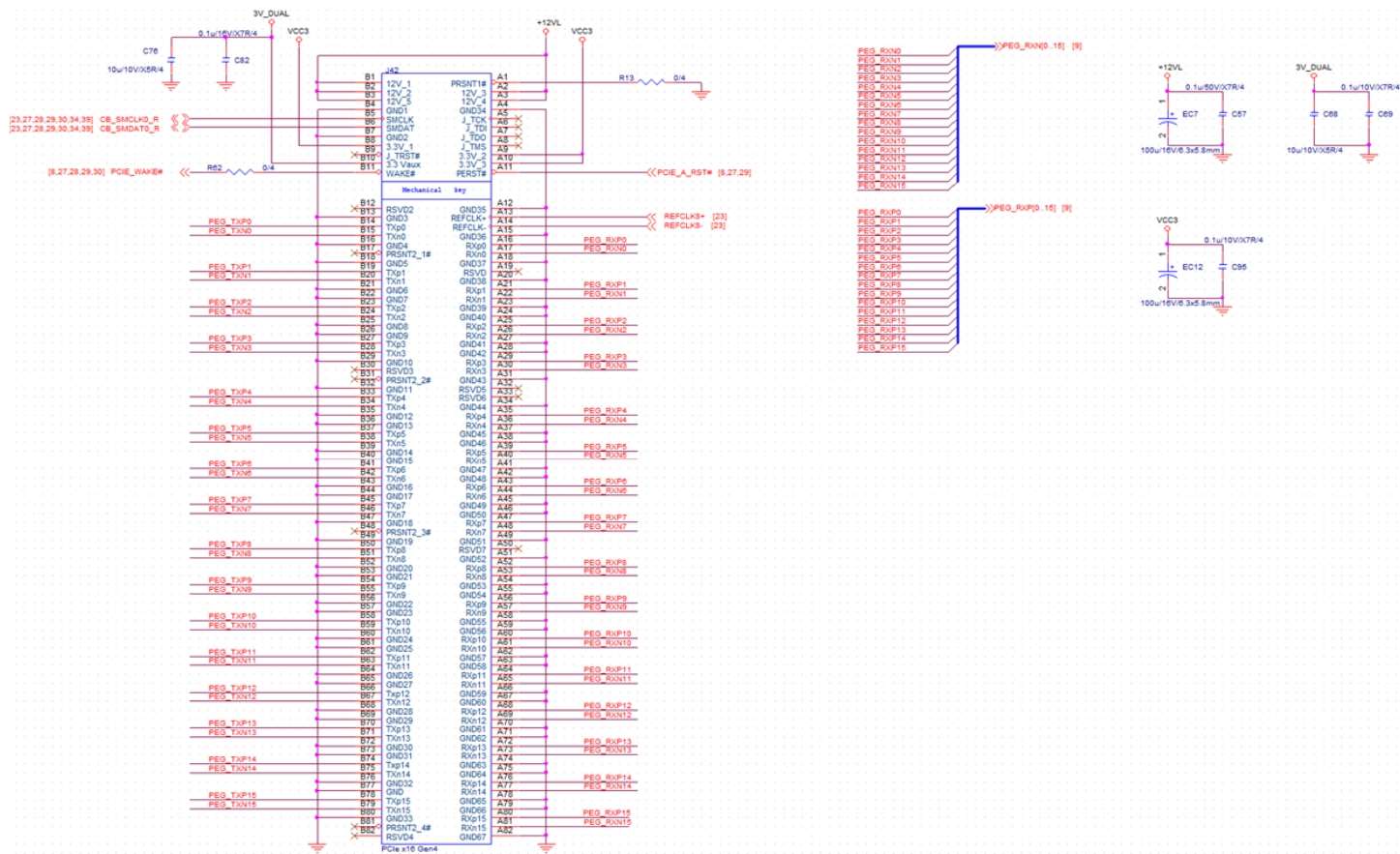


Figure 5 PCIe x4 reference schematic



3.1.5 Max trace length and available carrier trace length - PCIe

PIN	Name	Module Length	Max Length	Available Carrier length (Device Down Topology)
B68	PCIE_RXP0	1888.74	8000	6111.26
B69	PCIE_RXN0	1893.71	8000	6106.29
A68	PCIE_TXP0	2162.12	8000	5837.88
A69	PCIE_TXN0	2163.52	8000	5836.48
B64	PCIE_RXP1	2112.76	8000	5887.24
B65	PCIE_RXN1	2114.18	8000	5885.82
A64	PCIE_TXP1	2138.3	8000	5861.7
A65	PCIE_TXN1	2140.77	8000	5859.23
B61	PCIE_RXP2	1909.69	8000	6090.31
B62	PCIE_RXN2	1911.69	8000	6088.31
A61	PCIE_TXP2	2085.89	8000	5914.11
A62	PCIE_TXN2	2086.38	8000	5913.62
B58	PCIE_RXP3	1959.77	8000	6040.23
B59	PCIE_RXN3	1963.63	8000	6036.37
A58	PCIE_TXP3	2064.47	8000	5935.53
A59	PCIE_TXN3	2062.95	8000	5937.05
B55	PCIE_RXP4	1996.56	8000	6003.44
B56	PCIE_RXN4	1999.98	8000	6000.02
A55	PCIE_TXP4	2080.82	8000	5919.18
A56	PCIE_TXN4	2083.14	8000	5916.86
B52	PCIE_RXP5	1902.51	8000	6097.49
B53	PCIE_RXN5	1906.68	8000	6093.32
A52	PCIE_TXP5	2366.55	8000	5633.45
A53	PCIE_TXN5	2362.38	8000	5637.62
C19	PCIE_RXP6	3065.57	8000	4934.43
C20	PCIE_RXN6	3063.76	8000	4936.24
D19	PCIE_TXP6	3663.08	8000	4336.92
D20	PCIE_TXN6	3660.16	8000	4339.84
C22	PCIE_RXP7	2508.38	8000	5491.62
C23	PCIE_RXN7	2509.61	8000	5490.39
D22	PCIE_TXP7	2957.22	8000	5042.78
D23	PCIE_TXN7	2961.84	8000	5038.16

Table 7 PCIe carrier available traces - Device Down/Add In Card

3.1.6 Max trace length and available carrier trace length – PEG

PIN	Name	Module Length	Max Length	Available Carrier length (Device Down Topology)
C52	PEG_RX0+	1730.44	6900	5169.56
C53	PEG_RX0-	1726.55	6900	5173.45
D52	PEG_TX0+	1700.92	6900	5199.08
D53	PEG_TX0-	1696.97	6900	5203.03
C55	PEG_RX1+	1672.98	6900	5227.02
C56	PEG_RX1-	1671.41	6900	5228.59
D55	PEG_TX1+	1596.22	6900	5303.78
D56	PEG_TX1-	1597.64	6900	5302.36
C58	PEG_RX2+	2073.1	6900	4826.9
C59	PEG_RX2-	2072.59	6900	4827.41
D58	PEG_TX2+	1563.2	6900	5336.8
D59	PEG_TX2-	1563.42	6900	5336.58
C61	PEG_RX3+	2165.45	6900	4734.55
C62	PEG_RX3-	2166.32	6900	4733.68
D61	PEG_TX3+	1820.58	6900	5079.42
D62	PEG_TX3-	1816.85	6900	5083.15
C65	PEG_RX4+	N/C	6900	N/C
C66	PEG_RX4-	N/C	6900	N/C
D65	PEG_TX4+	N/C	6900	N/C
D66	PEG_TX4-	N/C	6900	N/C
C68	PEG_RX5+	N/C	6900	N/C
C69	PEG_RX5-	N/C	6900	N/C
D68	PEG_TX5+	N/C	6900	N/C
D69	PEG_TX5-	N/C	6900	N/C
C71	PEG_RX6+	N/C	6900	N/C
C72	PEG_RX6-	N/C	6900	N/C
D71	PEG_TX6+	N/C	6900	N/C
D72	PEG_TX6-	N/C	6900	N/C
C74	PEG_RX7+	N/C	6900	N/C
C75	PEG_RX7-	N/C	6900	N/C
D74	PEG_TX7+	N/C	6900	N/C
D75	PEG_TX7-	N/C	6900	N/C
C78	PEG_RX8+	2973.47	6900	3926.53
C79	PEG_RX8-	2976.88	6900	3923.12
D78	PEG_TX8+	2369.38	6900	4530.62

D79	PEG_TX8-	2367.65	6900	4532.35
C81	PEG_RX9+	2977.32	6900	3922.68
C82	PEG_RX9-	2981.61	6900	3918.39
D81	PEG_TX9+	2303.69	6900	4596.31
D82	PEG_TX9-	2301.97	6900	4598.03
C85	PEG_RX10+	2897.71	6900	4002.29
C86	PEG_RX10-	2902.26	6900	3997.74
D85	PEG_TX10+	2782.87	6900	4117.13
D86	PEG_TX10-	2782.56	6900	4117.44
C88	PEG_RX11+	2972.31	6900	3927.69
C89	PEG_RX11-	2974.69	6900	3925.31
D88	PEG_TX11+	2480.77	6900	4419.23
D89	PEG_TX11-	2480.21	6900	4419.79
C91	PEG_RX12+	N/C	6900	N/C
C92	PEG_RX12-	N/C	6900	N/C
D91	PEG_TX12+	N/C	6900	N/C
D92	PEG_TX12-	N/C	6900	N/C
C94	PEG_RX13+	N/C	6900	N/C
C95	PEG_RX13-	N/C	6900	N/C
D94	PEG_TX13+	N/C	6900	N/C
D95	PEG_TX13-	N/C	6900	N/C
C98	PEG_RX14+	N/C	6900	N/C
C99	PEG_RX14-	N/C	6900	N/C
D98	PEG_TX14+	N/C	6900	N/C
D99	PEG_TX14-	N/C	6900	N/C
C101	PEG_RX15+	N/C	6900	N/C
C102	PEG_RX15-	N/C	6900	N/C
D101	PEG_TX15+	N/C	6900	N/C
D102	PEG_TX15-	N/C	6900	N/C

Table 8 PEG carrier available traces - Device Down/Add In Card

3.2 USB 2.0/3.0

PCOM-B659 USB2.0

Pin#	Pin Name	COMe 3.0/3.1 Specification Specification (Signals Requiring Module Termination)	Pin Typ	B659 Module	Pwr Rail /Tolerance(Vo lt)
A45	USB0-	No termination is required on USB pairs.	I/O USB	PCH to Com Express Row connector.	3.3V Suspend/3.3V
A46	USB0+				
B45	USB1-				
B46	USB1+				
A42	USB2-				
A43	USB2+				
B42	USB3-				
B43	USB3+				
A39	USB4-				
A40	USB4+				
B39	USB5-				
B40	USB5+				
A36	USB6-				
A37	USB6+				
B36	USB7-				
B37	USB7+				
B44	USB_0_1_ OC#	Pulled up to 3.3V standby on module with a 10K Ω resistor	I CMOS	EC to Com Express Row connector.	3.3V Suspend/ 3.3V
A44	USB_2_3_ OC#			PU 10k ohm to V3P3A .	
B38	USB_4_5_ OC#				
A38	USB_6_7_ OC#				

Table 9 B659 USB 2.0

PCOM-B659 USB3.2

Pin#	Pin Name	COMe 3.0/3.1 Specification Specification (Signals Requiring Module Termination)	Pin Typ	B659 Module	Pwr Rail /Tolerance(Volt)
C3	USB_SSRX0-	AC coupled off Module.	I PCIE	PCH to Com Express Row connector.	AC coupled off Module.
C4	USB_SSRX0+				
C6	USB_SSRX1-				
C7	USB_SSRX1+				
C9	USB_SSRX2-				
C10	USB_SSRX2+				
C12	USB_SSRX3-				
C13	USB_SSRX3+				
D3	USB_SSTX0-	AC coupled on Module.	O PCIE	0.22uF AC coupled on the Module.	AC coupled on Module
D4	USB_SSTX0+				
D6	USB_SSTX1-				
D7	USB_SSTX1+				
D9	USB_SSTX2-				
D10	USB_SSTX2+				
D12	USB_SSTX3-				
D13	USB_SSTX3+				
B48	USB0_HOST_P RSNT	Pulled down to 3.3V standby on module with a 47K Ω resistor	I CMOS	PD 10k ohm to GND.	3.3V Suspend/ 3.3V
A48	RSMRST_OUT#		O CMOS CMOS		3.3V Suspend/ 3.3V

Table 10 B659 USB 3.2

3.2.1 PCB layout guideline - USB2.0/3.2

Parameter	Trace Routing	Trace Routing
Transfer rate / Port	480 Mbit/s	5.0 GBit/s
Maximum signal line length (coupled traces)	Std PCB :Max. 10.0 inches	Std PCB 7.5 inches
Differential Impedance	85 Ω +/-15%	85 Ω +/-15%
Single-ended Impedance	50 Ω +/-15%	50 Ω +/-15%
Trace width (W)	3.5 mil PCB stack-up dependent	3.5 mil PCB stack-up dependent
Spacing between differential pairs (intra-pair) (S)	4 mil PCB stack-up dependent	4mil PCB stack-up dependent
Spacing between pairs-to-pairs (inter-pair) (s)	Min. 15mils	Min. 15mils
Spacing between differential pairs and high-speed periodic signals	Min. 15mils	Min. 15mils
Spacing between differential pairs and low-speed non periodic signals	Min. 20mils	Min. 20mils
Length matching between differential pairs (intra-pair)	5 mils	5 mils
Reference plane	GND referenced preferred	GND
Spacing from edge of plane	Min. 10*W mils (W=trace width)	Min. 10*W mils (W=trace width)
Via Usage	Max. 1 vias	Max. 1 vias

Table 11 USB 2.0 / 3.2 Layout information

3.2.2 Reference schematic - PCOM-C60B R0

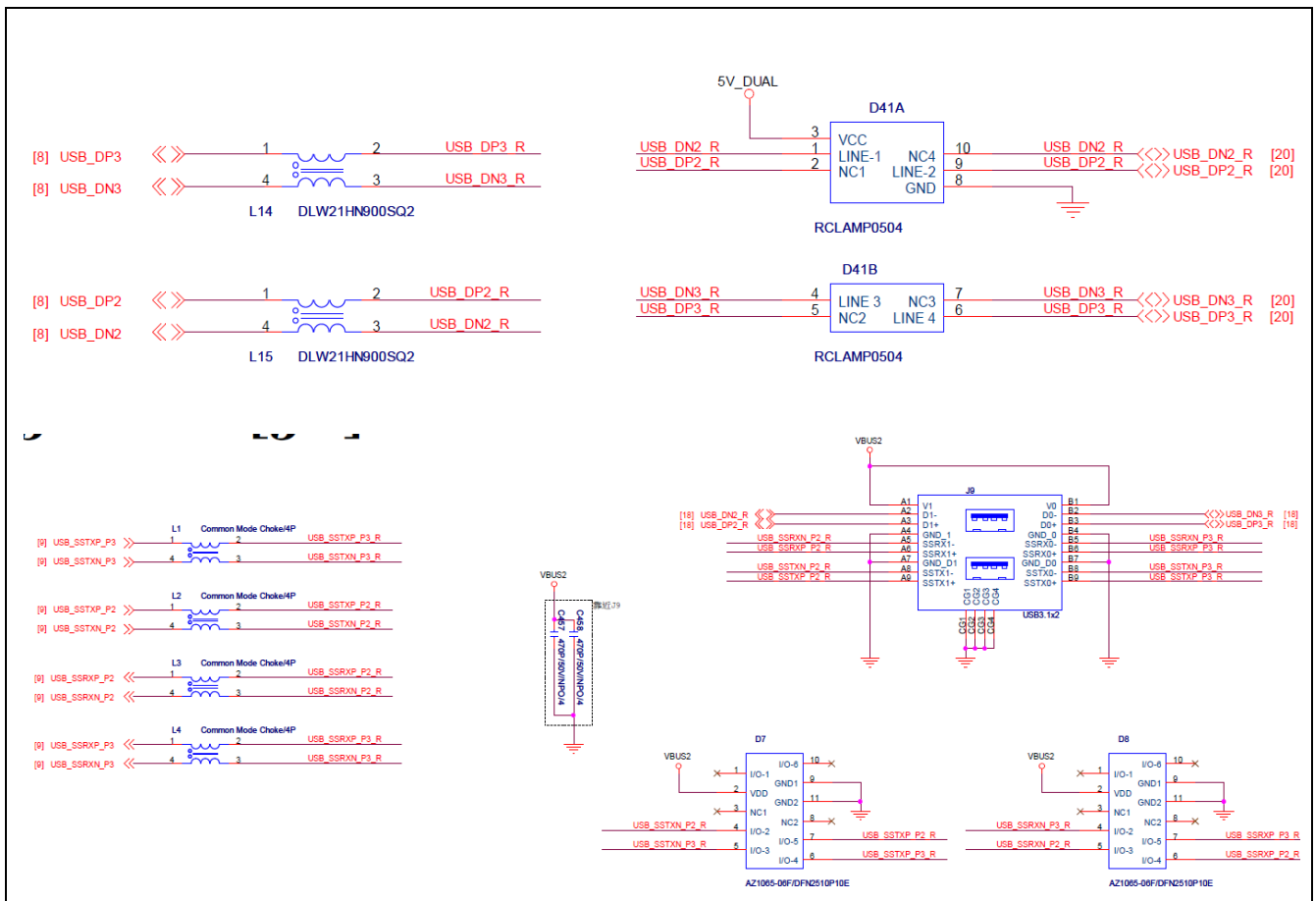


Figure 7 USB 2.0 / 3.2 Reference schematic 1

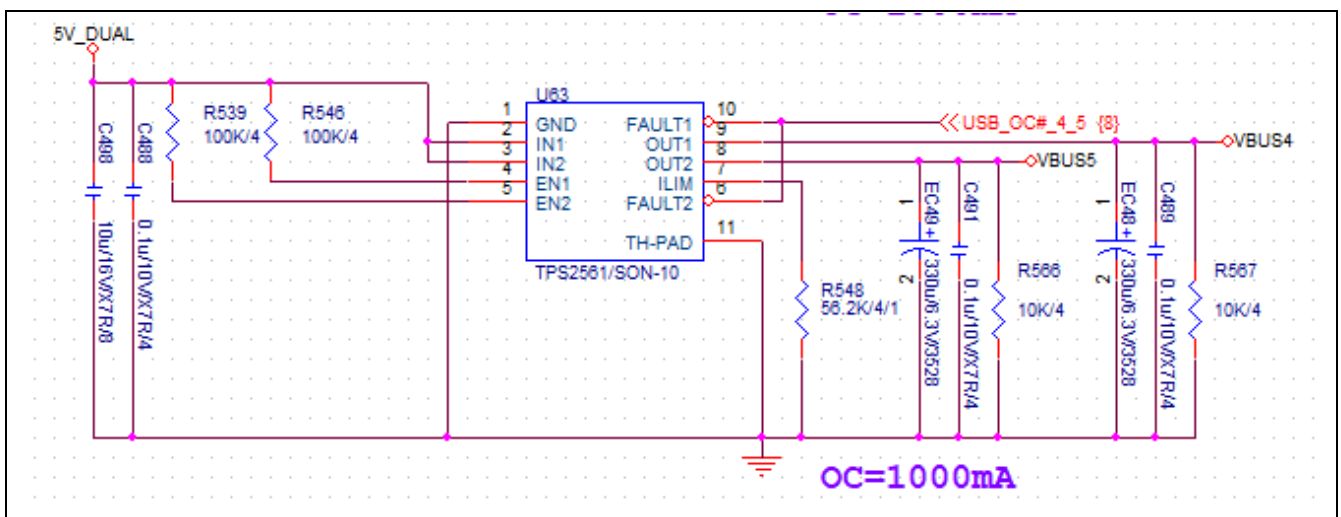


Figure 8 USB 2.0/3.2 Reference schematic 2

3.2.3 Max trace length and available carrier trace length - USB 2.0 / 3.2

PIN	Name	Module Length	Max Length	Available Carrier length
A45	USB_PN0	2492.84	10000	7507.16
A46	USB_PP0	2492.52	10000	7507.48
B45	USB_PN1	2458.94	10000	7541.06
B46	USB_PP1	2458.29	10000	7541.71
A42	USB_PN2	2790.1	10000	7209.9
A43	USB_PP2	2785.85	10000	7214.15
B42	USB_PN3	2431.49	10000	7568.51
B43	USB_PP3	2431.61	10000	7568.39
A39	USB_PN4	2886.59	10000	7113.41
A40	USB_PP4	2882.55	10000	7117.45
B39	USB_PN5	2297.25	10000	7702.75
B40	USB_PP5	2299.53	10000	7700.47
A36	USB_PN6	2654.27	10000	7345.73
A37	USB_PP6	2652.26	10000	7347.74
B36	USB_PN7	2377.28	10000	7622.72
B37	USB_PP7	2377.94	10000	7622.06
D4	USB_SSTX0+	3663.87	7500	3836.13
D3	USB_SSTX0-	3660.56	7500	3839.44
D7	USB_SSTX1+	3331.22	7500	4168.78
D6	USB_SSTX1-	3331.1	7500	4168.9
D10	USB_SSTX2+	3466.19	7500	4033.81
D9	USB_SSTX2-	3469.38	7500	4030.62
D13	USB_SSTX3+	3263.91	7500	4236.09
D12	USB_SSTX3-	3266.41	7500	4233.59
C4	USB_SSRX0+	3565.97	7500	3934.03
C3	USB_SSRX0-	3561.36	7500	3938.64
C7	USB_SSRX1+	3127.91	7500	4372.09
C6	USB_SSRX1-	3126.9	7500	4373.1
C10	USB_SSRX2+	3305.09	7500	4194.91
C9	USB_SSRX2-	3306.3	7500	4193.7
C13	USB_SSRX3+	3014.79	7500	4485.21
C12	USB_SSRX3-	3018.22	7500	4481.78

Table 12 USB2.0 / 3.2 carrier available traces

3.3 DDI

PCOM-B659 DDI1

Pin#	Pin Name	COMe 3.0/3.1 Specification Specification (Signals Requiring Module Termination)	Pin Typ	B659 Module	Pwr Rail /Tolerance(Volt)
D26	DDI1_PAIR0+	AC coupled off Module.	O LV_DIFF	AC coupled off Module.	AC coupled off Module
D27	DDI1_PAIR0-				
D29	DDI1_PAIR1+				
D30	DDI1_PAIR1-				
D32	DDI1_PAIR2+				
D33	DDI1_PAIR2-				
D36	DDI1_PAIR3+				
D37	DDI1_PAIR3-				
D15	DDI1_CTRLCLK_ AUX+		I/O LV_DIFF	1.Module follow COM Express Spec Figure 4-7: Dual-Mode COM Express Module Implementation	AC coupled on Module
			I/O OD CMOS		3.3V / 3.3V
D16	DDI1_CTRLDATA _AUX-		I/O PCIE		AC coupled on Module
			I/O OD CMOS		3.3V / 3.3V
D34	DDI1_DDC_AUX _SEL	1M pull-down to logic ground on the Module	I CMOS	1M pull-down to GND on the Module	3.3V / 3.3V
C24	DDI1_HPD		I CMOS	Follow INTEL SKL PDG : PD 100k ohm to GND	3.3V / 3.3V

Table 13 B659 DDI1

PCOM-B659 DDI2

Pin#	Pin Name	COMe 3.0/3.1 Specification Specification (Signals Requiring Module Termination)	Pin Typ	B659 Module	Pwr Rail /Tolerance(Volt)
D39	DDI2_PAIR0+	AC coupled off Module.	O LV_DIFF	AC coupled off Module.	AC coupled off Module
D40	DDI2_PAIR0-				
D42	DDI2_PAIR1+				
D43	DDI2_PAIR1-				
D46	DDI2_PAIR2+				
D47	DDI2_PAIR2-				
D49	DDI2_PAIR3+				
D50	DDI2_PAIR3-				
C32	DDI2_CTRLCLK_A UX+		I/O LV_DIFF	1.Module flow COM Express Spec Figure 4-1: Dual-Mode COM Express Module Implementation	AC coupled on Module
			I/O OD CMOS		3.3V / 3.3V
C33	DDI2_CTRLDATA_ AUX-		I/O PCIE		AC coupled on Module
			I/O OD CMOS		3.3V / 3.3V
C34	DDI2_DDC_AUX_S EL	1M pull-down to logic ground on the Module	I CMOS	1M pull-down to GND on the Module.	3.3V / 3.3V
D44	DDI2_HPD		I CMOS	Follow INTEL SKL PDG : PD 100k ohm to GND	3.3V / 3.3V

Table 14 B659 DDI2

PCOM-B659 DDI3

Pin#	Pin Name	COMe 3.0/3.1 Specification Specification (Signals Requiring Module Termination)	Pin Typ	B659 Module	Pwr Rail /Tolerance(Volt)
C39	DDI3_PAIR0+	AC coupled off Module.	O LV_DIFF	AC coupled off Module.	AC coupled off Module
C40	DDI3_PAIR0-				
C42	DDI3_PAIR1+				
C43	DDI3_PAIR1-				
C46	DDI3_PAIR2+				
C47	DDI3_PAIR2-				
C49	DDI3_PAIR3+				
C50	DDI3_PAIR3-				
C36	DDI3_CTRLCLK_A UX+		O LV_DIFF	1.Module flow COM Express Spec Figure 4-1: Dual-Mode COM Express Module Implementation	AC coupled on Module
			I/O OD CMOS		3.3V / 3.3V
C37	DDI3_CTRLDATA_ AUX-		I/O PCIE		AC coupled on Module
			I/O OD CMOS		3.3V / 3.3V
C38	DDI3_DDC_AUX_S EL	1M pull-down to logic ground on the Module	I CMOS	1M pull-down to GND on the Module.	3.3V / 3.3V
C44	DDI3_HPD			Follow INTEL SKL PDG : PD 100k ohm to GND	

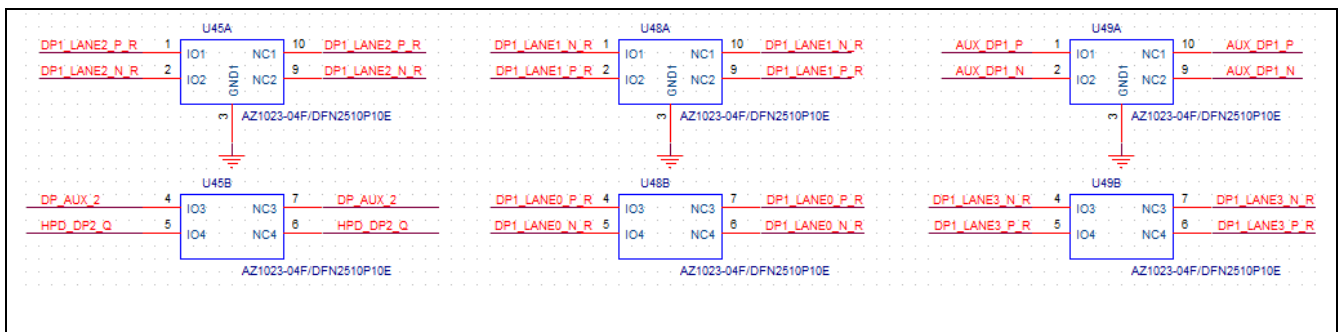
Table 17 B659 DDI3

3.3.1 PCB layout guideline - DDI (DP)

Parameter	Trace Routing
Transfer Rate	Max. 5.94 Gbit/s
Maximum signal line length (coupled traces)	10 inches
Differential Impedance	85 Ω +/-15%
Single-ended Impedance	50 Ω +/-15%
Trace width (W)	3.5 mil PCB stack-up dependent
Spacing between differential pairs (intra-pair) (S)	4mil PCB stack-up dependent
Spacing between pairs-to-pair	Min. 15mils
Spacing between differential pairs and high-speed periodic signals	Min. 15mils
Spacing between differential pairs and low-speed non periodic signals	Min. 15mils
Length matching between differential pairs (intra-pair)	Max. 5 mils
Spacing from edge of plane	Min. 10*W mils (W=trace width)
Via Usage	Max. 1
AC coupling capacitors	100nF

Table 18 DDI Layout information

3.3.2 Reference schematic - PCOM-C60B R0



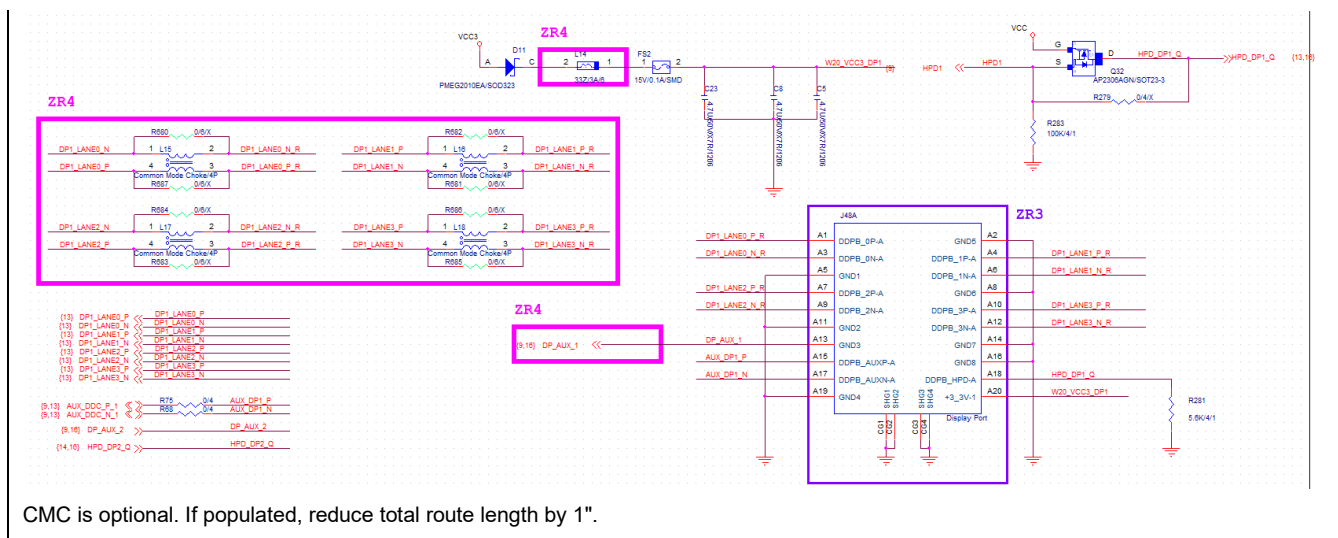


Figure 9 Reference schematic - DDI

3.3.3 Max trace length and available carrier trace length -

DDI

PIN	Name	Module Length	Max Length	Available Carrier length
D26	DDI1_PAIR0+	1620.67	10000	8379.33
D27	DDI1_PAIR0-	1618.97	10000	8381.03
D29	DDI1_PAIR1+	1587.83	10000	8412.17
D30	DDI1_PAIR1-	1586.66	10000	8413.34
D32	DDI1_PAIR2+	1641.04	10000	8358.96
D33	DDI1_PAIR2-	1636.37	10000	8363.63
D36	DDI1_PAIR3+	1633.21	10000	8366.79
D37	DDI1_PAIR3-	1631.03	10000	8368.97
D39	DDI2_PAIR0+	928.07	10000	9071.93
D40	DDI2_PAIR0-	927.52	10000	9072.48
D42	DDI2_PAIR1+	970.57	10000	9029.43
D43	DDI2_PAIR1-	970.81	10000	9029.19
D46	DDI2_PAIR2+	971.82	10000	9028.18
D47	DDI2_PAIR2-	972.6	10000	9027.4
D49	DDI2_PAIR3+	1162.71	10000	8837.29
D50	DDI2_PAIR3-	1160.51	10000	8839.49
C39	DDI3_PAIR0+	1228.42	10000	8771.58
C40	DDI3_PAIR0-	1225.14	10000	8774.86

C42	DDI3_PAIR1+	1261.36	10000	8738.64
C43	DDI3_PAIR1-	1263.7	10000	8736.3
C46	DDI3_PAIR2+	1220.2	10000	8779.8
C47	DDI3_PAIR2-	1216.96	10000	8783.04
C49	DDI3_PAIR3+	1276.63	10000	8723.37
C50	DDI3_PAIR3-	1280.45	10000	8719.55

Table 19 Carrier available traces - DDI

3.4 LAN

PCOM-B659 LAN

Pin#	Pin Name	COMe 3.0/3.1 Specification Specification (Signals Requiring Module Termination)	Pin Typ	B659 Module	Pwr Rail /Tolerance(Volt)
A12	GBE0_MDI0-		I/O MDI	Media Dependent Interface signal. I226 PHY chip on Module.	Less than 3.3V May be active in Suspend Suspend
A13	GBE0_MDI0+				
A9	GBE0_MDI1-				
A10	GBE0_MDI1+				
A6	GBE0_MDI2-				
A7	GBE0_MDI2+				
A2	GBE0_MDI3-				
A3	GBE0_MDI3+				
A8	GBE0_LINK#		OD CMOS	Gigabit Ethernet Controller 0 link indicator, active low.	3.3V Suspend/3.3V
A4	GBE0_LINK_1000#		OD(I/O) CMOS	Indicate 1Gbe signal speed.	3.3V Suspend/3.3V
A5	GBE0_LINK_2500#		OD(I/O) CMOS	Indicate 2.5Gbe signal speed.	3.3V Suspend/3.3V
A14	GBE0_CTREF(N/C)		REF		GND min 3.3V max
B2	GBE0_ACT#		OD(I/O) COMS	I226 PHY chip to Com Express Row connector.	3.3V Suspend/3.3V
A49	GBE0_SDP		I/O	I226 PHY chip to	3.3V Suspend

			CMOS	Com Express Row connector.	/3.3V
--	--	--	------	----------------------------	-------

Table 20 B659 LAN

RJ45 LED State for B659(ZR0):

Speed LED	
10Mbps	OFF
100Mbps	OFF
1000Mbps	Yellow
2500Mbps	Green
Link-Activity LED	
Link-up	Green
Tx/Rx Activity	Blinking Green

3.4.1 PCB layout guideline - LAN

Parameter	Trace Routing
Differential Impedance	100 Ω +/-10%
Single-ended Impedance	50 Ω +/-10%
Trace width (W)	4 mil PCB stack-up dependent
Spacing between differential pairs (intra-pair) (S)	9 mil PCB stack-up dependent
Spacing between RX and TX pairs (inter-pair) (s)	Min. 28 mils
Length matching between RX and TX pairs (inter-pair)	Max. 10mils
Spacing from edge of plane	Min. 10*W mils (W=trace width)

Table 15 LAN Layout information

3.4.2 Reference schematic – for 2.5G LAN

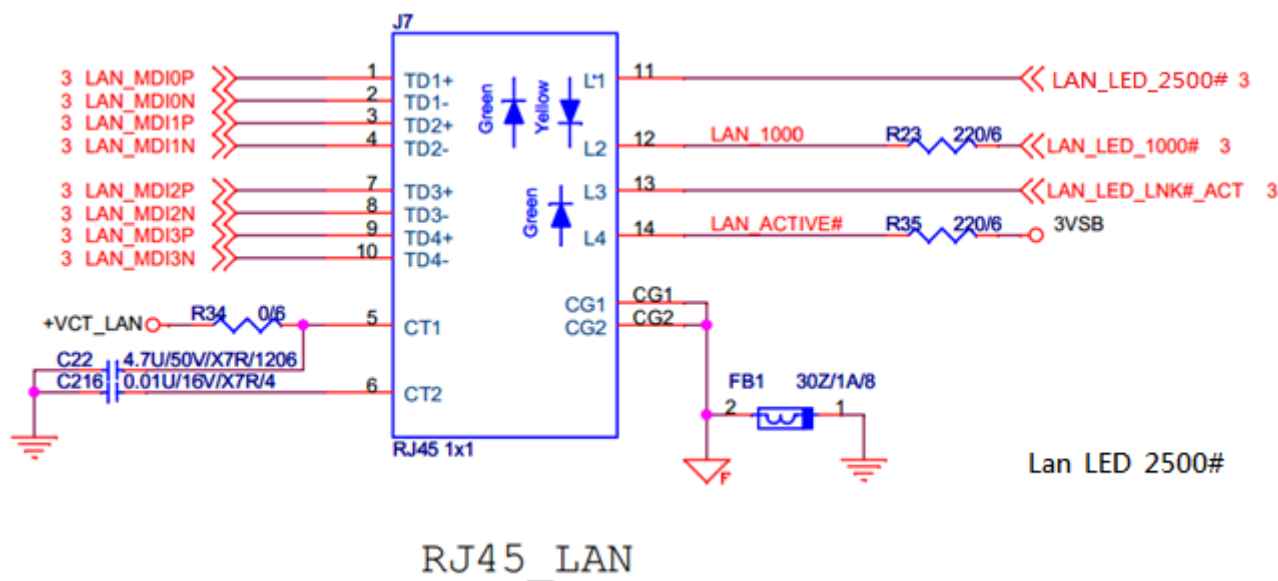


Figure 10 Reference schematic – LAN

3.4.3 Max trace length and available carrier trace length -

LAN

PIN	Name	Module Length	Max Length	Available Carrier length
A13	GBE0_MDI0+	592.68	4000	3407.32
A12	GBE0_MDI0-	589.59	4000	3410.41
A10	GBE0_MDI1+	617.05	4000	3382.95
A9	GBE0_MDI1-	615.73	4000	3384.27
A7	GBE0_MDI2+	630.44	4000	3369.56
A6	GBE0_MDI2-	628.29	4000	3371.71
A3	GBE0_MDI3+	598.26	4000	3401.74
A2	GBE0_MDI3-	596.34	4000	3403.66

Table 16 Carrier available traces - LAN

3.5 SATA

PCOM-B659 SATA

Pin#	Pin Name	COMe 3.0/3.1 Specification (Signals Requiring Module Termination)	Pin Typ	B659 Module	Pwr Rail /Tolerance(Volt)
A16	SATA0_TX+	AC coupled on the Module	O	0.01uF AC coupled on the Module(Gen3).	AC coupled on Module
A17	SATA0_TX-		SATA		
A19	SATA0_RX+		I		
A20	SATA0_RX-		SATA		
B16	SATA1_TX+		O		
B17	SATA1_TX-		SATA		
B19	SATA1_RX+		I		
B20	SATA1_RX-		SATA		
A28	(S)ATA_ACT#		O/D(I/O) CMOS	PU 4.7k ohm to V3P3S .	3.3V / 3.3V
B18	SUS_STAT#	Indicates imminent suspend operation; used to notify LPC devices	O CMOS	EC to Com Express Row connector.	3.3VSuspend/ 3.3V

Table 17 B659 SATA

3.5.1 PCB layout guideline -SATA

Parameter	Trace Routing
Transfer Rate	Up to 6.0 Gbit/s
Maximum signal line length (coupled traces)	6.0 inches
Differential Impedance	85 Ω +/-15%
Single-ended Impedance	50 Ω +/-15%
Trace width (W)	3.5 mil PCB stack-up dependent
Spacing between differential pairs (intra-pair) (S)	4mil PCB stack-up dependent
Spacing between differential pairs and high-speed periodic signals	Min. 20 mils

Spacing between differential pairs and low-speed non periodic signals	Min. 15 mils
Length matching between differential pairs (intra-pair)	Max. 5mils
Spacing from edge of plane	Min. 10*W mils (W=trace width)
Via Usage	A maximum of 1 vias is recommended.
AC Coupling capacitors	AC coupling capacitors for the TX and RX lines are incorporated on the COM Express Module
Reference plane	SATA pairs should be routed against a continuous GND plane.

Table 18 SATA layout information

3.5.2 Reference schematic - PCOM-C60B R0

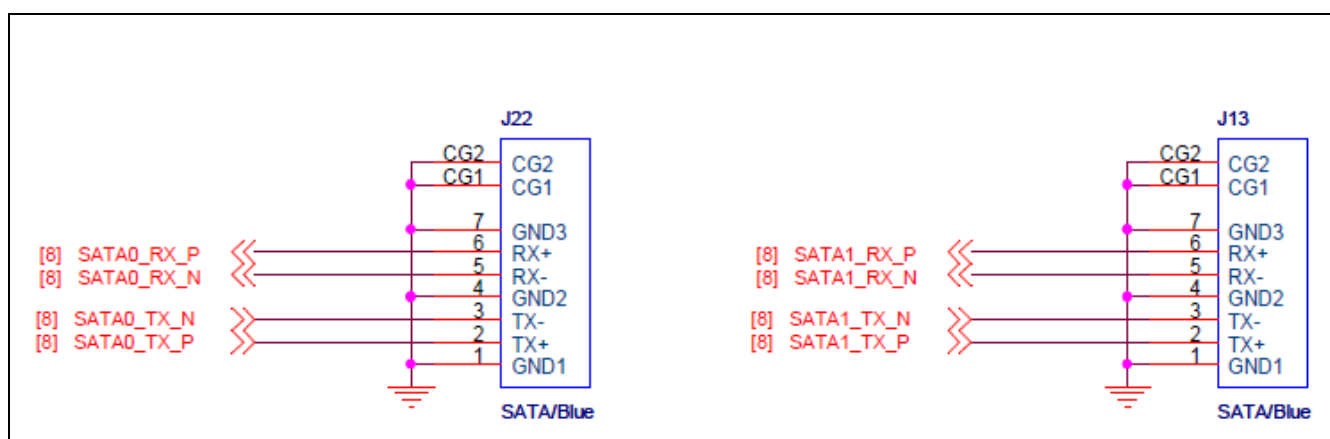


Figure 11 Reference schematic - SATA

3.5.3 Max trace length and available carrier trace length -

SATA

PIN	Name	Module Length	Max Length	Available Carrier length
A19	SATA0_RX+	2976.95	6000	3023.05
A20	SATA0_RX-	2980.9	6000	3019.1
A16	SATA0_TX+	2907.06	6000	3092.94
A17	SATA0_TX-	2910.45	6000	3089.55
B19	SATA1_RX+	2536.3	6000	3463.7

B20	SATA1_RX-	2534.61	6000	3465.39
B16	SATA1_TX+	2596.54	6000	3403.46
B17	SATA1_TX-	2597.16	6000	3402.84

Table 19 Carrier available traces - SATA

3.6 LVDS

PCOM-B659 LVDS

Pin#	Pin Name	COMe 3.0/3.1 Specification Specification (Signals Requiring Module Termination)	Pin Typ	B659 Module	Power Rail /Tolerance(Volt)
A71	LVDS_A0+		O LVDS	According to COM Express Spec 3.1 Table 4.39 LVDS/eDP Pin Assignment definition Co-lay,default module PTN3460 to LVDS Com Express Row connector.	LVDS
A72	LVDS_A0-				
A73	LVDS_A1+				
A74	LVDS_A1-				
A75	LVDS_A2+				
A76	LVDS_A2-				
A78	LVDS_A3+				
A79	LVDS_A3-				
A81	LVDS_A_CK+				
A82	LVDS_A_CK-				
B71	LVDS_B0+				
B72	LVDS_B0-				
B73	LVDS_B1+				
B74	LVDS_B1-				
B75	LVDS_B2+				
B76	LVDS_B2-				
B77	LVDS_B3+				
B78	LVDS_B3-				
B83	LVDS_BKLT_CTRL		O CMOS	LVDS_BKLT_CTRL	3.3V/ 3.3V
A77	LVDS_VDD_EN			LVDS panel power enable	
B79	LVDS_BKLT_EN			According to COM	
A83	LVDS_I2C_CK		I/O OD CMOS	Express Spec 2.1 Table	
A84	LVDS_I2C_DAT			4.37 LVDS/eDP Pin	

				Assignment definition Co-lay,default module PTN3460 to LVDS DDC signal to Com Express Row connector.	
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Table 20 B659 LVDS

3.6.1 PCB layout guideline - LVDS

Parameter	Trace Routing
Maximum signal line length to the LVDS connector (coupled traces)	10 inches
Differential Impedance	100 Ω +/-20%
Single-ended Impedance	50 Ω +/-15%
Trace width (W)	PCB stack-up dependent
Spacing between differential pair signals (intra-pair) (S)	30 PCB stack-up dependent
Spacing between pair to pairs (inter-pair) (s)	Min. 20mils
Spacing between differential pairs and high-speed periodic signals	Min. 20mils
Spacing between differential pairs and low-speed non periodic signals	Min. 20mils
Length matching between differential pairs (intra-pair)	+/- 20mils
Length matching between clock and data pairs (inter-pair)	+/- 20mils
Length matching between data pairs (inter-pair)	+/- 40mils
Spacing from edge of plane	+/- 40mils
Reference plane	GND referenced preferred
Via Usage	Max. of 2 vias per line

Table 21 LVDS Layout information

3.6.2 Reference schematic - PCOM-C60B R0

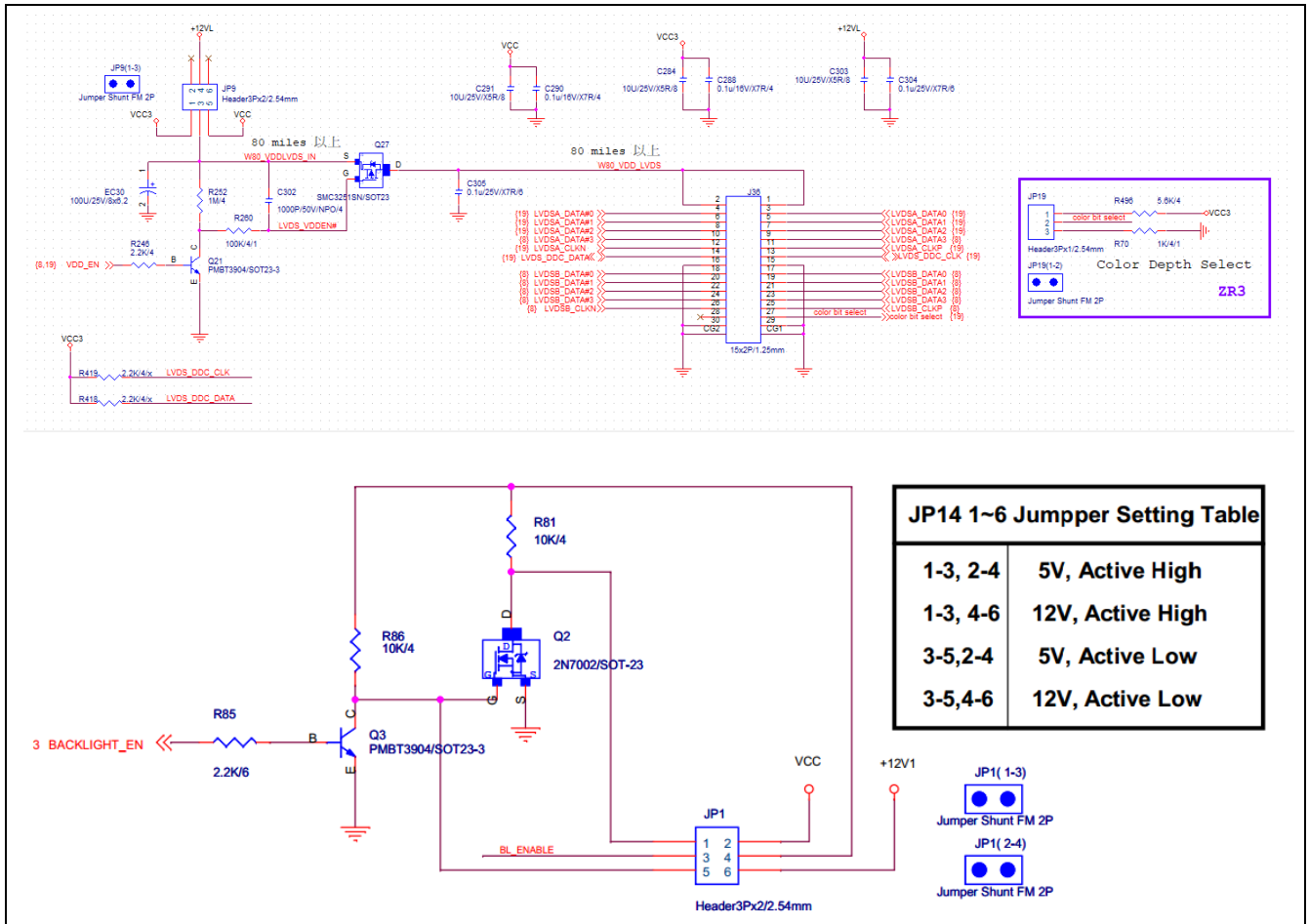


Figure 12 Reference schematic - LVDS

3.6.3 Max trace length and available carrier trace length - LVDS

PIN	Name	Module Length	Max Length	Available Carrier length
A71	LVDS_A0+	1389.76	10000	8610.24
A72	LVDS_A0-	1384.38	10000	8615.62
A73	LVDS_A1+	1130.87	10000	8869.13
A74	LVDS_A1-	1129.85	10000	8870.15
A75	LVDS_A2+	1030.66	10000	8969.34
A76	LVDS_A2-	1035.24	10000	8964.76
A78	LVDS_A3+	1016.56	10000	8983.44
A79	LVDS_A3-	1022.98	10000	8977.02
A81	LVDS_A_CK+	1073.88	10000	8926.12
A82	LVDS_A_CK-	1073.19	10000	8926.81
A83	LVDS_I2CCLK	1753.79	12000	10246.21

A84	LVDS_I2CDAT	1685.78	12000	10314.22
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Table 22 Carrier available traces – LVDS Channel A

PIN	Name	Module Length	Max Length	Available Carrier length
B71	LVDS_B0+	712.3	10000	9287.7
B72	LVDS_B0-	710.73	10000	9289.27
B73	LVDS_B1+	716.99	10000	9283.01
B74	LVDS_B1-	716.33	10000	9283.67
B75	LVDS_B2+	705.29	10000	9294.71
B76	LVDS_B2-	707.1	10000	9292.9
B77	LVDS_B3+	871.21	10000	9128.79
B78	LVDS_B3-	870.3	10000	9129.7
B81	LVDS_B_CK+	792.66	10000	9207.34
B82	LVDS_B_CK-	791.65	10000	9208.35

Table 23 Carrier available traces – LVDS Channel B

Table 4.39: LVDS / eDP Pin Assignment

Pin Name	Type 6/10 Pin Number	eDP
LVDS_A0+	A71	eDP_TX2+
LVDS_A0-	A72	eDP_TX2-
LVDS_A1+	A73	eDP_TX1+
LVDS_A1-	A74	eDP_TX1-
LVDS_A2+	A75	eDP_TX0+
LVDS_A2-	A76	eDP_TX0-
LVDS_A_CK+	A81	eDP_TX3+
LVDS_A_CK-	A82	eDP_TX3-
LVDS_VDD_EN	A77	eDP_VDD_EN
LVDS_BKLT_EN	B79	eDP_BKLT_EN
LVDS_I2C_CK	A83	eDP_AUX+
LVDS_I2C_DAT	A84	eDP_AUX-
LVDS_BKLT_CTRL	B83	eDP_BKLT_CTRL
RSVD	A87	eDP_HPD

3.7 UART

PCOM-B659 UART

Pin#	Pin Name	COMe 3.0/3.1 Specification (Signals Requiring Module Termination)	Pin Typ	B659 Module	Pwr Rail /Tolerance(Volt)
A98	SER0_TX		O CMOS		3.3V Suspend/ 3.3V
A99	SER0_RX	PU on Module	I CMOS	PU 47K to V3P3S on Module	
A101	SER1_TX		O CMOS		
A102	SER1_RX	PU on Module	I CMOS	PU 47K to V3P3S on Module	

Table 24 B659 UART

3.7.1 Reference schematic - PCOM-C605R

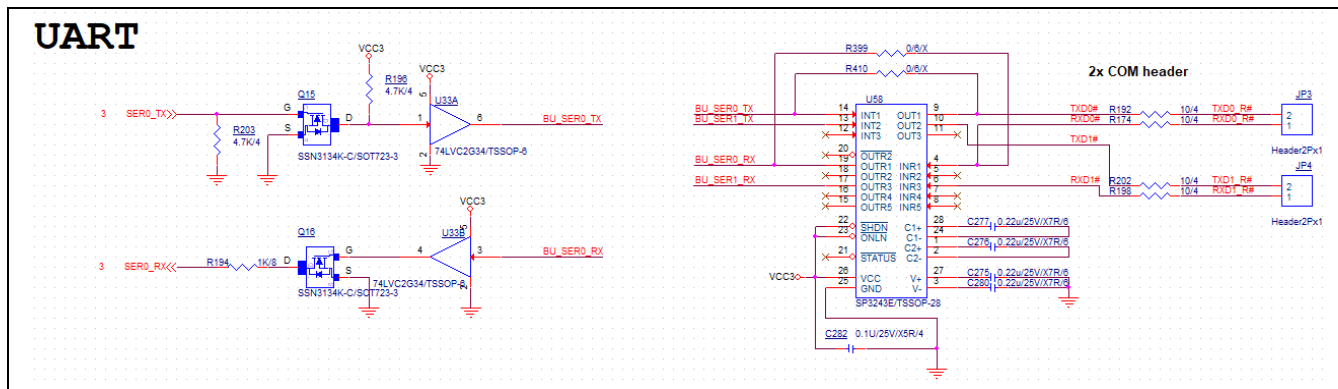


Figure 13 Reference schematic - UART

3.8 I2C

PCOM-B659 I2C

Pin#	Pin Name	COMe 3.0/3.1 Specification (Signals Requiring Module Termination)	Pin Typ	B659 Module	Pwr Rail /Tolerance(Volt)

B33	I2C_CLK	Pulled-up to 3.3V Standby on module with a 2.2k Ω resistor	I/O OD CMOS	PU 2.2k ohm to VCC3P3A_DSW .	3.3V Suspend/ 3.3V
B34	I2C_DAT				

Table 25 B659 I2C

3.9 SMBus

PCOM-B659 SMBus

Pin#	Pin Name	COMe 3.0/3.1 Specification (Signals Requiring Module Termination)	Pin Typ	B659 Module	Pwr Rail /Tolerance(Volt)
B13	SMB_CLK	Pulled-up to 3.3V standby on module with a 2.2k Ω resistor	I/O OD CMOS	PU 2.2k ohm to V3P3A	3.3VSuspend/ 3.3V
B14	SMB_DAT				
B15	SMB_ALERT#	-	I CMOS		

Table 26 B659 SMBus

3.9 GPIO

PCOM-B659 GPIO

Pin#	Pin Name	COMe 3.0/3.1 Specification (Signals Requiring Module Termination)	Pin Typ	B659 Module	Pwr Rail /Tolerance(Volt)
A54	GPI0	Pulled high internally on the Module.	I CMOS	PU 4.7k ohm to V3P3S.	3.3V/3.3V
A63	GPI1				
A67	GPI2				
A85	GPI3				
A93	GPO0	-	O CMOS	EC to Com Express Row connector.	3.3V/ 3.3V
B54	GPO1	-			
B57	GPO2	-			
B63	GPO3	-			

Table 27 B659 GPIO

3.10 LPC

PCOM-B659 LPC

Pin#	Pin Name	COMe 3.0/3.1 Specification (Signals Requiring Module Termination)	Pin Typ	B659VGL Module	Pwr Rail /Tolerance
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		Termination)			(Volt)
A50	LPC_SERIRQ	Pulled-up to 3.3V on module with a 8.2~10kΩ resistor	I/O CMOS	NONE	3.3V/3.3V
B3	LPC_FRAME#	-	O CMOS	F85227 (eSPI to LPC IC) to Com Express Row connector.	
B4	LPC_AD0	-	I/O CMOS		
B5	LPC_AD1	-			
B6	LPC_AD2	-			
B7	LPC_AD3	-			
B8	LPC_DRQ0#	-	I CMOS	NC	
B9	LPC_DRQ1#	-		ESPI_ALERT1#	
B10	LPC_CLK	-	O CMOS	Series connection 22 ohm (Intel CRB)	

Table 28 B659 LPC

3.10.1 PCB layout guideline - LPC

Parameter	Trace Routing
Transfer Rate	25/33MHz
Maximum signal line length for the COM Express Carrier Board	15.0 inches
Single-ended Impedance	55 Ω +/-15%
Trace width (W)	PCB stack-up dependent
Spacing between signals (inter-signal) (S)	PCB stack-up dependent
Length matching between single ended signals	Max. 200mils
Length matching between clock signals	Max. 200mils
Spacing from edge of plane	Min. 40mils
Reference plane	GND referenced preferred
Via Usage	Try to minimize number of vias

Table 29 LPC Layout information

3.10.2 Reference schematic - PCOM-C605 R0

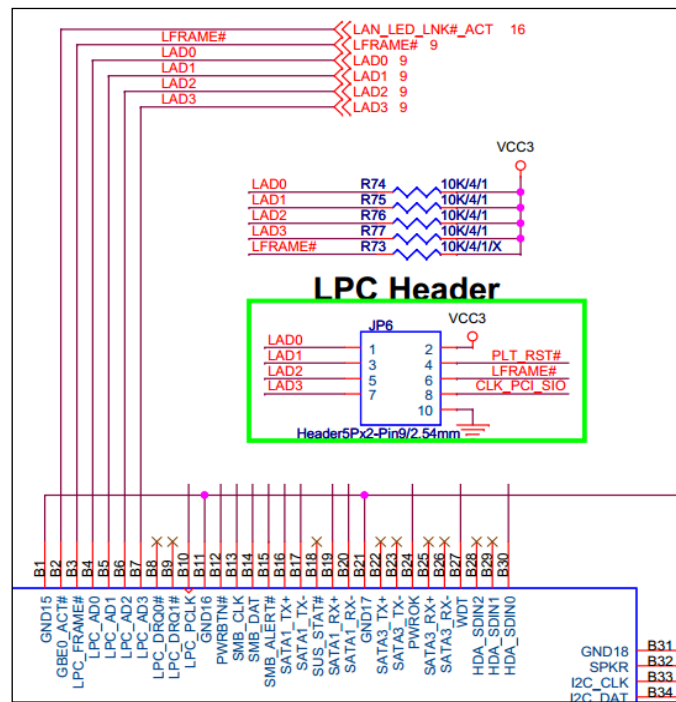


Figure 14 Reference schematic - LPC

3.11 SPI

An external SPI BIOS is designed on the Carrier board, which allows the Module boot from the Carrier SPI BIOS. To achieve this function, the BIOS_DIS0# and BIOS_DIS1# must be designed as a selectable method on the Carrier.

PCOM-B659 SPI

Pin#	Pin Name	COMe 3.0/3.1 Specification (Signals Requiring Module Termination)	Pin Typ	B659VGL Module	Pwr Rail /Tolerance (Volt)
A34	BIOS_DIS0#	Pulled up to 3.3V on module with a 10K Ω resistor	I	PU 10k ohm to VCC3P3A_DSW	NA
B88	BIOS_DIS1#		CMOS		
A91	SPI_POWER	Power supply for Carrier Board SPI – sourced from Module – nominally 3.3V. The Module shall provide a minimum of 100mA on SPI_POWER	Power Out	SPI_POWER	3.3V Suspend/ 3.3V
A92	SPI_MISO	All such terminations shall be on the Module	I CMOS	33 ohm series connection	
A94	SPI_CLK	When supporting Carrier Board based SPI devices, the SPI_MISO, SPI_MOSI and SPI_CLK line shall have a series resistor of 15Ω	O CMOS		
A95	SPI_MOSI				
B97	SPI_CS#	-	O CMOS	-	

Table 30 PCOM-B659 SPI

(Single Ended) trace impedance for all lines (data, clock, and chip selects) should be 50 ohms. The junction branch point (a via for each signal in the set SPI_MISO, SPI_MOSI and SPI_CLK) marked with a red 'BP' in the figure should be placed as close as possible (within 100 mil) to the relevant Module Connector ball. The series resistors shown in the Figure should be 15 ohms.

Figure 5.13: COM Express BOOT SPI Topology – Data and Clock lines

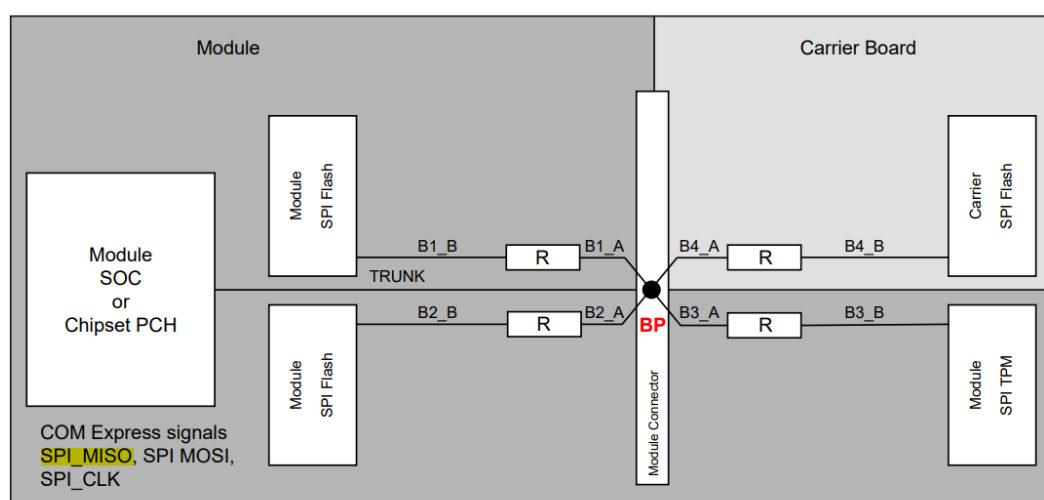


Table 5.35: Boot SPI Branch Segment Length Restrictions

Branch	Allowable Branch Segment Length Min / Max (mils)	Length Matching Within a Branch	Notes
TRUNK	1000 / 5000	Length match data and clock in this trunk branch to within + / - 125 mils	Includes SOC breakout
B1_A + B1_B	2000 / 3000	Length match data and clock in this branch to within + / - 125 mils	Module Branch
B2_A + B2_B	2000 / 3000	Length match data and clock in this branch to within + / - 125 mils	Module Branch
B3_A + B3_B	2000 / 3000	Length match data and clock in this branch to within + / - 125 mils	Module Branch
B4_A + B4_B	2000 / 3000	Length match data and clock in this branch to within + / - 125 mils	Carrier Branch
B1_A	0 / 500		
B2_A	0 / 500		
B3_A	0 / 500		
B4_A	0 / 500		

3.11.1 Reference schematic - PCOM-C60B R0

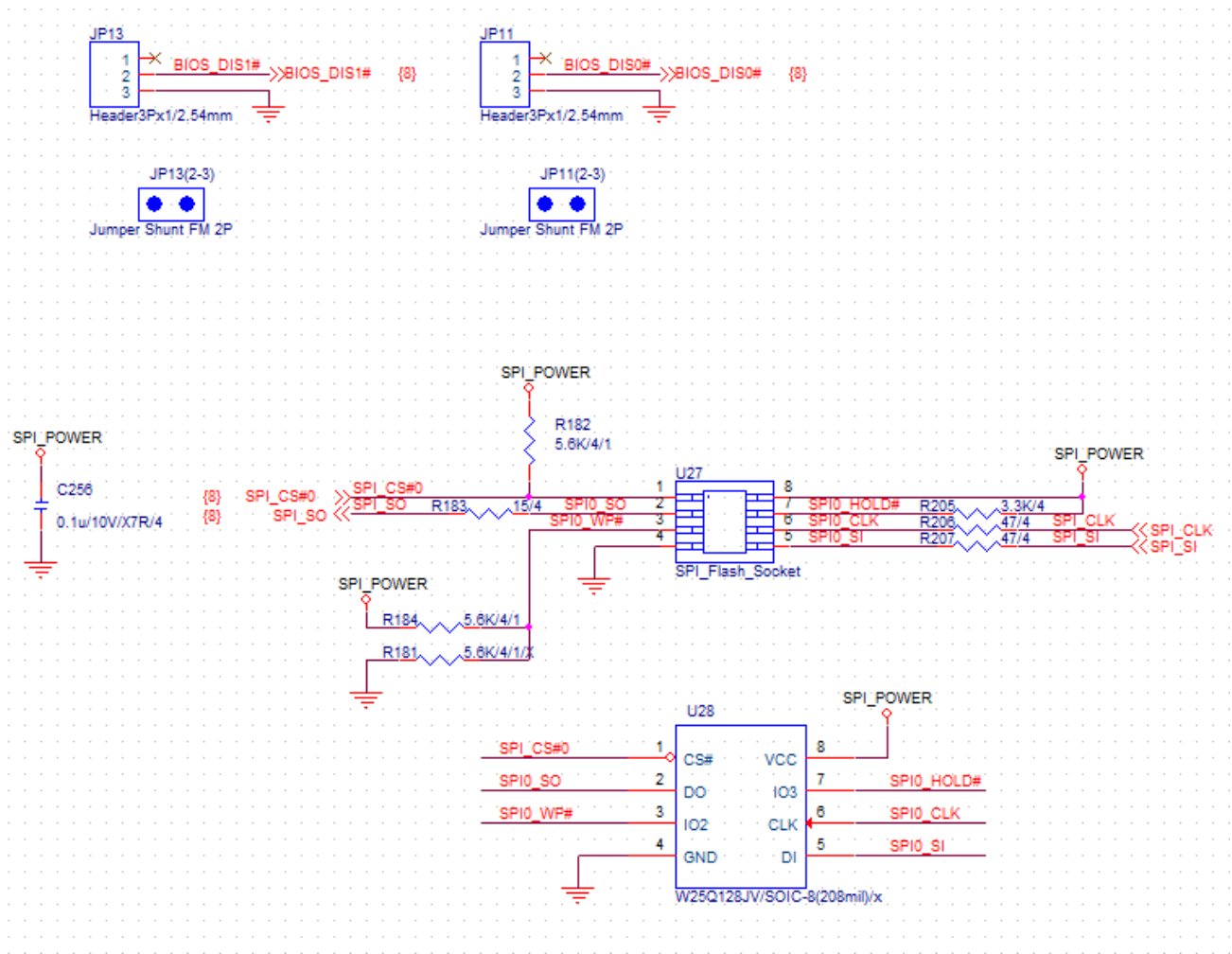


Figure 15 Reference schematic – SPI

3.12 VGA

PCOM-B659 VGA

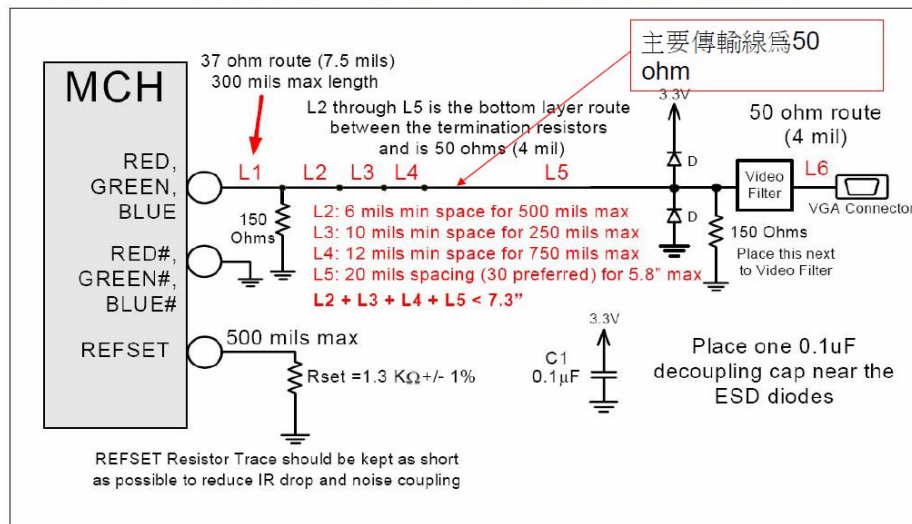
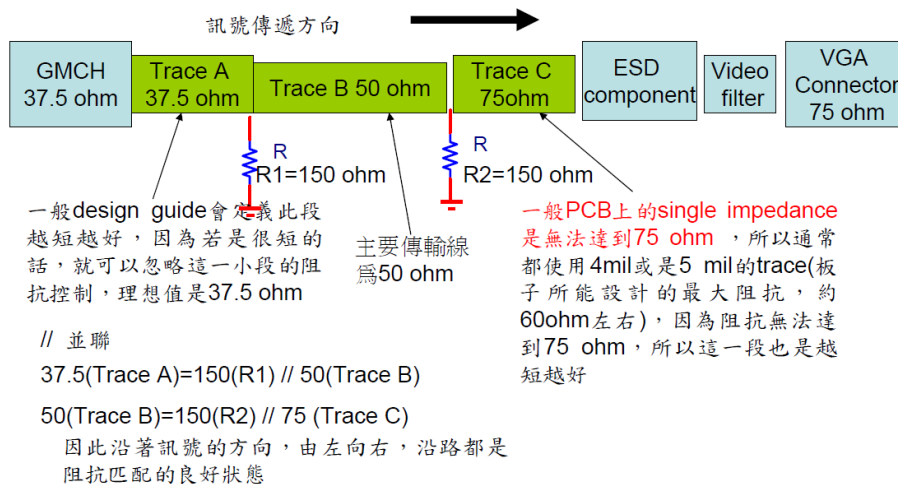
Pin#	Pin Name	COMe 3.0/3.1 Specification (Signals Requiring Module Termination)	Pin Typ	B659VGL Module	Pwr Rail /Tolerance(Volt)
B89	VGA_RED	The analog VGA data lines are typically terminated with 150 ohms to GND on the Module, and with a parallel 150 ohms to GND at the Carrier VGA connector, for a combined 75 ohm Module / Carrier termination. The VGA monitor is also terminated with 75 ohms to GND. A 37.5 ohm characteristic impedance cable is typically used.	O Analog	PD 150 ohm	Analog
B91	VGA_GRN				
B92	VGA_BLU				
B93	VGA_HSYNC	-	O	-	3.3V / 3.3V
B94	VGA_VSYNC	-	CMOS	-	
B95	VGA_I2C_CK	PU 2.2k ohm	I/O OD	PU 2.2k ohm to V3P3S.	
B96	VGA_I2C_DAT	PU 2.2k ohm	CMOS	PU 2.2k ohm to V3P3S.	

Table 31 PCOM-B659 VGA

3.12.1 PCB layout guideline - VGA

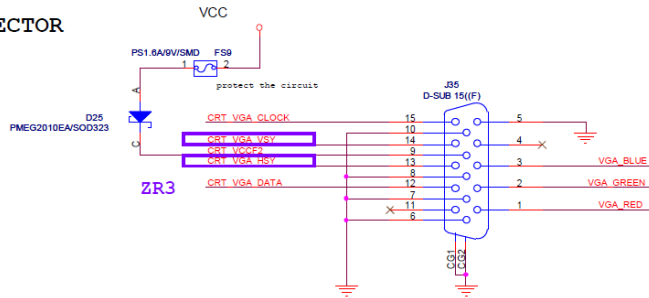
Parameter	Trace Routing
Maximum signal line length to the LVDS connector (coupled traces)	7.5 inches
PD Resistance	150 ohm
Single-ended Impedance	50 Ω +/-15%
Trace width (W)	4~5 mil PCB stack-up dependent
Spacing between pairs-to-pairs (inter-pair) (s) _RGB	20 mil (30 preferred)

Table 32 VGA Layout information

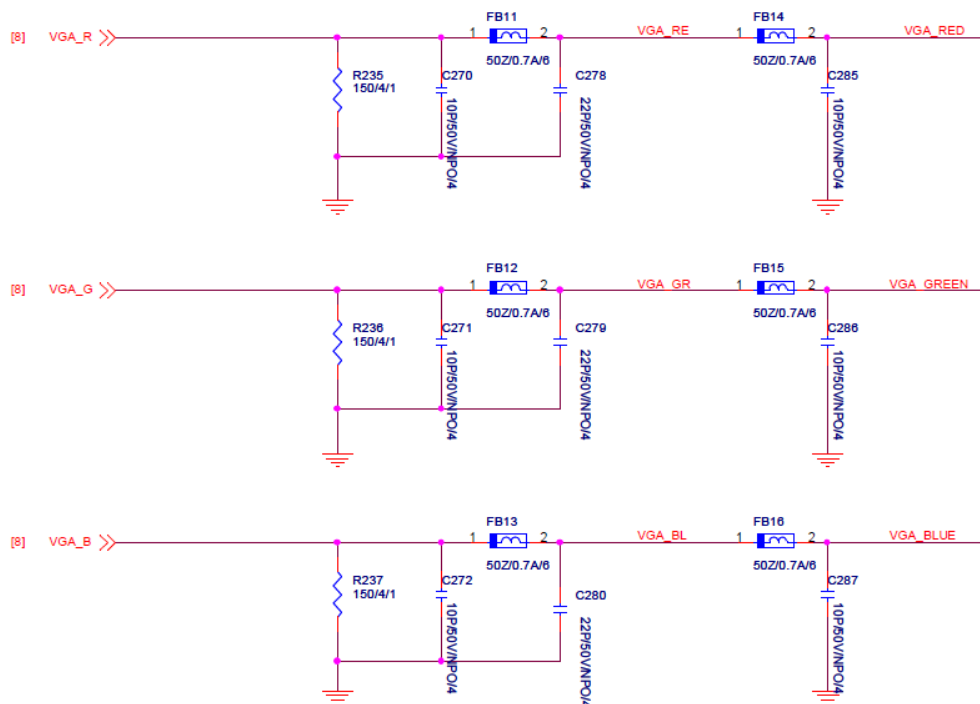
Figure 6-1. R, G, B Board Routing Recommendation for BTX/ μ BTX platforms

3.12.2 Reference schematic - PCOM-C60B ZR3

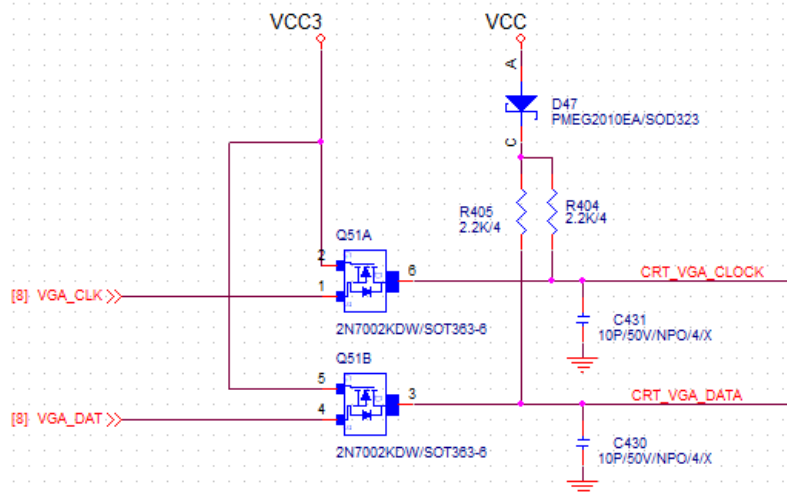
VGA_CONNECTOR



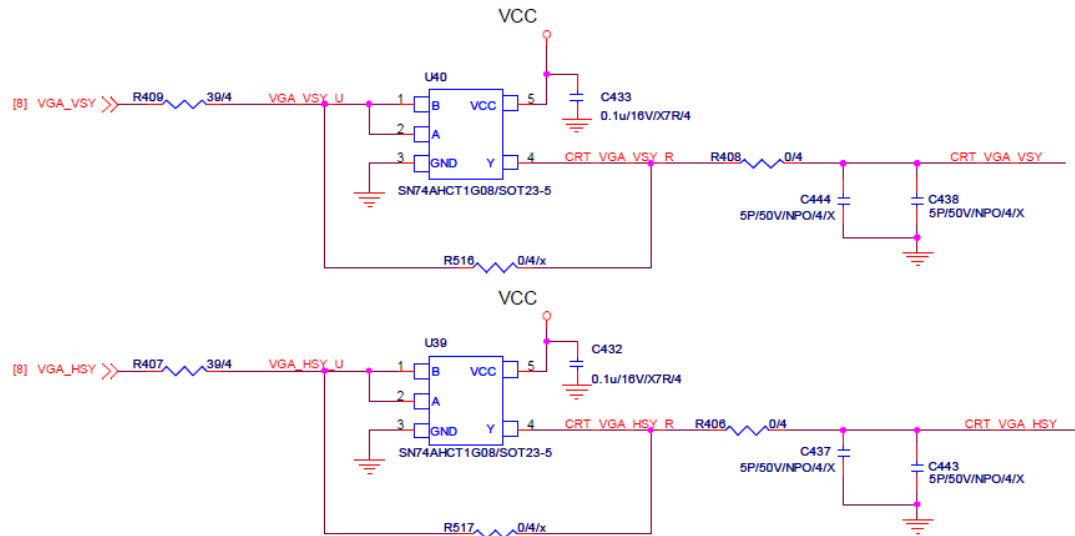
VGA_RGB



VGA_CLK&DAT



VGA_H&V



VGA_PROTECTION

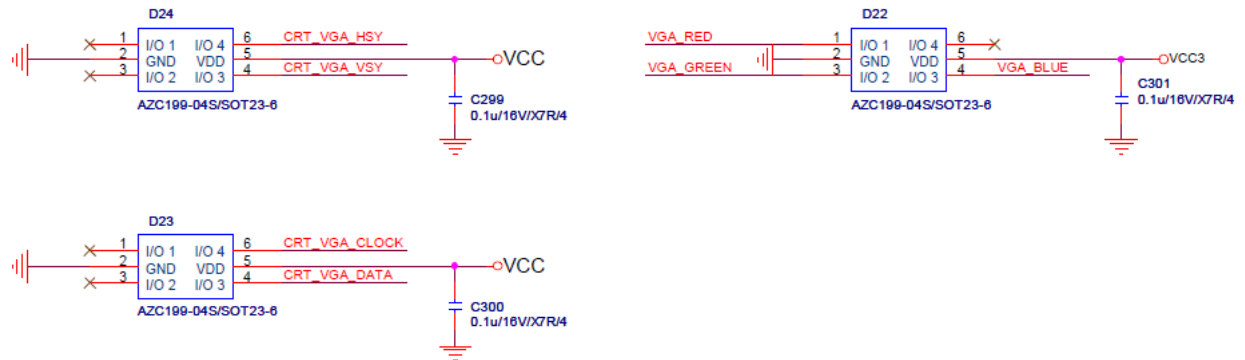


Figure 16 Reference schematic - VGA

3.12.3 Max trace length and available carrier trace length - VGA

PIN	Name	Module Length	Max Length	Available Carrier length
B89	VGA_RED	404.08	7500	7095.92
B91	VGA_GRN	343.89	7500	7156.11
B92	VGA_BLU	381.41	7500	7118.59
B93	VGA_HSYNC	354.98	7500	7145.02
B94	VGA_VSYNC	364.92	7500	7135.08
B95	VGA_I2C_CK	560.99	7500	6939.01
B96	VGA_I2C_DAT	531.09	7500	6968.91

Table 33 Carrier available traces – VGA

3.13 RTC

To implement the RTC Battery according to the Underwriters Laboratories Inc® (UL) guidelines, battery cells must be protected against a reverse current going to the cell. This can be done by either a series low-leakage diode and/or a series resistor. Revision 1.0 of this specification did not specify the location of this diode and the location was vendor implementation specific. For revision 2.0 Carrier Boards, a protection diode or a series resistor shall be placed on the Carrier Board. For backwards compatibility, a revision 2.0 Module may also implement the protection diode.

Note: If a Schottky diode is used, the leakage current must not exceed the UL requirement of the battery, especially at the temperature limits.

Power Rail	Module Pin Current Capability (Amps)	Nominal Input (Volts)	Input Range (Volts)	Max Input Ripple (mV)
VCC_RTC	0.5	3	2.0 - 3.3	+/-20

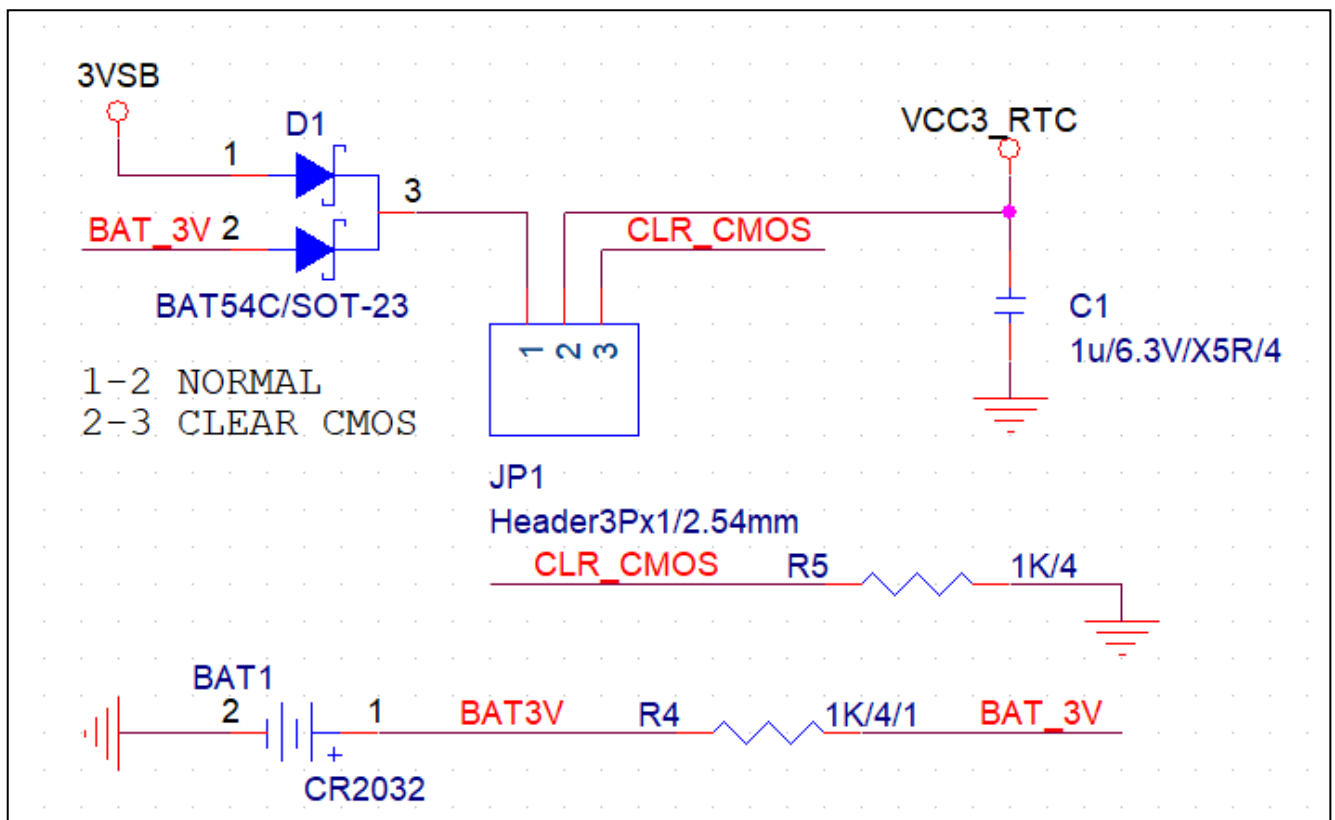


Figure 17 Reference schematic - RTC

4 Power

PCOM-B659 is designed for both AT and ATX power mode, which depends on the power mode design on carrier board. The following ATX and AT mode power sequences are provided for the carrier design guideline.

4.1 Power sequence

The ATX power sequence is based on PCOM-B659-ZR0 with evaluation carrier PCOM-C60B-R0 or PCOM-C605-R0.

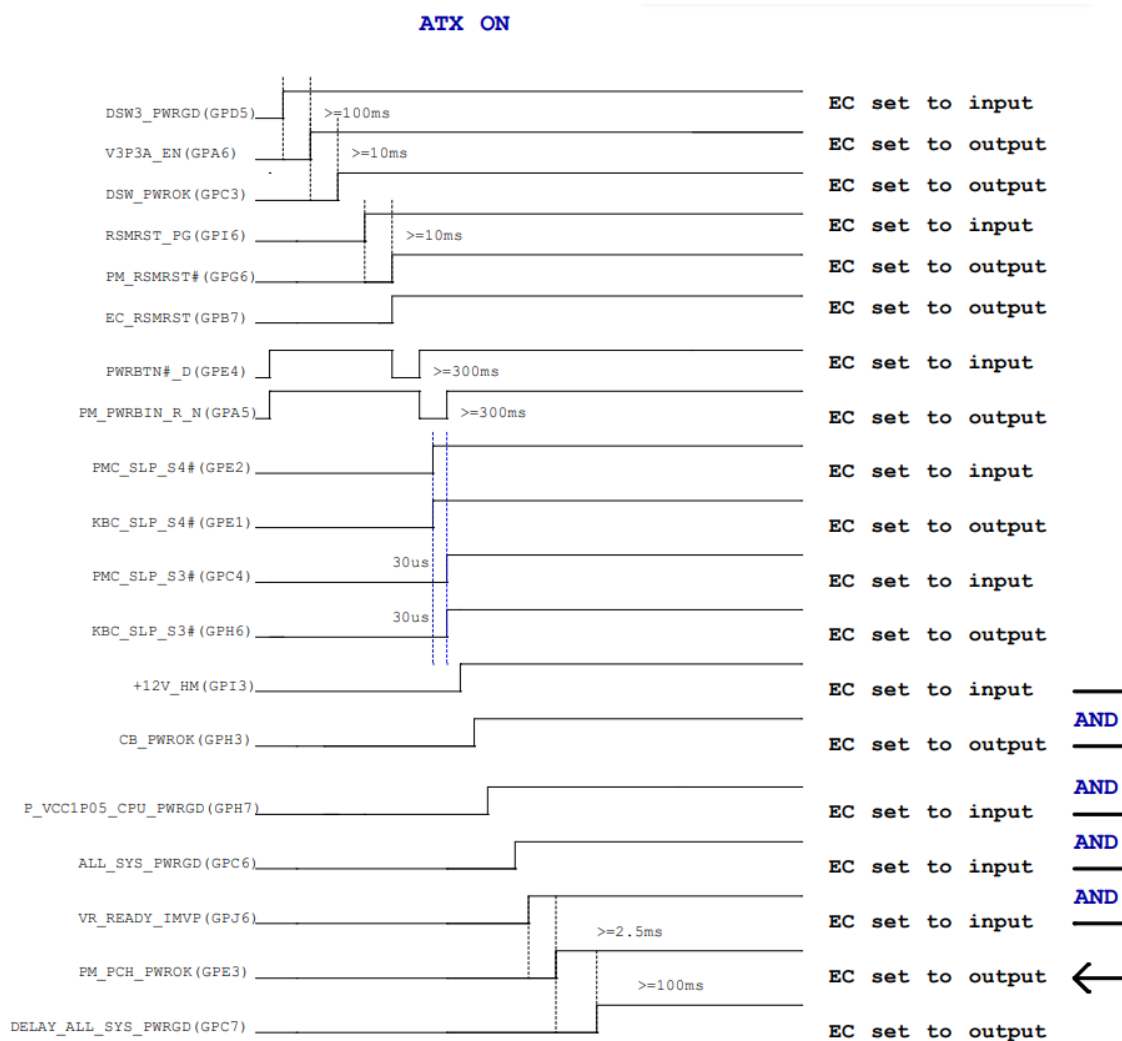


Figure 18 B659 ATX Mode power sequence

The AT power sequence is based on PCOM- B659 with evaluation carrier PCOM-C60B-R0 or PCOM-C605-R0.

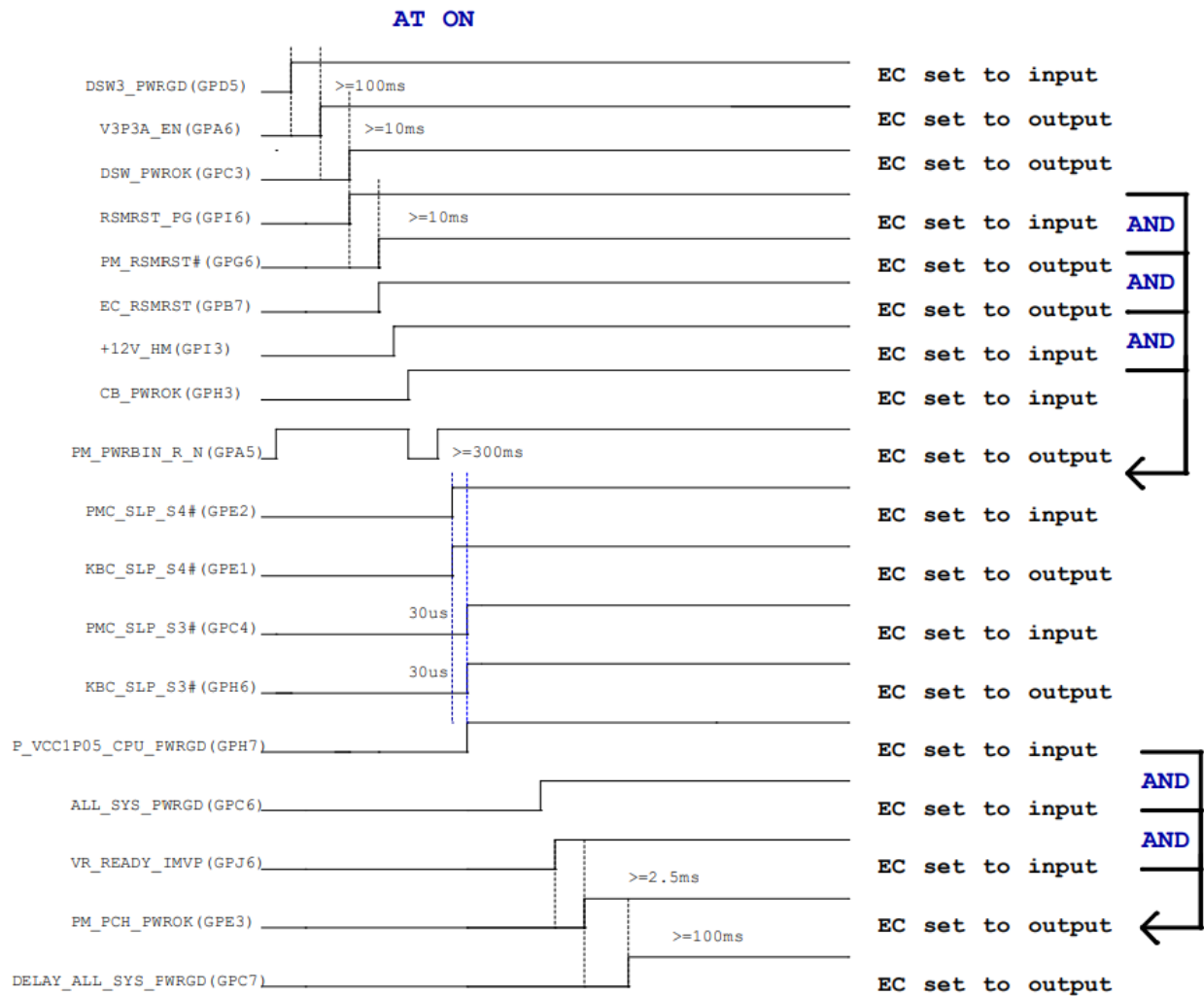


Figure 19 B659 AT Mode power sequence

5 Mechanical

5.1 PCOM-B659 Dimension

PCOM-B659 top & bottom side view dimension

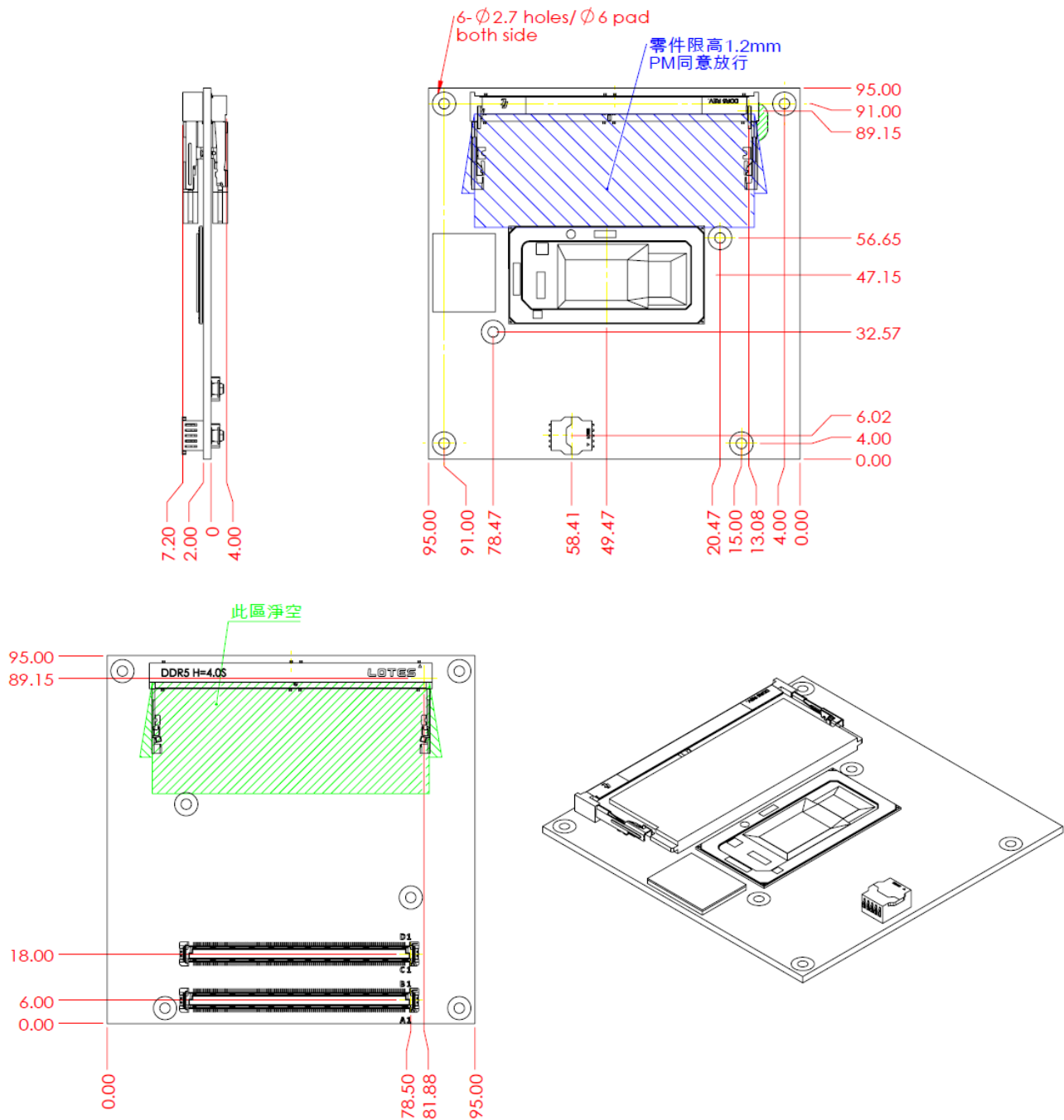


Figure 20 PCOM-B659 Dimension – TOP & Bottom

PCOM-B659 cooler / heatsink / heatspreader dimension

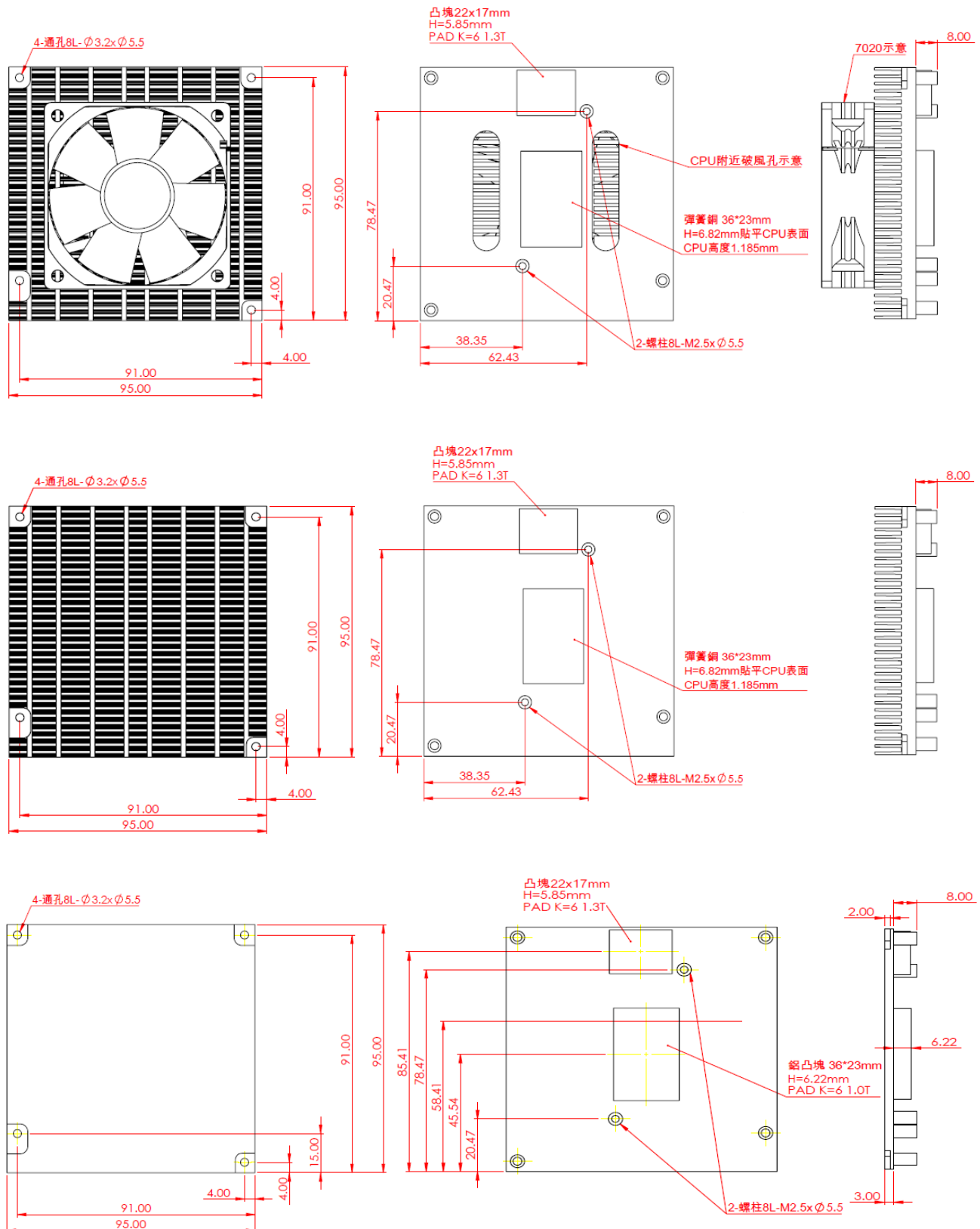


Figure 21 PCOM-B659 cooler / heatsink / heatspreader dimension

6 COM Express Module and Carrier protection design

6.1 Module protection

PCOM-B659 Type 6 is also compatible with COM Express Type 2 carrier, Schottky diode protection has been design on the COM Express module for Serial Port, FAN(PWMOUT & TACHIN), LID and SLEEP. Please refer to Fig.21 Module circuit protection schematic.

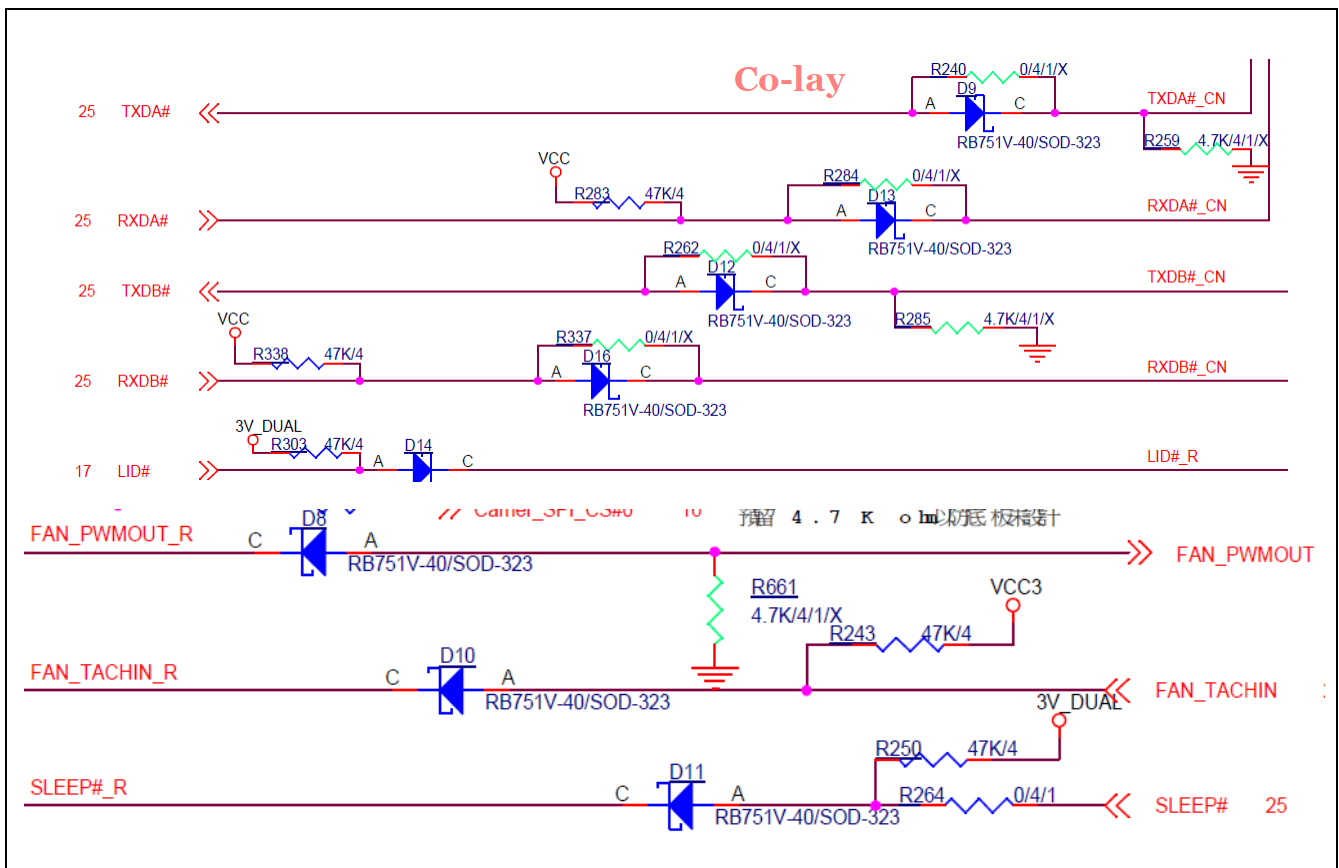


Figure 22 Circuit protection on Module

6.2 Carrier protection

Avoiding Carrier accidentally exposure to VCC_12V pool, a circuit protection design should be implemented on the Carrier, please refer to Fig.22 Carrier circuit protection schematic.

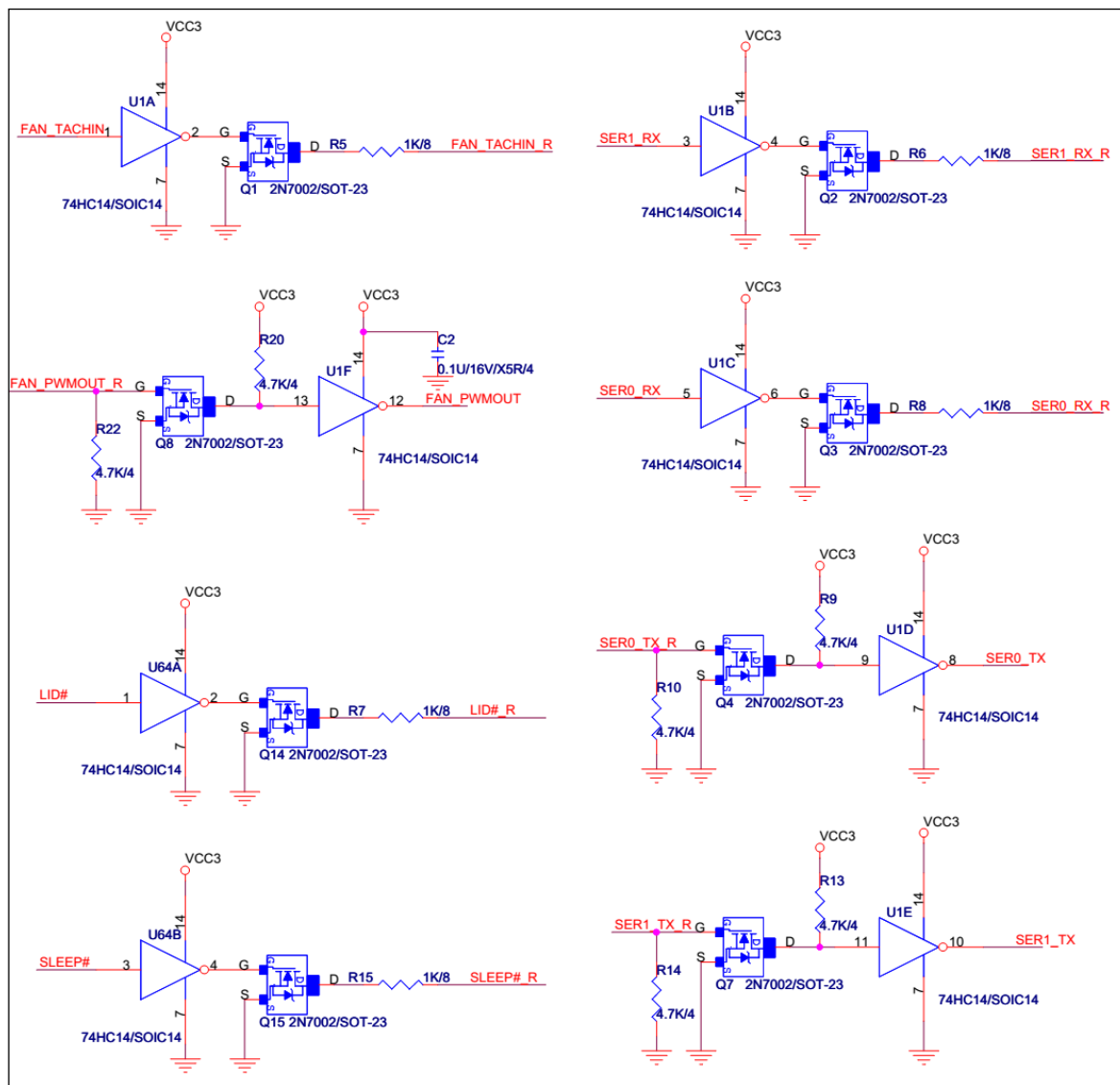


Figure 23 Circuit protection on Carrier

7 Industry Specifications

Low Pin Count Interface Specification, Revision 1.0 (LPC)

<http://www.intel.com/design/chipsets/industry/lpc.htm>

Universal Serial Bus (USB) Specification, Revision 2.0 <http://www.usb.org/home>

PCI Specification, Revision 2.3 <https://www.pcisig.com/specifications>

Serial ATA Specification, Revision 3.0 <http://www.serialata.org/>

PCI Express Base Specification, Revision 2.0 <https://www.pcisig.com/specifications>

PICMG® COM Express Module™ Base Specification <http://www.picmg.org/>

PICMG®COM Express Carrier Board Design Guide <http://www.picmg.org/>