

COM Express Carrier Design Guide

Carrier design guideline for PCOM-B702GT

Rev. R1.3

Revision history

Rev.	Date	Note
R0.1	June.2019	Preliminary
R1.0	April.2020	First Release
R1.1	Jan. 2022	Update all. (David Lee)
R1.2	Dec. 2023	Sku updated
R1.3	Feb. 2026	VBAT updated

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1 Introduction

The Carrier Design Guide provides the guideline of designing your own carrier board based on Portwell's COM Express Modular product PCOM-B702GT. PCOM-B702GT is a Type 7, 95x95mm Module board, more information is included in PCOM-B702GT User's Guide and can be downloaded from Portwell download center (Or contact your Portwell sales representative for acquiring PCOM-B702GT User's Guide). This carrier design guide is dedicated for the designers designing a COM Express Type 7 carrier board which will have an excellent compatibility with Portwell's PCOM-B702GT modular product.

The layout guideline provided are 8 PCB layer stack up, each interface has three sections, which are detail PCOM-B702GT pin out, pin name, power rail, PU/PD, AC couple capacitor and etc. information are included. Second part containing PCB layout guide, impedance, maximum trace, trace width, and trace spacing etc. Third section provides the available trace length of which designers are able to optimize the high speed signals such as PCIE, SATA, USB etc.

1.1 Comparison of Type 6 and Type 7 (COM Express draft ver.)

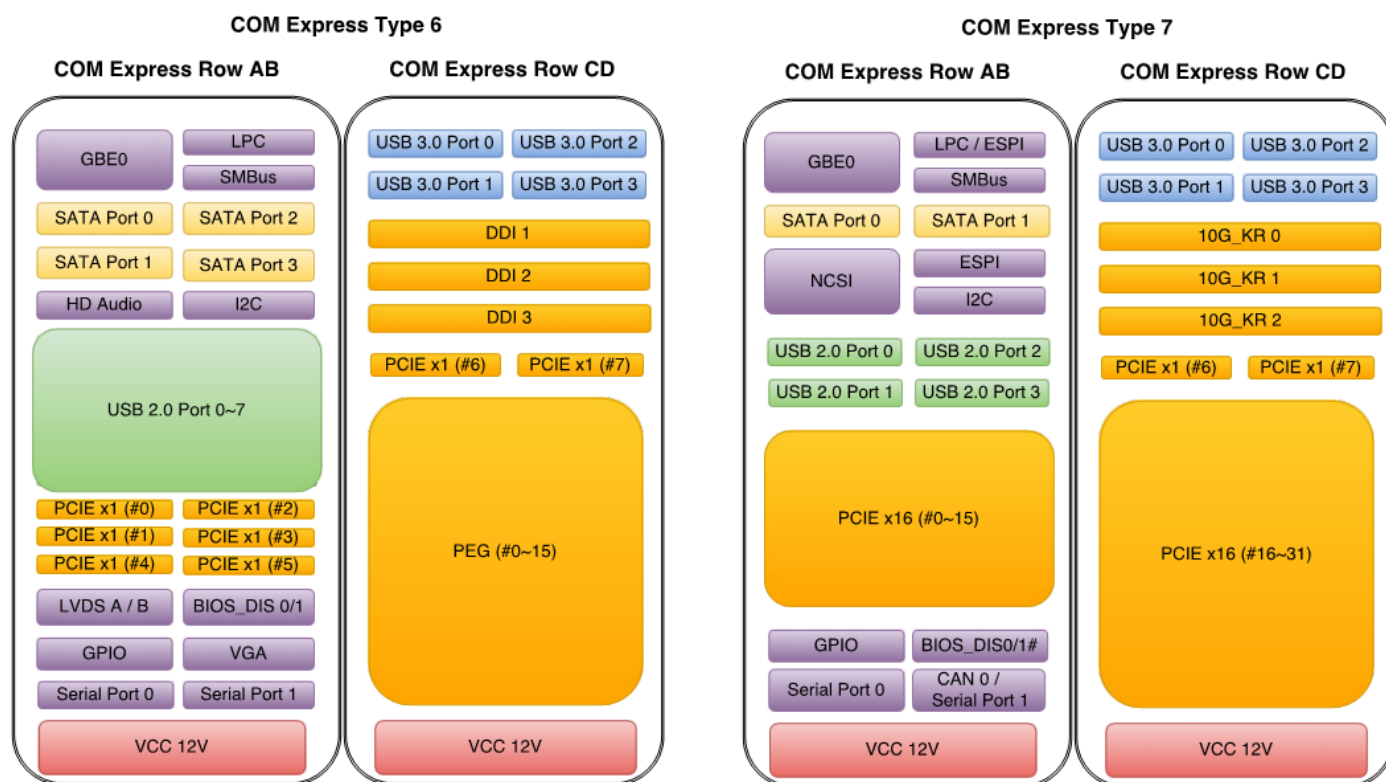
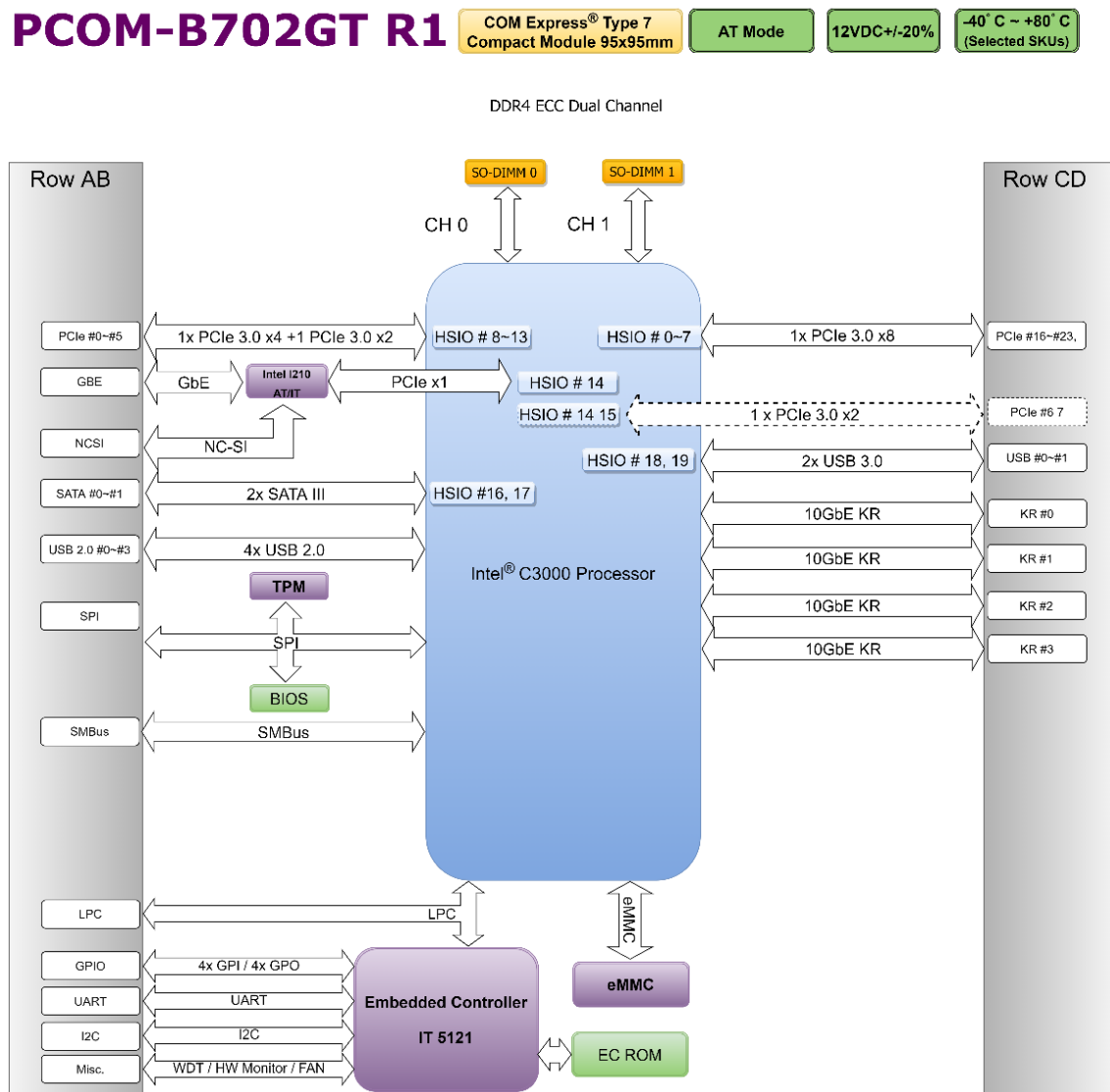


Figure 1 COM Express Type 6 and Type 7 Comparison

2.1 PCOM-B702GT Block Diagram



3 COM Express Interface

3.1 PCIe

PIN OUT

Pin	Signal	Description	I/O	Type	Power / Tolerance	PU / PD	Note
A52	PCIE_TX_DP13	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A53	PCIE_TX_DN13	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A55	PCIE_TX_DP12	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A56	PCIE_TX_DN12	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A58	PCIE_TX_DP11	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A59	PCIE_TX_DN11	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A61	PCIE_TX_DP10	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A62	PCIE_TX_DN10	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A64	PCIE_TX_DP9	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A65	PCIE_TX_DN9	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A68	PCIE_TX_DP8	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A69	PCIE_TX_DN8	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A88	CLK3_PCIE_P_CN	Reference clock output for all PCI Express and PCI Express Graphics lanes.	O	PCIE	PCIE	-	-
A89	CLK3_PCIE_N_CN	Reference clock output for all PCI Express and PCI Express Graphics lanes.	O	PCIE	PCIE	-	-

B52	PCIE_RX_DP13	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B53	PCIE_RX_DN13	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B55	PCIE_RX_DP12	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B56	PCIE_RX_DN12	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B58	PCIE_RX_DP11	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B59	PCIE_RX_DN11	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B61	PCIE_RX_DP10	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B62	PCIE_RX_DN10	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B64	PCIE_RX_DP9	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B65	PCIE_RX_DN9	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B68	PCIE_RX_DP8	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B69	PCIE_RX_DN8	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C52	PCIE_RX_DP0	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C53	PCIE_RX_DN0	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C55	PCIE_RX_DP1	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C56	PCIE_RX_DN1	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C58	PCIE_RX_DP2	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C59	PCIE_RX_DN2	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C61	PCIE_RX_DP3	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-

C62	PCIE_RX_DN3	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C65	PCIE_RX_DP4	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C66	PCIE_RX_DN4	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C68	PCIE_RX_DP5	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C69	PCIE_RX_DN5	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C71	PCIE_RX_DP6	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C72	PCIE_RX_DN6	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C74	PCIE_RX_DP7	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C75	PCIE_RX_DN7	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
D52	PCIE_TX_DP0	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D53	PCIE_TX_DN0	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D55	PCIE_TX_DP1	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D56	PCIE_TX_DN1	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D58	PCIE_TX_DP2	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D59	PCIE_TX_DN2	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D61	PCIE_TX_DP3	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D62	PCIE_TX_DN3	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D65	PCIE_TX_DP4	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D66	PCIE_TX_DN4	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D68	PCIE_TX_DP5	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-

D69	PCIE_TX_DN5	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D71	PCIE_TX_DP6	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D72	PCIE_TX_DN6	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D74	PCIE_TX_DP7	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D75	PCIE_TX_DN7	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-

Table 1 PCIE Pin Out

3.1.1 AC Coupling Capacitor

PCIE / PEG AC Coupling: Device Down

While PCIE devices are designed on COM Express Carrier Board, the AC coupling Capacitor should be added on the carrier, please refer to below diagram.

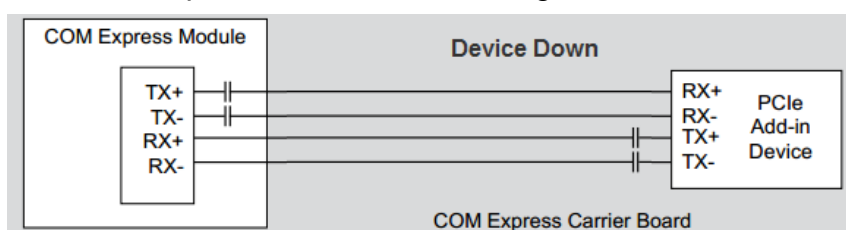


Figure 3 PCIE AC Coupling Capacitor - Device Down
(From PICMG COM Express Carrier Board Design Guide)

PCIE / PEG AC Coupling: Add-In Card

While PCIE devices are designed as Add in Card, the AC coupling Capacitor should be on PCIE Add-In Card, rather than on the COM Express Carrier Board, please refer to below diagram.

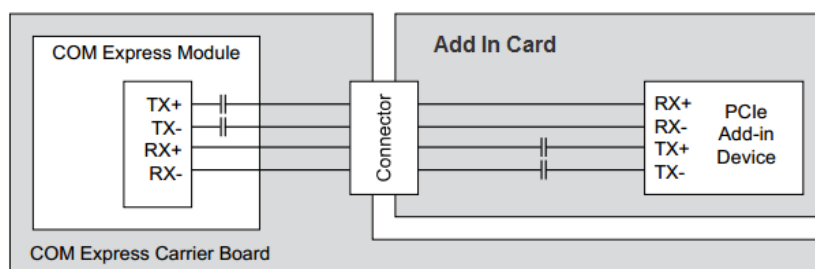


Figure 4 PCIe AC Coupling Capacitor - Add In Card
(From PICMG COM Express Carrier Board Design Guide)

3.1.2 PCB Layout Guideline - PCIe

Parameter	PCIe Gen1	PCIe Gen2	PCIe Gen3
Symbol Rate / PCIe Lane	2.5 G Symbols/s	5.0 G Symbols/s	8.0 G Symbols/s
Maximum signal line length (coupled traces) TX and RX	21.0 inches	21.0 inches	14.0 inches
Signal length allowance on the COM Express Carrier Board to PCIe device	15.85 inches	15.85 inches	10.0 inches
Signal length allowance on the COM Express Carrier Board to PCIe slot	9.00 inches	9.00 inches	4.0 inches
PCI-SIG: Differential impedance recommendation	100 Ω +/-20%	85 Ω +/-15%	85 Ω +/-15%
COMCDG Rev. 1.0: Differential impedance recommendation for a GEN1 and GEN2 design	92 Ω +/-10%		-
COMCDG Rev. 2.0: Differential impedance recommendation for new Carrier designs	85 Ω +/-15%		
Single-ended Impedance	55 Ω +/-15%	50 Ω +/-15%	50 Ω +/-15%
Trace width (W)	PCB stack-up dependent	PCB stack-up dependent	PCB stack-up dependent
Spacing between differential pairs (intra-pair) (S)	PCB stack-up dependent	PCB stack-up dependent	PCB stack-up dependent
Spacing between RX and TX pairs (inter-pair) (s)	Min. 20mils	Min. 20mils	Min. 20mils
Spacing between differential pairs and high-speed periodic signals	Min. 50mils	Min. 50mils	Min. 50mils
Spacing between differential pairs and low-speed non periodic signals	Min. 20mils	Min. 20mils	Min. 20mils
Length matching between differential pairs (intra-pair)	Max. 5mils	Max. 5mils	Max. 5mils
Length matching between RX and TX pairs (inter-pair)	No strict electrical requirements. Keep difference within a 3.0 inch delta to minimize latency.	No strict electrical requirements. Keep difference within a 3.0 inch delta to minimize latency.	No strict electrical requirements. Keep difference within a 3.0 inch delta to minimize latency.
Length matching between reference clock differential pairs REFCLK+ and REFCLK- (intra-pair)	Max. 5mils	Max. 5mils	Max. 5mils
Length matching between reference clock pairs (inter-pair)	No electrical requirements.	No electrical requirements.	No electrical requirements.
Reference plane	GND referenced preferred	GND referenced preferred	GND referenced preferred
Spacing from edge of plane	Min. 40mils	Min. 40mils	Min. 40mils
Via Usage	Max. 2 vias per TX trace Max. 4 vias per RX trace	Max. 2 vias per TX trace Max. 4 vias per RX trace	Max. 2 vias / TX Max. 4 vias / RX (to device) Max. 2 vias / RX (to slot)
AC coupling capacitors	The AC coupling capacitors for the TX lines are incorporated on the COM Express Module. The AC coupling capacitors for RX signal lines have to be implemented on the customer COM Express Carrier Board. Capacitor type: X7R, 100nF +/-10%, 16V, shape 0402.	The AC coupling capacitors for the TX lines are incorporated on the COM Express Module. The AC coupling capacitors for RX signal lines have to be implemented on the customer COM Express Carrier Board. Capacitor type: X7R, 100nF +/-10%, 16V, shape 0402.	The AC coupling capacitors for the TX lines are incorporated on the COM Express Module. The AC coupling capacitors for RX signal lines have to be implemented on the customer COM Express Carrier Board. Capacitor type: X7R, 200nF +/-10%, 16V, shape 0402.

Table 2 Layout Guideline – PCIe/PEG

3.1.3 Passive Devices

AC Cap value (Gen1/Gen2)	Min = [75nF] Max = [265nF]	PCOM-B702GT AC Cap value [220nF]
AC Cap value (Gen3)	Min = [75nF] Max = [265nF]	

Table 3 PCIe/PEG AC Coupling Capacitor Value

3.1.4 Reference Schematic - PCIe

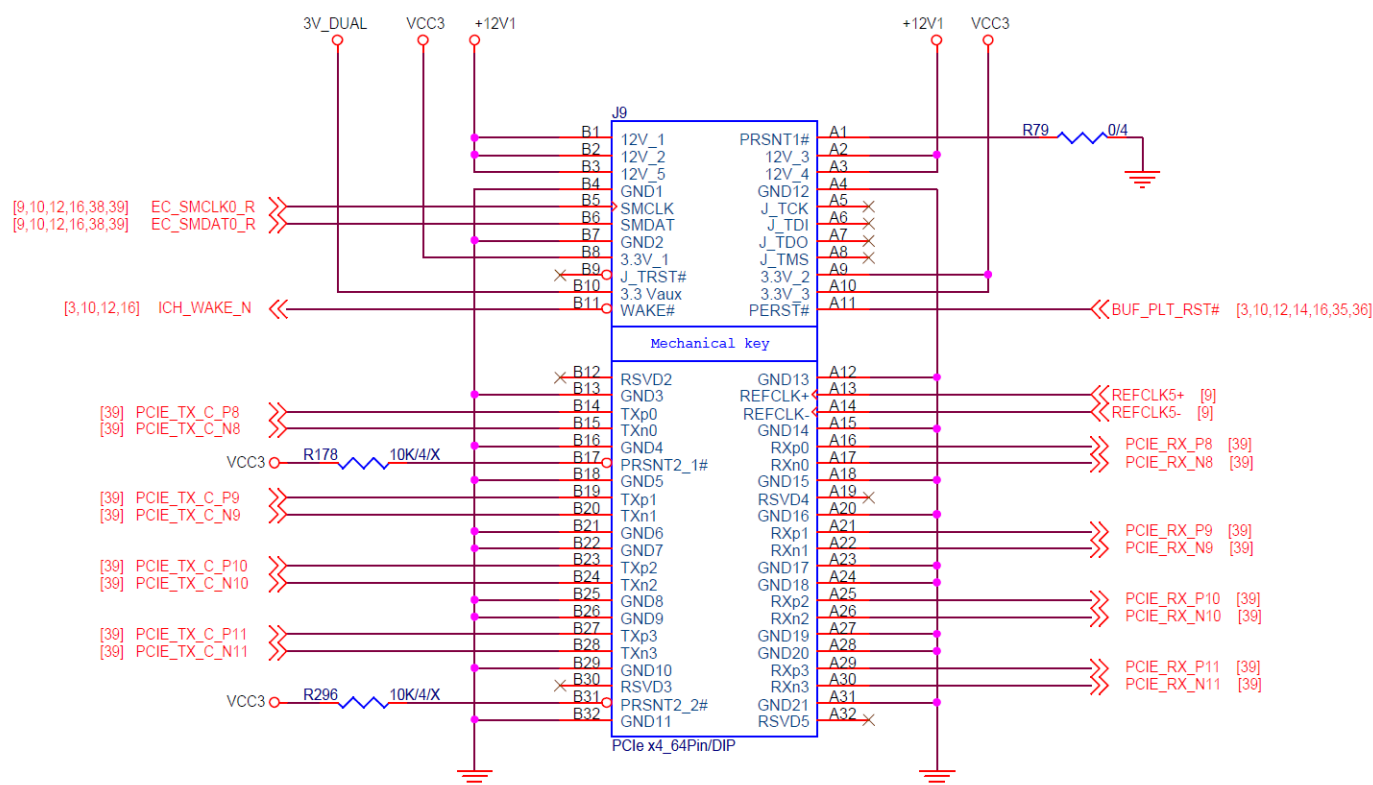


Figure 5 PCIe Reference Schematic

3.1.5 Max Trace Length and Available Carrier Trace Length – PCIE (Gen 3)

Pin	Signal	Max Length	Module length	Available carrier length
C53	PCIE_RX_DN0	14000	2170.41	11829.59
C52	PCIE_RX_DP0	14000	2170.66	11829.34
C56	PCIE_RX_DN1	14000	2301.76	11698.24
C55	PCIE_RX_DP1	14000	2302.23	11697.77
C59	PCIE_RX_DN2	14000	2144.73	11855.27
C58	PCIE_RX_DP2	14000	2144.21	11855.79
C62	PCIE_RX_DN3	14000	2223.59	11776.41
C61	PCIE_RX_DP3	14000	2223.12	11776.88
C66	PCIE_RX_DN4	14000	2059.9	11940.1
C65	PCIE_RX_DP4	14000	2059.53	11940.47
C69	PCIE_RX_DN5	14000	2738.49	11261.51
C68	PCIE_RX_DP5	14000	2738.45	11261.55
C72	PCIE_RX_DN6	14000	2224.04	11775.96
C71	PCIE_RX_DP6	14000	2223.7	11776.3
C75	PCIE_RX_DN7	14000	2608.09	11391.91
C74	PCIE_RX_DP7	14000	2607.63	11392.37
B68	PCIE_RX_DN8	14000	3338.48	10661.52
B69	PCIE_RX_DP8	14000	3338.09	10661.91
B64	PCIE_RX_DN9	14000	2960.55	11039.45
B65	PCIE_RX_DP9	14000	2961.21	11038.79
B61	PCIE_RX_DN10	14000	2825.6	11174.4
B62	PCIE_RX_DP10	14000	2825.06	11174.94
B58	PCIE_RX_DN11	14000	2784.02	11215.98
B59	PCIE_RX_DP11	14000	2783.42	11216.58
B56	PCIE_RX_DN12	14000	2912.54	11087.46
B57	PCIE_RX_DP12	14000	2912.07	11087.93
B52	PCIE_RX_DN13	14000	3185.68	10814.32
B53	PCIE_RX_DP13	14000	3186.34	10813.66
C20	PCIE_RX_DN14_CB	14000	1124.97	12875.03
C19	PCIE_RX_DP14_CB	14000	1124	12876
C23	PCIE_RX_DN15	14000	2107.76	11892.24
C22	PCIE_RX_DP15	14000	2108.54	11891.46
A20	SATA0_PCIE16_RXN	14000	2272.78	11727.22
A19	SATA0_PCIE16_RXP	14000	2272.95	11727.05
B19	SATA1_PCIE17_RXN	14000	2616.59	11383.41

B20	SATA1_PCIE17_RXP	14000	2617.39	11382.61
C3	USB3_PCIE18_RXN0	14000	1861.62	12138.38
C4	USB3_PCIE18_RXP0	14000	1861.19	12138.81
C6	USB3_PCIE19_RXN1	14000	1591.73	12408.27
C7	USB3_PCIE19_RXP1	14000	1591.15	12408.85
D53	PCIE_TX_DN0	14000	1682.39	12317.61
D52	PCIE_TX_DP0	14000	1682.89	12317.11
D56	PCIE_TX_DN1	14000	1627.48	12372.52
D55	PCIE_TX_DP1	14000	1628.43	12371.57
D59	PCIE_TX_DN2	14000	1843.52	12156.48
D58	PCIE_TX_DP2	14000	1844.17	12155.83
D62	PCIE_TX_DN3	14000	1896.43	12103.57
D61	PCIE_TX_DP3	14000	1896.78	12103.22
D66	PCIE_TX_DN4	14000	2103.09	11896.91
D65	PCIE_TX_DP4	14000	2103.92	11896.08
D69	PCIE_TX_DN5	14000	2324.62	11675.38
D68	PCIE_TX_DP5	14000	2325.06	11674.94
D73	PCIE_TX_DN6	14000	2728.69	11271.31
D72	PCIE_TX_DP6	14000	2728.91	11271.09
D75	PCIE_TX_DN7	14000	2867.18	11132.82
D74	PCIE_TX_DP7	14000	2867.16	11132.84
A68	PCIE_TX_DP8	14000	2797.97	11202.03
A69	PCIE_TX_DN8	14000	2797.65	11202.35
A64	PCIE_TX_DP9	14000	2883.68	11116.32
A65	PCIE_TX_DN9	14000	2884.58	11115.42
A61	PCIE_TX_DP10	14000	2886.63	11113.37
A62	PCIE_TX_DN10	14000	2886.79	11113.21
A58	PCIE_TX_DP11	14000	3319.18	10680.82
A59	PCIE_TX_DN11	14000	3319.78	10680.22
A55	PCIE_TX_DP12	14000	3130.88	10869.12
A56	PCIE_TX_DN12	14000	3131.63	10868.37
A52	PCIE_TX_DP13	14000	3384.65	10615.35
A53	PCIE_TX_DN13	14000	3384.99	10615.01
D19	PCIE_TX_DP14_CB	14000	2,053.04	11,946.96
D20	PCIE_TX_DN14_CB	14000	2,054.24	11,945.76
D22	PCIE_TX_DP15	14000	1458.43	12541.57
D23	PCIE_TX_DN15	14000	1459.13	12540.87
A16	SATA0_PCIE16_TXP	14000	2166.89	11833.11
A17	SATA0_PCIE16_TXN	14000	2166.3	11833.7
B16	SATA1_PCIE17_TXP	14000	1823.12	12176.88

B17	SATA1_PCIE17_TXN	14000	1823.09	12176.91
D4	USB3_PCIE18_TXP0	14000	1542.43	12457.57
D3	USB3_PCIE18_TXN0	14000	1542.07	12457.93
D7	USB3_PCIE19_TXP1	14000	1729.81	12270.19
D6	USB3_PCIE19_TXN1	14000	1729.46	12270.54
A89	CLK3_PCIE_N_CN	14000	2771.88	11228.12
A88	CLK3_PCIE_P_CN	14000	2772.33	11227.67

Table 4 Carrier Available Traces – PCIE

3.2 USB 2.0/3.0

PIN OUT

Pin	Signal	Description	I/O	Type	Power / Tolerance	PU / PD	Note
A42	SOC_USB2_DN2	USB differential pairs, channels 2. All USB ports except USB7, if implemented, shall be host ports.	I/O	USB	3.3V Suspend / 3.3V	-	-
A43	SOC_USB2_DP2	USB differential pairs, channels 2. All USB ports except USB7, if implemented, shall be host ports.	I/O	USB	3.3V Suspend / 3.3V	-	-
A45	SOC_USB2_DN0	USB differential pairs, channels 0. All USB ports except USB7, if implemented, shall be host ports.	I/O	USB	3.3V Suspend / 3.3V	-	-
A46	SOC_USB2_DP0	USB differential pairs, channels 0. All USB ports except USB7, if implemented, shall be host ports.	I/O	USB	3.3V Suspend / 3.3V	-	-
B42	SOC_USB2_DN3	USB differential pairs, channels 3. All USB ports except USB7, if implemented, shall be host ports.	I/O	USB	3.3V Suspend / 3.3V	-	-
B43	SOC_USB2_DP3	USB differential pairs, channels 3. All USB ports except USB7, if implemented, shall be host ports.	I/O	USB	3.3V Suspend / 3.3V	-	-
B45	SOC_USB2_DN1	USB differential pairs, channels 1. All USB ports except USB7, if implemented, shall be host ports.	I/O	USB	3.3V Suspend / 3.3V	-	-

B46	SOC_USB2_DP1	USB differential pairs, channels 1. All USB ports except USB7, if implemented, shall be host ports.	I/O	USB	3.3V Suspend / 3.3V	-	-
C3	USB3_PCIE18_RXN0	Additional receive signal differential pairs for the SuperSpeed USB data path.	I	PCIE	AC coupled off Module		
C4	USB3_PCIE18_RXP0	Additional receive signal differential pairs for the SuperSpeed USB data path.	I	PCIE	AC coupled off Module		
C6	USB3_PCIE19_RXN0	Additional receive signal differential pairs for the SuperSpeed USB data path.	I	PCIE	AC coupled off Module		
C7	USB3_PCIE19_RXP0	Additional receive signal differential pairs for the SuperSpeed USB data path.	I	PCIE	AC coupled off Module		
D3	USB3_PCIE18_TXN0	Additional receive signal differential pairs for the SuperSpeed USB data path.	O	PCIE	AC coupled on Module		
D4	USB3_PCIE18_TXP0	Additional receive signal differential pairs for the SuperSpeed USB data path.	O	PCIE	AC coupled on Module		
D6	USB3_PCIE19_TXN0	Additional receive signal differential pairs for the SuperSpeed USB data path.	O	PCIE	AC coupled on Module		
D7	USB3_PCIE19_TXP0	Additional receive signal differential pairs for the SuperSpeed USB data path.	O	PCIE	AC coupled on Module		

Table 5 USB Pin Out

3.2.1 PCB Layout Guideline – USB 2.0 / 3.0

Parameter	Trace Routing
Transfer rate / Port	480 MBit/s
Maximum signal line length (coupled traces)	Max. 17.0 inches
Signal length used on COM Express Module (including the COM Express connector)	3.0 inches
Signal length allowance for the COM Express Carrier Board	14.0 inches
Differential Impedance	90 Ω +/-15%
Single-ended Impedance	45 Ω +/-10%
Trace width (W)	PCB stack-up dependent
Spacing between differential pairs (intra-pair) (S)	PCB stack-up dependent
Spacing between pairs-to-pairs (inter-pair) (s)	Min. 20mils
Spacing between differential pairs and high-speed periodic signals	Min. 50mils
Spacing between differential pairs and low-speed non periodic signals	Min. 20mils
Length matching between differential pairs (intra-pair)	150mils
Reference plane	GND referenced preferred
Spacing from edge of plane	Min. 40mils
Via Usage	Try to minimize number of vias

Table 6 Layout Guideline – USB 2.0

Parameter	Trace Routing
Transfer rate / Port	5.0 GBit/s
Maximum signal line length (coupled traces)	7.5 inches
Signal length used on COM Express Module (including the COM Express connector)	3.0 inches
Signal length allowance for the COM Express Carrier Board	4.5 inches
Differential Impedance	85 Ω +/-10%
Single-ended Impedance	50 Ω +/-15%
Trace width (W)	PCB stack-up dependent
Spacing between differential pairs (intra-pair) (S)	PCB stack-up dependent
Spacing between pairs-to-pairs (inter-pair) (s)	Min. 15mils
Spacing between differential pairs and high-speed periodic signals	Min. 15mils
Spacing between differential pairs and low-speed non periodic signals	Min. 20mils
Length matching between differential pairs (intra-pair)	Max. 5mils
Reference plane	Ground
Spacing from edge of plane	Min. 40mils
Via Usage	Max. 3 vias per differential signal trace

Table 7 Layout Guideline – USB 3.0

3.2.2 Reference Schematic – USB 2.0 / 3.0

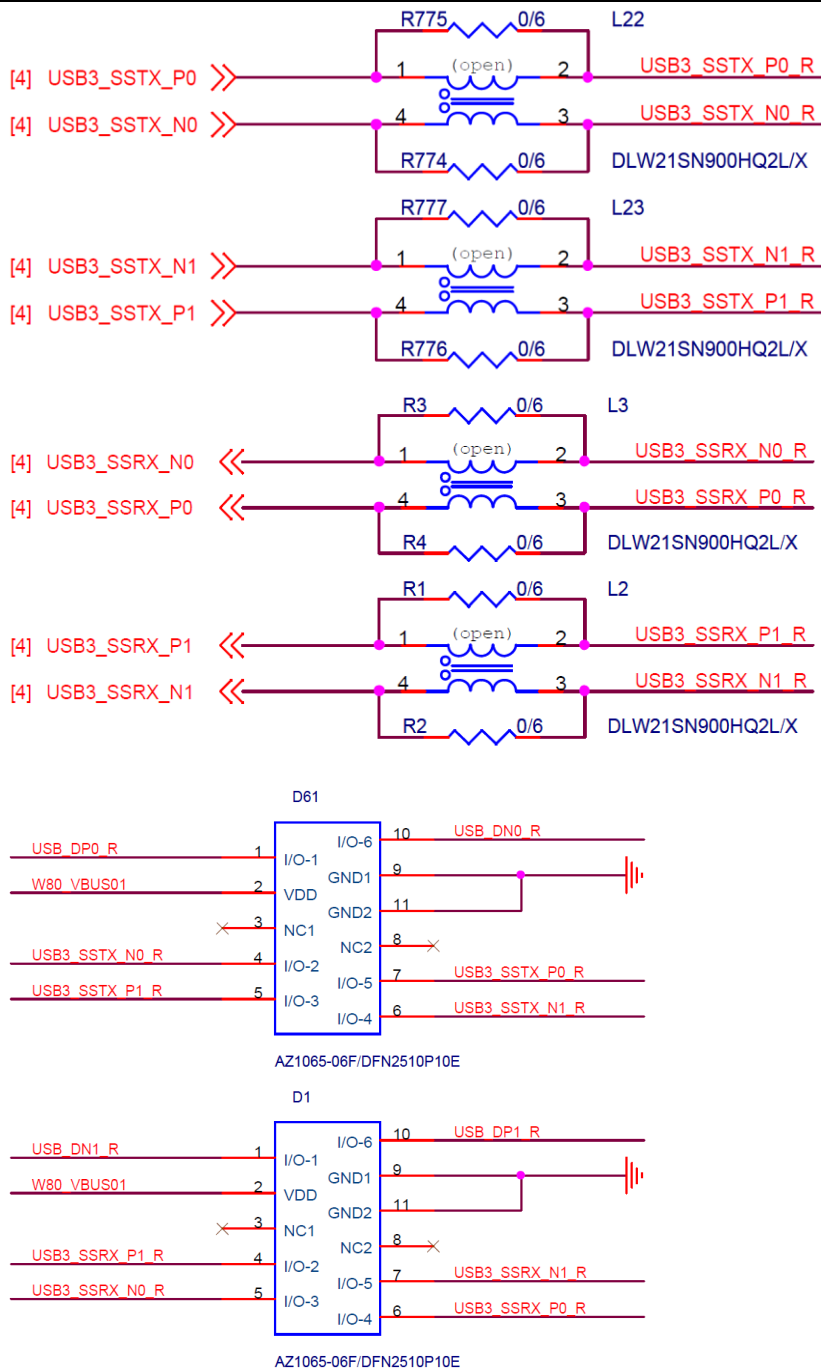


Figure 6 USB 2.0 / 3.0 Reference Schematic 1

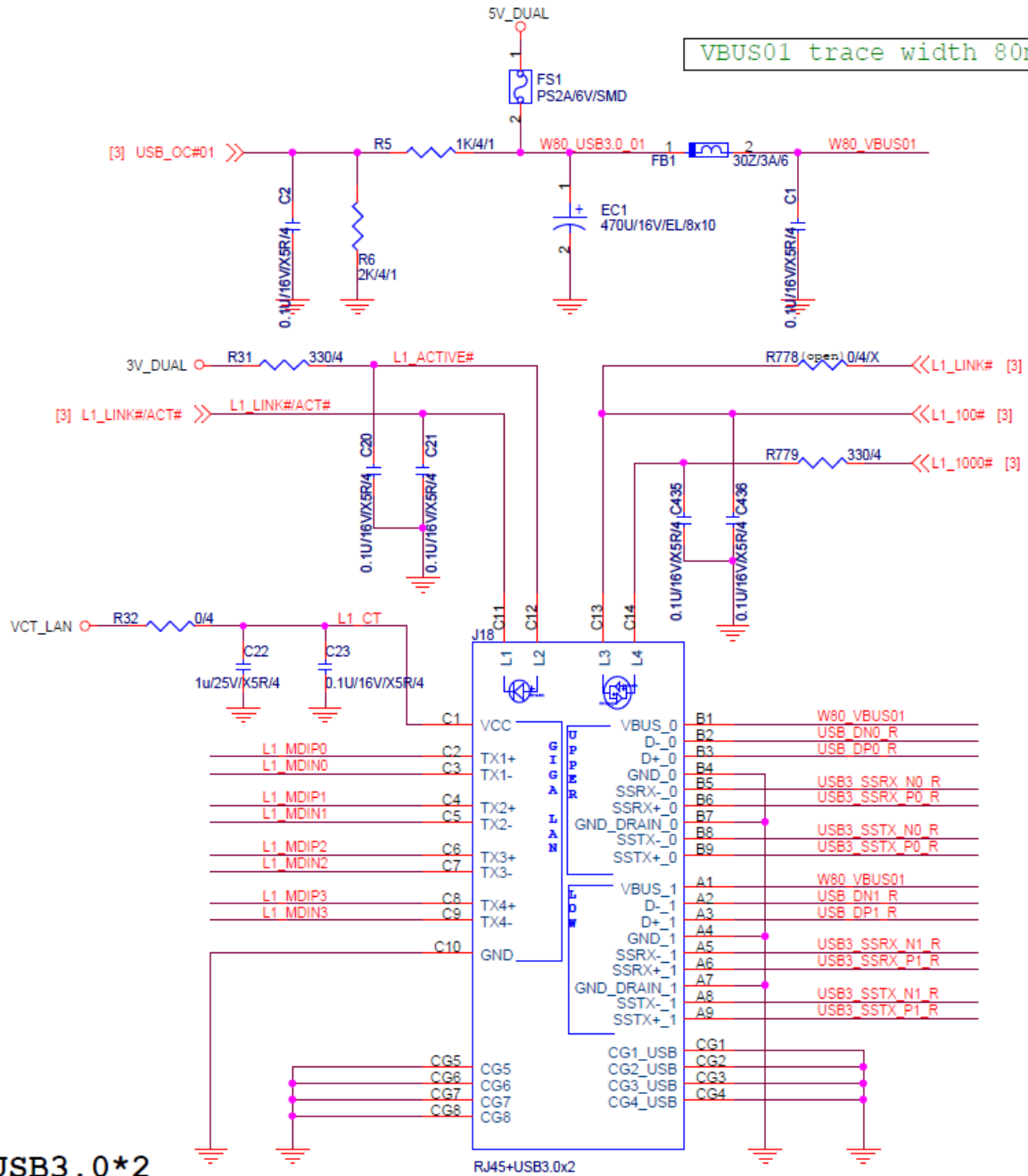


Figure 7 USB 2.0/3.0 Reference Schematic 2

3.2.3 Max Trace Length and Available Carrier Trace Length - USB 2.0 / 3.0

Pin	Signal	Max Length	Module length	Available carrier length
A42	SOC_USB2_DN2	17000	3465.75	13534.25
A43	SOC_USB2_DP2	17000	3466.41	13533.59
A45	SOC_USB2_DN0	17000	3305.39	13694.61
A46	SOC_USB2_DP0	17000	3304.99	13695.01
B42	SOC_USB2_DN3	17000	2193.46	14806.54
B43	SOC_USB2_DP3	17000	2192.72	14807.28
B45	SOC_USB2_DN1	17000	2413.32	14586.68
B46	SOC_USB2_DP1	17000	2413.62	14586.38
C3	USB3_PCIE18_RXN0	7500	1861.62	5638.38
C4	USB3_PCIE18_RXP0	7500	1861.19	5638.81
C6	USB3_PCIE19_RXN1	7500	1591.73	5908.27
C7	USB3_PCIE19_RXP1	7500	1591.15	5908.85
D4	USB3_PCIE18_TXP0	7500	1542.43	5957.57
D3	USB3_PCIE18_TXN0	7500	1542.07	5957.93
D7	USB3_PCIE19_TXP1	7500	1729.81	5770.19
D6	USB3_PCIE19_TXN1	7500	1729.46	5770.54

Table 8 Carrier Available Traces – USB 2.0 / 3.0

3.3 GbE LAN

External Ethernet magnetics shall be implemented on the Carrier Board.

PIN OUT

Pin	Signal	Description	I/O	Type	Power / Tolerance	PU / PD	Note
A2	L1_MDIN3	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs	I/O	Analog	3.3V max Suspend	-	-
A3	L1_MDIP3	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs	I/O	Analog	3.3V max Suspend	-	-
A4	L1_100#	Gigabit Ethernet Controller 0 100 Mbit / sec link indicator, active low.	OD	CMOS	3.3V Suspend / 3.3V	-	-
A5	L1_1000#	Gigabit Ethernet Controller 0 1000 Mbit / sec link indicator, active low.	OD	CMOS	3.3V Suspend / 3.3V	-	-
A6	L1_MDIN2	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs	I/O	Analog	3.3V max Suspend	-	-
A7	L1_MDIP2	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs	I/O	Analog	3.3V max Suspend	-	-
A8	L1_LINK#	Gigabit Ethernet Controller 0 link indicator, active low.	OD	CMOS	3.3V Suspend / 3.3V	PU 10k ohm to 3VSB	-
A9	L1_MDIN1	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs	I/O	Analog	3.3V max Suspend	-	-
A10	L1_MDIP1	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs	I/O	Analog	3.3V max Suspend	-	-
A12	L1_MDIN0	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs	I/O	Analog	3.3V max Suspend	-	-
A13	L1_MDIP0	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs	I/O	Analog	3.3V max Suspend	-	-

A49	GBE0_SDP	Gigabit Ethernet Controller 0 Software-Definable Pins. Can also be used for	I/O	CMOS	3.3V Suspend /		-
B2	L1_LINK#/ACT#	Gigabit Ethernet Controller 1 activity indicator, active low.	OD	CMOS	3.3V Suspend / 3.3V	-	-

Table 9 GbE LAN Pin Out

3.3.1 PCB Layout Guideline - GbE LAN

Parameter	Trace Routing
Signal length allowance for the COM Express Carrier Board	5.0 inches from the COM Express Module to the magnetics Module
Maximum signal length between isolation magnetics Module and RJ45 connector on the Carrier Board	1.0 inch
Differential Impedance	95 Ω +/-20%
Single-ended Impedance	55 Ω +/-15%
Trace width (W)	PCB stack-up dependent
Spacing between differential pairs (intra-pair) (S)	PCB stack-up dependent
Spacing between RX and TX pairs (inter-pair) (s)	Min. 50mils
Spacing between differential pairs and high-speed periodic signals	Min. 300mils
Spacing between differential pairs and low-speed non periodic signals	Min. 100mils
Length matching between differential pairs (intra-pair)	Max. 5mils
Length matching between RX and TX pairs (inter-pair)	Max. 30mils
Spacing between digital ground and analog ground plane (between the magnetics Module and RJ45 connector)	Min. 60mils
Spacing from edge of plane	Min. 40mils
Via Usage	Max. of 2 vias on TX path Max. of 2 vias on RX path

Table 10 Layout Guideline – GbE LAN

3.3.2 Max Trace Length and Available Carrier Trace Length – GbE LAN

Pin	Signal	Max Length	Module length	Available carrier length
A2	L1_MDIN3	8000	753.08	7246.92
A3	L1_MDIP3	8000	753.51	7246.49
A6	L1_MDIN2	8000	731.87	7268.13
A7	L1_MDIP2	8000	731.57	7268.43
A9	L1_MDIN1	8000	735.95	7264.05
A10	L1_MDIP1	8000	735.58	7264.42
A12	L1_MDIN0	8000	818.06	7181.94
A13	L1_MDIP0	8000	818.57	7181.43

Table 11 Carrier Available Traces – GbE LAN

3.4 SATA

PIN OUT

Pin	Signal	Description	I/O	Type	Power / Tolerance	PU / PD	Note
A16	SATA0_PCIE16_TXP	Serial ATA or SAS Channel 0 transmit differential pair.	O	SATA	AC coupled on Module	-	-
A17	SATA0_PCIE16_TXN	Serial ATA or SAS Channel 0 transmit differential pair.	O	SATA	AC coupled on Module	-	-
A19	SATA0_PCIE16_RXP	Serial ATA or SAS Channel 0 receive differential pair.	I	SATA	AC coupled on Module	-	-
A20	SATA0_PCIE16_RXN	Serial ATA or SAS Channel 0 receive differential pair.	I	SATA	AC coupled on Module	-	-
B16	SATA1_PCIE17_TXP	Serial ATA or SAS Channel 1 transmit differential pair.	O	SATA	AC coupled on Module	-	-
B17	SATA1_PCIE17_TXN	Serial ATA or SAS Channel 1 transmit differential pair.	O	SATA	AC coupled on Module	-	-
B19	SATA1_PCIE17_RXP	Serial ATA or SAS Channel 1 receive differential pair.	I	SATA	AC coupled on Module	-	-
B20	SATA1_PCIE17_RXN	Serial ATA or SAS Channel 1 receive differential pair.	I	SATA	AC coupled on Module	-	-

Table 12 SATA Pin Out

3.4.1 PCB Layout Guideline - SATA

Parameter	Trace Routing
Transfer Rate	Up to 6.0 GBit/s
Maximum signal line length (coupled traces)	5.0 inches on PCB (COM Express Module and Carrier Board. The length of the SATA cable is specified between 0 and 40 inches)
Signal length used on COM Express Module (including the COM Express Carrier Board connector)	2 inches
Signal length available for the COM Express Carrier Board	3 inches, a redriver may be necessary for GEN3 signaling rates
Differential Impedance	85 Ω +/-20%
Single-ended Impedance	50 Ω +/-15%
Trace width (W)	PCB stack-up dependent
Spacing between differential pairs (intra-pair) (S)	PCB stack-up dependent
Spacing between RX and TX pairs (inter-pair) (s)	Min. 20mils
Spacing between differential pairs and high-speed periodic signals	Min. 50mils
Spacing between differential pairs and low-speed non periodic signals	Min. 20mils
Length matching between differential pairs (intra-pair)	Max. 5mils
Length matching between RX and TX pairs (inter-pair)	No strict length-matching requirements. Route the signals as directly as possible.
Spacing from edge of plane	Min. 40mils
Via Usage	A maximum of 2 vias is recommended.
AC Coupling capacitors	The AC coupling capacitors for the TX and RX lines are incorporated on the COM Express Module.

Table 13 Layout Guideline – SATA

3.4.2 Max Trace Length and Available Carrier Trace Length - SATA

Pin	Signal	Max Length	Module length	Available carrier length
A16	SATA0_PCIE16_TXP	5000	2272.95	2727.05
A17	SATA0_PCIE16_TXN	5000	2272.78	2727.22
A19	SATA0_PCIE16_RXP	5000	2166.89	2833.11
A20	SATA0_PCIE16_RXN	5000	2166.3	2833.7
B16	SATA1_PCIE17_TXP	5000	2617.39	2382.61
B17	SATA1_PCIE17_TXN	5000	2616.59	2383.41
B19	SATA1_PCIE17_RXP	5000	1823.12	3176.88
B20	SATA1_PCIE17_RXN	5000	1823.09	3176.91

Table 14 Carrier Available Traces – SATA

3.5 NCSI

PIN OUT

Pin	Signal	Description	I/O	Type	Power / Tolerance	PU / PD	Note
A84	NCSI_TX_EN_CN	NCSI Transmit Enable	I	-	3.3V Suspend / 3.3V		-
B89	NCSI_RX_ER_CN	NC-SI Receive error	O	-	3.3V Suspend / 3.3V	NC	-
B91	NCSI_CLK_IN	NC-SI Clock reference for receive, transmit, and control interface.	I	-	3.3V Suspend / 3.3V	-	-
B92	NCSI_RXD_1	NC-SI Receive Data (from NC to BMC).	O	-	3.3V Suspend / 3.3V	Placeholder PU 10K to 3VSB	-
B93	NCSI_RXD_0	NC-SI Receive Data (from NC to BMC).	O	-	3.3V Suspend / 3.3V	Placeholder PU 10K to 3VSB	-
B94	NCSI_CRS_DV	NC-SI Carrier Sense/Receive Data Valid to MC, indicating that the transmitted data from NC to BMC is valid.	O	-	3.3V Suspend / 3.3V	Placeholder PD 10K	-
B95	NCSI_TXD_1_CN	NC-SI Transmit Data (from BMC to NC).	I	-	3.3V Suspend / 3.3V	PD 10K	-
B96	NCSI_TXD_0_CN	NC-SI Transmit Data (from BMC to NC).	I	-	3.3V Suspend / 3.3V	PD 10K	-
B98	NCSI_ARB_IN_CN	NC-SI hardware arbitration input.	I	-	3.3V Suspend / 3.3V	PU 10k ohm to 3VSB	-
B99	NCSI_ARB_OUT	NC-SI hardware arbitration output.	O	-	3.3V Suspend / 3.3V		-

Table 15 NCSI Pin Out

3.5.1 Max Trace Length and Available Carrier Trace Length - NCSI

Pin	Signal	Max Length	Module length	Available carrier length
A84	NCSI_TX_EN	10000	4721.36	5278. 64
B91	NCSI_CLK_IN	10000	5789.04	4210. 96
B92	NCSI_RXD1	10000	4,634.24	5365. 76
B93	NCSI_RXD0	10000	5154.84	4845. 16
B94	NCSI_CRS_DV	10000	4660.09	5339. 91
B95	NCSI_TXD1	10000	4874.47	5125. 53
B96	NCSI_TXD0	10000	5055.38	4944. 62
B98	NCSI_ARB_IN	14000	3704.87	10295. 13
B99	NCSI_ARB_OUT	14000	7049.95	6950. 05

Table 16 Carrier Available Traces – NCSI

3.6 10GbE LAN

Pin out

Pin	Signal	Description	I/O	Type	Power / Tolerance	PU / PD	Note
D26	LAN1_TX_DP1	10GBASE-KR ports, transmit output differential pairs.	O	KR	AC coupled at receiver	-	-
D27	LAN1_TX_DN1	10GBASE-KR ports, transmit output differential pairs.	O	KR	AC coupled at receiver	-	-
D29	LAN1_TX_DP0	10GBASE-KR ports, transmit output differential pairs.	O	KR	AC coupled at receiver	-	-
D30	LAN1_TX_DN0	10GBASE-KR ports, transmit output differential pairs.	O	KR	AC coupled at receiver	-	-
D32	LAN1_P1_I2C_CLK	I2C clock signal of the 2-wire management interface used by the 10GbE controller to access the management registers of an external Optical SFP Module.	I/O	CMOS	3.3V Suspend / 3.3V	Module PU 1kohm to 3.3V	-
D33	LAN1_P0_I2C_CLK	I2C clock signal of the 2-wire management interface used by the 10GbE controller to access the management registers of an external Optical SFP Module.	I/O	CMOS	3.3V Suspend / 3.3V	Module PU 1kohm to 3.3V	-
C26	LAN1_RX_DP1	10GBASE-KR ports, receive input differential pairs.	I	KR	AC coupled on Module	-	-
C27	LAN1_RX_DN1	10GBASE-KR ports, receive input differential pairs.	I	KR	AC coupled on Module	-	-
C29	LAN1_RX_DP0	10GBASE-KR ports, receive input differential pairs.	I	KR	AC coupled on Module	-	-
C30	LAN1_RX_DN0	10GBASE-KR ports, receive input differential pairs.	I	KR	AC coupled on Module	-	-
C15	10PHY_MDC3_CN	MDIO Mode / I2C Mode	O, I/O	CMOS	3.3V Suspend / 3.3V	-	Not connected

C16	10PHY_MDC2_CN	MDIO Mode / I2C Mode	O, I/O	CMOS	3.3V Suspend / 3.3V	-	Not connected
C24	10G_INT2_CN	Interrupt pin from copper PHY or optical SFP Module to the 10GbE controller.	I	CMOS	3.3V Suspend / 3.3V	-	Not connected
D15	10G_PHY_MDIO_SDA3	MDIO Mode / I2C Mode	O, I/O	CMOS	3.3V Suspend / 3.3V	-	Not connected
D16	10G_PHY_MDIO_SDA2	MDIO Mode / I2C Mode	O, I/O	CMOS	3.3V Suspend / 3.3V	-	Not connected
D34	10GPHY_SEL23_CN	Indicates if the PHY for 10G lanes 2 and 3 is capable of configuration by I ² C. High indicates MDIO-only configuration, and low indicates configuration capability via I ² C or MDIO.	I	CMOS	3.3V Suspend / 3.3V	-	Not connected
D35	10GPHY_SEL01_CN	Indicates if the PHY for 10G lanes 0 and 1 is capable of configuration by I ² C. High indicates MDIO-only configuration, and low indicates configuration capability via I ² C or MDIO.	I	CMOS	3.3V Suspend / 3.3V	-	Not connected
D38	LAN0_P1_I2C_CLK	I2C clock signal of the 2-wire management interface used by the 10GbE controller to access the management registers of an external Optical SFP Module.	I/O	CMOS	3.3V Suspend / 3.3V	Module PU 1kohm to 3.3V	-
D39	LAN0_P0_I2C_CLK	I2C clock signal of the 2-wire management interface used by the 10GbE controller to access the management registers of an external Optical SFP Module.	I/O	CMOS	3.3V Suspend / 3.3V	Module PU 1kohm to 3.3V	-
D40	LAN0_PORT1_SDP0	Software-Definable Pins. Can	I/O	CMOS	3.3V	-	-

		also be used for IEEE1588 support such as a 1pps signal.			Suspend / 3.3V		
D42	LAN0_TX_DP1	10GBASE-KR ports, transmit output differential pairs.	O	KR	AC coupled at receiver	-	-
D43	LAN0_TX_DN1	10GBASE-KR ports, transmit output differential pairs.	O	KR	AC coupled at receiver	-	-
D45	10PHY_MDA1_CN	MDIO Mode / I2C Mode	O, I/O	CMOS	3.3V Suspend / 3.3V	Module PU 1kohm to 3.3V	
D46	10PHY_MDA0_CN	MDIO Mode / I2C Mode	O, I/O	CMOS	3.3V Suspend / 3.3V	Module PU 1kohm to 3.3V	-
D47	10G_INT1_CN	Interrupt pin from copper PHY or optical SFP Module to the 10GbE controller.	I	CMOS	3.3V Suspend / 3.3V	-	Not connected
D49	LAN0_TX_DP0	10GBASE-KR ports, transmit output differential pairs.	O	KR	AC coupled at receiver	-	-
D50	LAN0_TX_DN0	10GBASE-KR ports, transmit output differential pairs.	O	KR	AC coupled at receiver	-	-
C32	LAN1_P1_I2C_DAT	I2C data signal of the 2-wire management interface used by the 10GbE controller to access the management registers of an external Optical SFP Module.	I/O	CMOS	3.3V Suspend / 3.3V	Module PU 1kohm to 3.3V	-
C33	LAN1_P0_I2C_DAT	I2C data signal of the 2-wire management interface used by the 10GbE controller to access the management registers of an external Optical SFP Module.	I/O	CMOS	3.3V Suspend / 3.3V	Module PU 1kohm to 3.3V	-
C34	10GPHY_RST23_CN	Output signal that resets an optical PHY on port 2 and port 3 (with copper PHY this signal is not used).	O	CMOS	3.3V Suspend / 3.3V	-	
C35	10GPHY_RST01_CN	Output signal that resets an optical PHY on port 0 and	O	CMOS	3.3V Suspend /	-	

		port1 (with copper PHY this signal is not used).			3.3V		
.C39	LAN0_P0_I2C_DAT	I2C data signal of the 2-wire management interface used by the 10GbE controller to access the management registers of an external Optical SFP Module.	I/O	CMOS	3.3V Suspend / 3.3V	Module PU 1kohm to 3.3V	-
C40	LAN0_PORT0_SDP0	Software-Definable Pins. Can also be used for IEEE1588 support such as a 1pps signal.	I/O	CMOS	3.3V Suspend / 3.3V	-	-
C42	LAN0_RX_DP1	10GBASE-KR ports, receive input differential pairs.	I	KR	AC coupled on Module	-	-
C43	LAN0_RX_DN1	10GBASE-KR ports, receive input differential pairs.	I	KR	AC coupled on Module	-	-
C45	10PHY_MDC1_CN	MDIO Mode / I2C Mode	O	-	3.3V Suspend / 3.3V	- Placeholder 0 ohm to LAN_MDC	-
C46	10PHY_MDC0_CN	MDIO Mode / I2C Mode	O, I/O	CMOS	3.3V Suspend / 3.3V	Module PU 1kohm to 3.3V	-
C47	10G_INT0_CN	Interrupt pin from copper PHY or optical SFP Module to the 10GbE controller.	I	CMOS	3.3V Suspend / 3.3V	-	Not connected
C49	LAN0_RX_DP0	10GBASE-KR ports, receive input differential pairs.	I	KR	AC coupled on Module	-	-
C50	LAN0_RX_DN0	10GBASE-KR ports, receive input differential pairs.	I	KR	AC coupled on Module	-	-
C36	10G_LED_SDA_CN	I2C Data of the 2-wire interface that transfers LED signals and PHY straps for I2C or MDIO operation of optical PHYs.	I/O	CMOS	3.3V Suspend / 3.3V	-	-
C37	10G_LED_SCL_CN	I2C Clock of the 2-wire interface that transfers LED and strap signals for I2C or MDIO operation of optical PHYs.	I/O	CMOS	3.3V Suspend / 3.3V	-	-
C38	LAN0_P1_I2C_DAT	I2C data signal of the 2-wire management interface used by	I/O	CMOS	3.3V Suspend /	Module PU 1kohm to	-

		the 10GbE controller to access the management registers of an external Optical SFP Module.			3.3V	3.3V	
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Table 17 10GbE LAN Pin Out

3.6.1 Max Trace Length and Available Carrier Trace Length – 10GbE LAN

Pin	Signal	Max Length	Module length	Available carrier length
D26	LAN1_TX_DP1	6000	736.49	5263.51
D27	LAN1_TX_DN1	6000	736.07	5263.93
D29	LAN1_TX_DP0	6000	694.87	5305.13
D30	LAN1_TX_DN0	6000	693.99	5306.01
D32	LAN1_P1_I2C_CLK	16000	2079.22	13920.78
D33	LAN1_P0_I2C_CLK	16000	2736.32	13263.68
C26	LAN1_RX_DP1	6000	1178.87	4821.13
C27	LAN1_RX_DN1	6000	1179.29	4820.71
C29	LAN1_RX_DP0	6000	1230.29	4769.71
C30	LAN1_RX_DN0	6000	1230.98	4769.02
D38	LAN0_P1_I2C_CLK	16000	2818.5	13181.5
D39	LAN0_P0_I2C_CLK	16000	3323.78	12676.22
D42	LAN0_TX_DP1	6000	1297.47	4702.53
D43	LAN0_TX_DN1	6000	1297.61	4702.39
D46	10PHY_MDA0_CN	16000	3254.69	12745.31
D49	LAN0_TX_DP0	6000	1280.14	4719.86
D50	LAN0_TX_DN0	6000	1280.66	4719.34
C32	LAN1_P1_I2C_DAT	16000	1683.04	14316.96
C33	LAN1_P0_I2C_DAT	16000	2825.66	13174.34
C39	LAN0_P0_I2C_DAT	16000	3336.91	12663.09
C42	LAN0_RX_DP1	6000	1708.96	4291.04
C43	LAN0_RX_DN1	6000	1708.95	4291.05
C46	10PHY_MDC0_CN	16000	3800.76	12199.24
C49	LAN0_RX_DP0	6000	1631.12	4368.88
C50	LAN0_RX_DN0	6000	1631.86	4368.14
C36	10G_LED_SDA_CN	10000	2712.65	7287.35
C37	10G_LED_SCL_CN	10000	2538.44	7461.56
C38	LAN0_P1_I2C_DAT	16000	2993.76	13006.24

Table 18 Carrier Available Traces – 10GbE LAN

3.7 UART

PIN OUT

Pin	Signal	Description	I/O	Type	Power / Tolerance	PU / PD	Note
A50	SOC_LPC_SERIRQ	LPC serial interrupt / Shared pin with ESPI_CS1#	I/O	CMOS	3.3V / 3.3V	PU 10K ohm to 3.3V	-
A98	SER0_TX	General purpose serial port transmitter	O	CMOS	3.3V / 12V	Placeholder PD 4.7K	-
A99	SER0_RX	General purpose serial port receiver	I	CMOS	3.3V / 12V	Go through diode PU 47K to 3.3V	-
A101	SER1_TX	General purpose serial port transmitter / CAN_TX	O	CMOS	3.3V / 12V	Placeholder PD 4.7K	-
A102	SER1_RX	General purpose serial port receiver / CAN_RX	I	CMOS	3.3V / 12V	Go through diode PU 47K to 3.3V	-

Table 19 UART Pin Out

3.7.1 Reference Schematic - UART

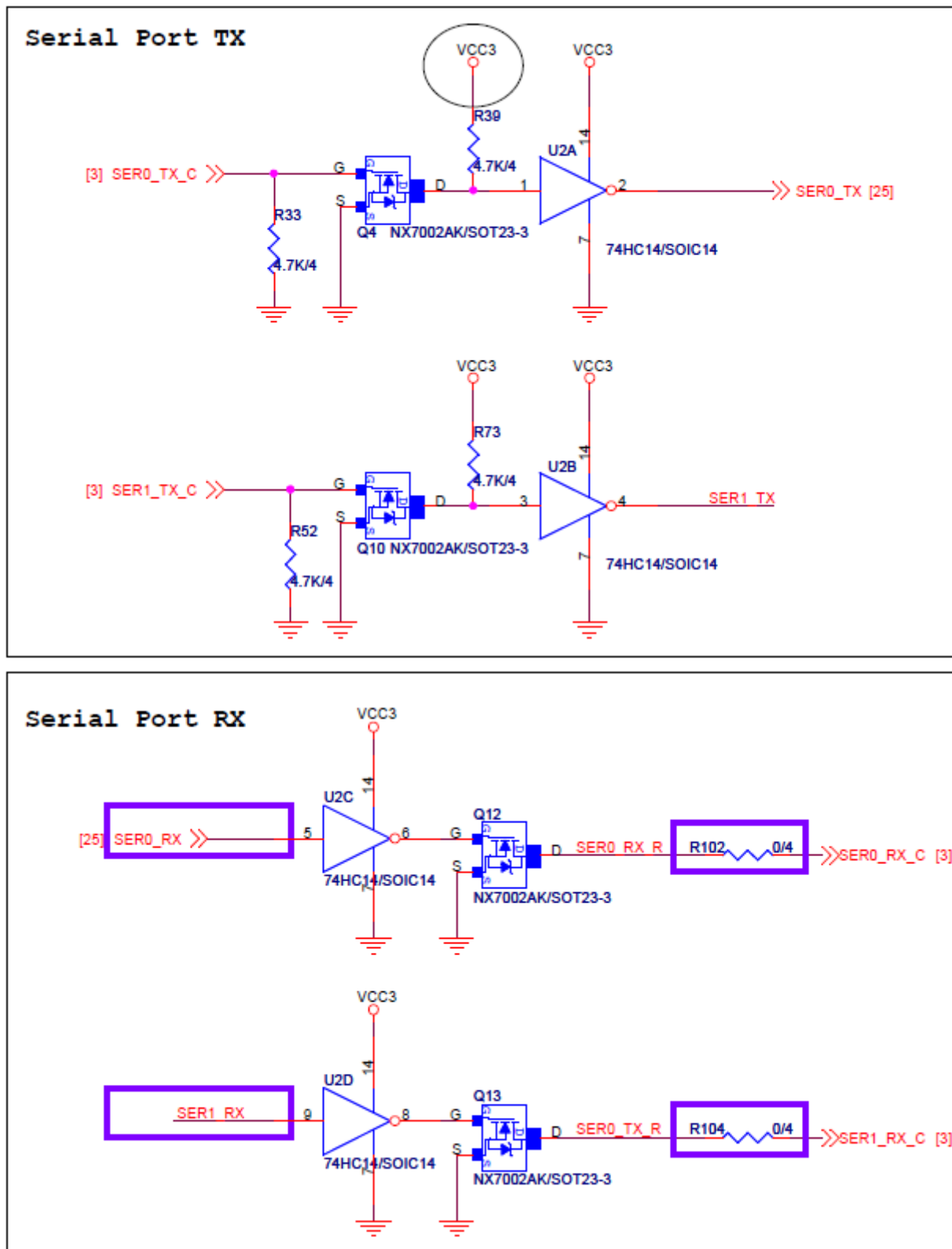


Figure 8 UART Reference Schematic 1

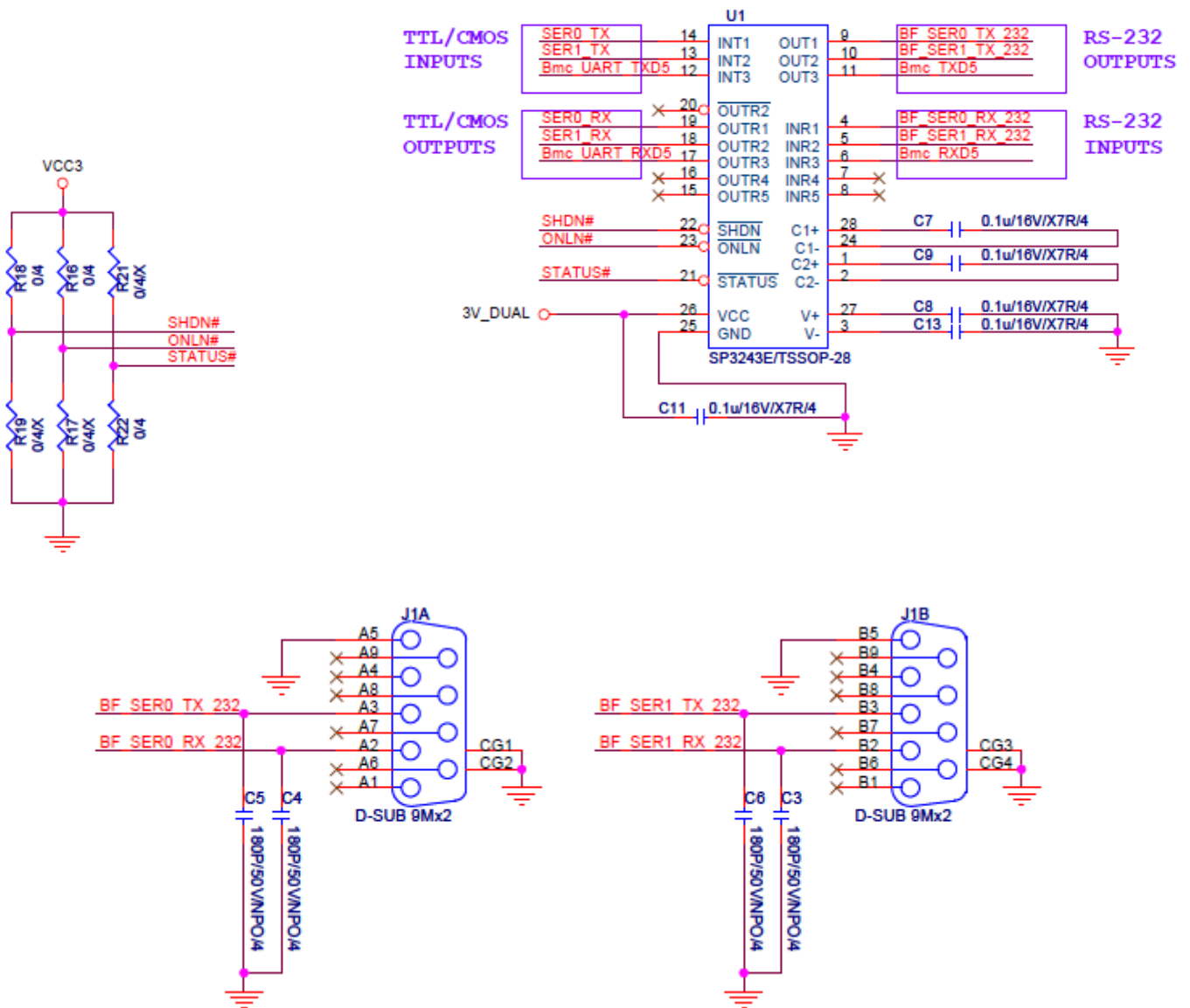


Figure 9 UART Reference Schematic 2

3.8 I2C

PIN OUT

Pin	Signal	Description	I/O	Type	Power / Tolerance	PU / PD	Note
B33	I2C_CLK_CN	General purpose I2C port clock output	I/O	CMOS	3.3V Suspend / 3.3V	Placeholder PU 10k ohm to 3.3V	-
B34	I2C_DAT_CN	General purpose I2C port data I/O line	I/O	CMOS	3.3V Suspend / 3.3V	Placeholder PU 10k ohm to 3.3V	-

Table 20 I2C Pin Out

3.9 SMBus

PIN OUT

Pin	Signal	Description	I/O	Type	Power / Tolerance	PU / PD	Note
B13	SMB_CLK_CN	System Management Bus bidirectional clock line.	I/O	CMOS	3.3V Suspend / 3.3V	Placeholder 0 ohm	-
B14	SMB_DATA_CN	System Management Bus bidirectional data line.	I/O	CMOS	3.3V Suspend / 3.3V	Placeholder 0 ohm	-
B15	SMB_ALRT_N_CN	System Management Bus Alert – active low input can be used to generate an SMI# (System Management Interrupt) or to wake the system.	I	CMOS	3.3V Suspend / 3.3V	Go through 0 ohm	-

Table 21 SMBus Pin Out

3.10 GPIO

PIN OUT

Pin	Signal	Description	I/O	Type	Power / Tolerance	PU / PD	Note
A54	GPI0	General purpose input pins. Pulled high internally on the Module.	I	CMOS	3.3V / 3.3V	PU 10k ohm to 3.3V	-
A63	GPI1	General purpose input pins. Pulled high internally on the Module.	I	CMOS	3.3V / 3.3V	PU 10k ohm to 3.3V	-
A67	GPI2	General purpose input pins. Pulled high internally on the Module.	I	CMOS	3.3V / 3.3V	PU 10k ohm to 3.3V	-
A85	GPI3	General purpose input pins. Pulled high internally on the Module.	I	CMOS	3.3V / 3.3V	PU 10k ohm to 3.3V	-
A93	GPO0	General purpose output pins. Upon a hardware reset, these outputs should be low.	O	CMOS	3.3V / 3.3V	-	-
B54	GPO1	General purpose output pins. Upon a hardware reset, these outputs should be low.	O	CMOS	3.3V / 3.3V	-	-
B57	GPO2	General purpose output pins. Upon a hardware reset, these outputs should be low.	O	CMOS	3.3V / 3.3V	-	-
B63	GPO3	General purpose output pins. Upon a hardware reset, these outputs should be low.	O	CMOS	3.3V / 3.3V	-	-

Table 22 GPIO Pin Out

3.11 LPC

PIN OUT

Pin	Signal	Description	I/O	Type	Power / Tolerance	PU / PD	Note
A50	SOC_LPC_SERIRQ	LPC serial interrupt / Shared pin with ESPI_CS1#	I/O	CMOS	3.3V / 3.3V	PU 10K ohm to 3.3V	-
B3	SOC_LPC_FRAME_N	LPC frame indicates the start of an LPC cycle / Shared pin with ESPI_CS0#	O	CMOS	3.3V / 3.3V	PU 8.2k ohm to 3.3V	-
B4	SOC_LPC_AD0	LPC multiplexed address, command and data bus / Shared pin with ESPI IO	I/O	CMOS	3.3V / 3.3V	-	-
B5	SOC_LPC_AD1	LPC multiplexed address, command and data bus / Shared pin with ESPI IO	I/O	CMOS	3.3V / 3.3V	-	-
B6	SOC_LPC_AD2	LPC multiplexed address, command and data bus / Shared pin with ESPI IO	I/O	CMOS	3.3V / 3.3V	-	-
B7	SOC_LPC_AD3	LPC multiplexed address, command and data bus / Shared pin with ESPI IO	I/O	CMOS	3.3V / 3.3V	-	-
B8	LPC_DRQ0# / ESPI_ALERT0#	LPC serial DMA request / Shared pin with ESPI_ALERT	I	CMOS	3.3V / 3.3V	-	-
B9	LPC_DRQ1# / ESPI_ALERT1#	LPC serial DMA request / Shared pin with ESPI_ALERT	I	CMOS	3.3V / 3.3V	-	-
B10	LPC_CLK1_CE	LPC clock output - 33MHz nominal / Shared pin with ESPI_Clock	O	CMOS	3.3V / 3.3V	-	-

Table 23 LPC Pin Out

3.12 SPI

An external SPI BIOS is designed on the Carrier board, which allows the Module boot from the Carrier SPI BIOS. To achieve this function, the BIOS_DIS0# and BIOS_DIS1# must be designed as a selectable method on the Carrier.

PIN OUT

Pin	Signal	Description	I/O	Type	Power / Tolerance	PU / PD	Note
A34	BIOS_DIS0#	Selection straps to determine the BIOS boot device. The Carrier should only float these or pull them low. Shared pin with ESPI_SAFS	I	CMOS	NA	PU 10K ohm to 3.3V	-
A92	SPI_MISO_CN	Data into Module from Carrier SPI	I	CMOS	3.3V Suspend / 3.3V	-	-
A94	SPI_CLK_CN	Clock from Module to Carrier SPI	O	CMOS	3.3V Suspend / 3.3V	-	-
A95	SPI_MOSI_CN	Data out from Module to Carrier SPI	O	CMOS	3.3V Suspend / 3.3V	-	-
B8	LPC_DRQ0# / ESPI_ALERT0#	LPC serial DMA request / Shared pin with ESPI_ALERT	I	CMOS	3.3V / 3.3V	-	-
B9	LPC_DRQ1# / ESPI_ALERT1#	LPC serial DMA request / Shared pin with ESPI_ALERT	I	CMOS	3.3V / 3.3V	-	-
B47	ESPI_EN	This signal is used by the Carrier to indicate the operating mode of the LPC/eSPI bus. If pulled down by the Carrier LPC mode is selected. If pulled up or left floating, eSPI is selected if available. This signal is pulled up on the Module. This signal is a “don’t care” for Modules that do not support eSPI	I	CMOS	NA	-	-

B88	BIOS_DIS1#	Selection straps to determine the BIOS boot device. The Carrier should only float these or pull them low / Shared pin with ESPI_BBS	I	CMOS	NA	PU 10k ohm to 3VSB	-
B97	SPI_CS_CN	Chip select for Carrier Board SPI - maybe sourced from chipset SPI0 or SPI1	O	CMOS	3.3V Suspend / 3.3V	-	-

Table 24 SPI Pin Out

4 Power

PCOM-B702GT is designed for AT power mode, which depends on the power mode design on carrier board. The following AT mode power sequences are provided for the carrier design guideline.

4.1 Power Sequence

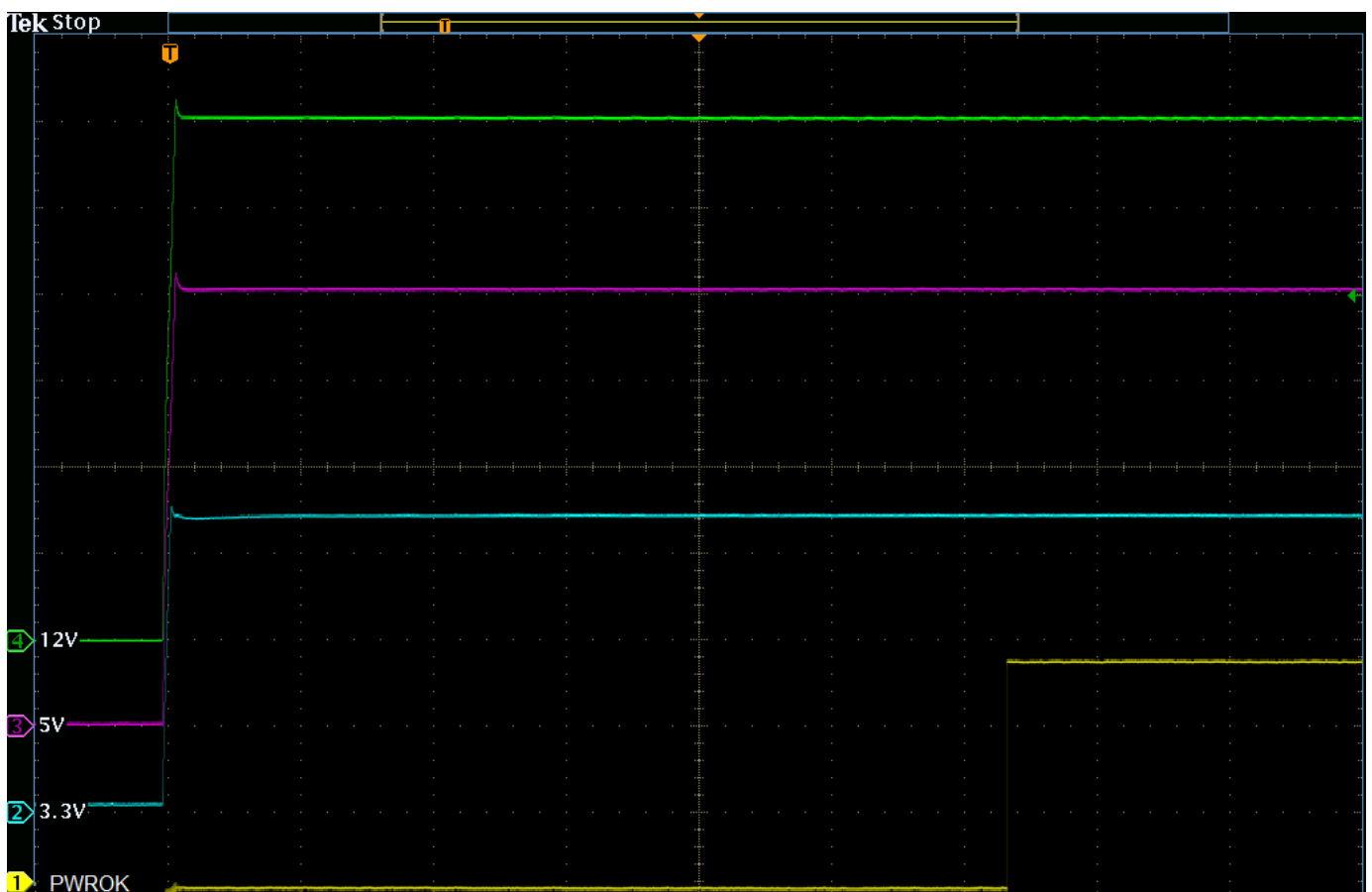


Figure 10 Power Sequence

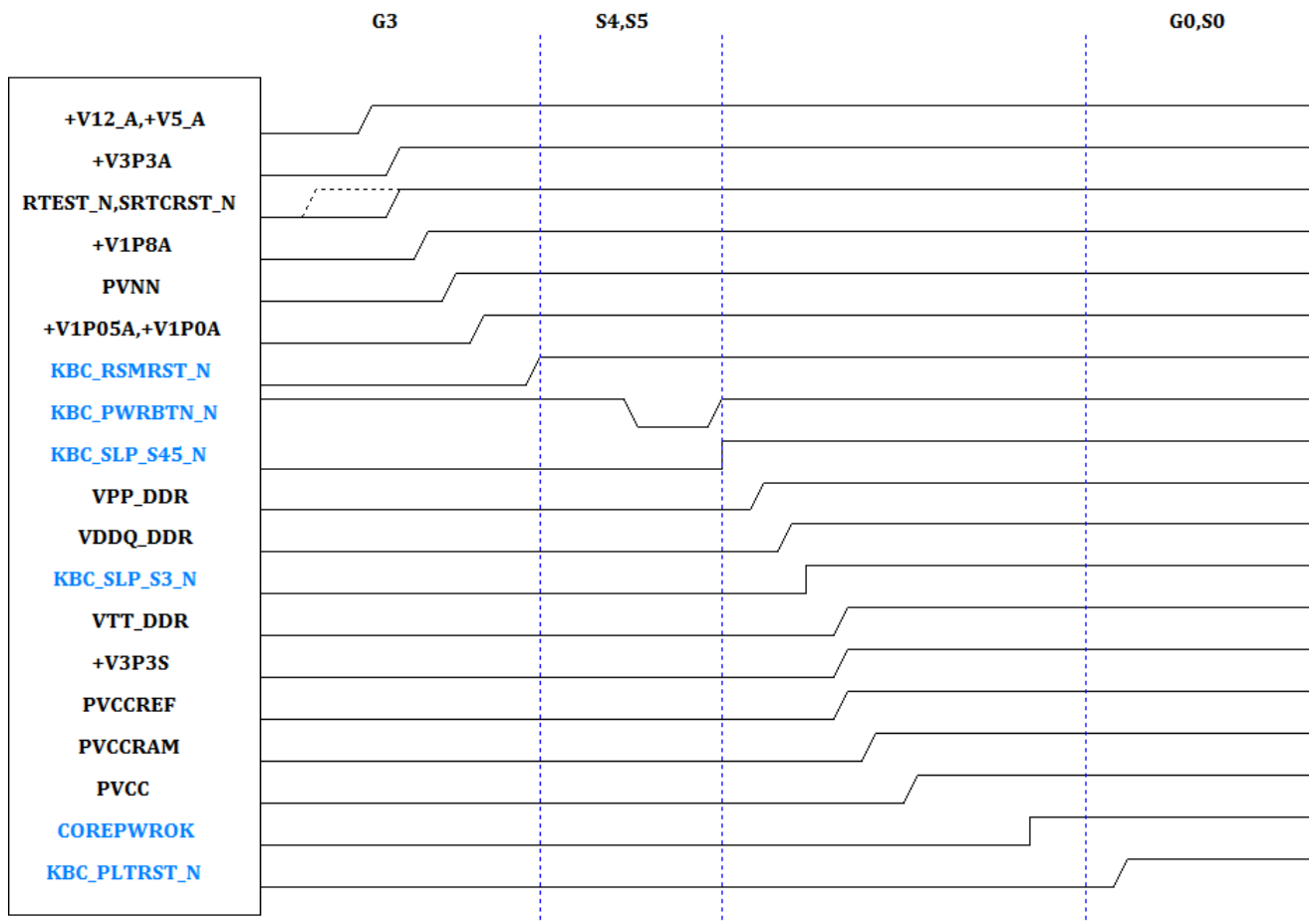


Figure 11 Carrier Power Sequence

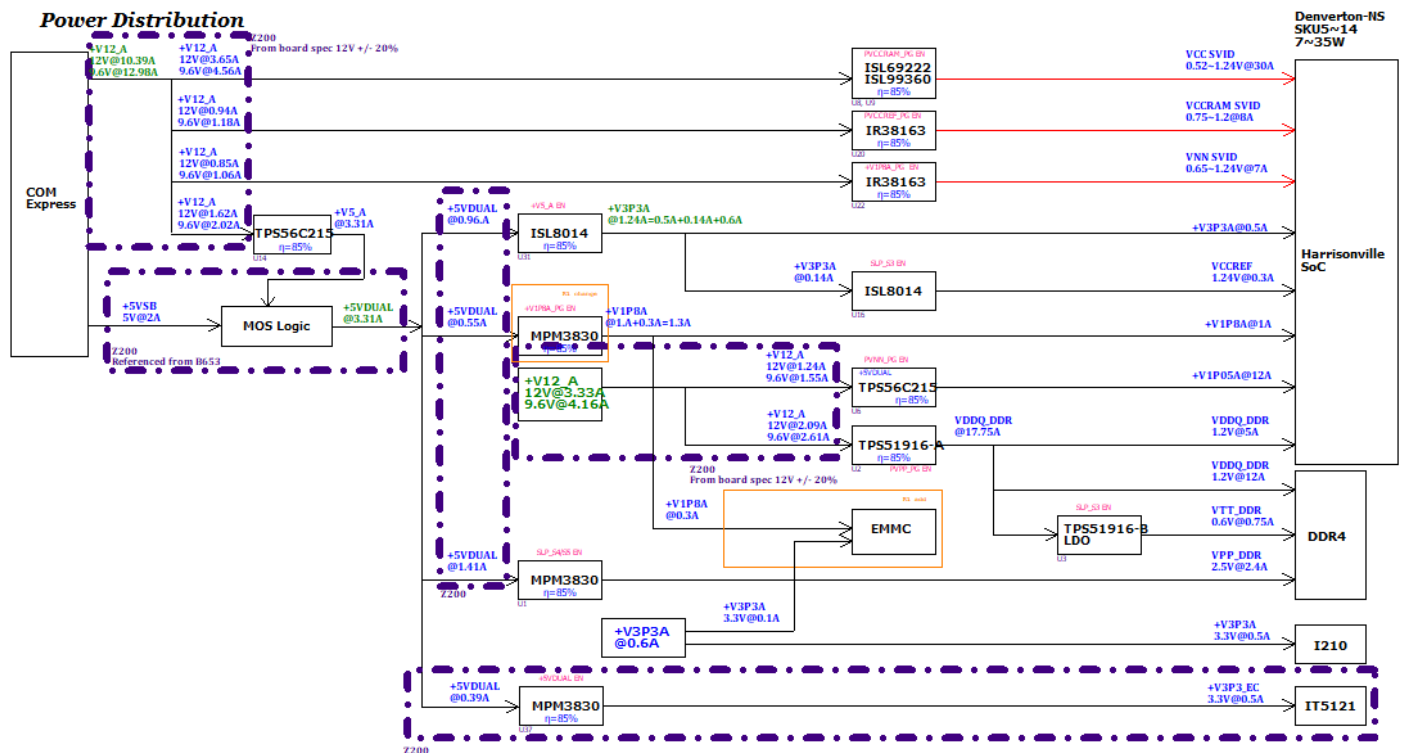


Figure 12 Power Distribution

4.2 VBAT

RTC Battery

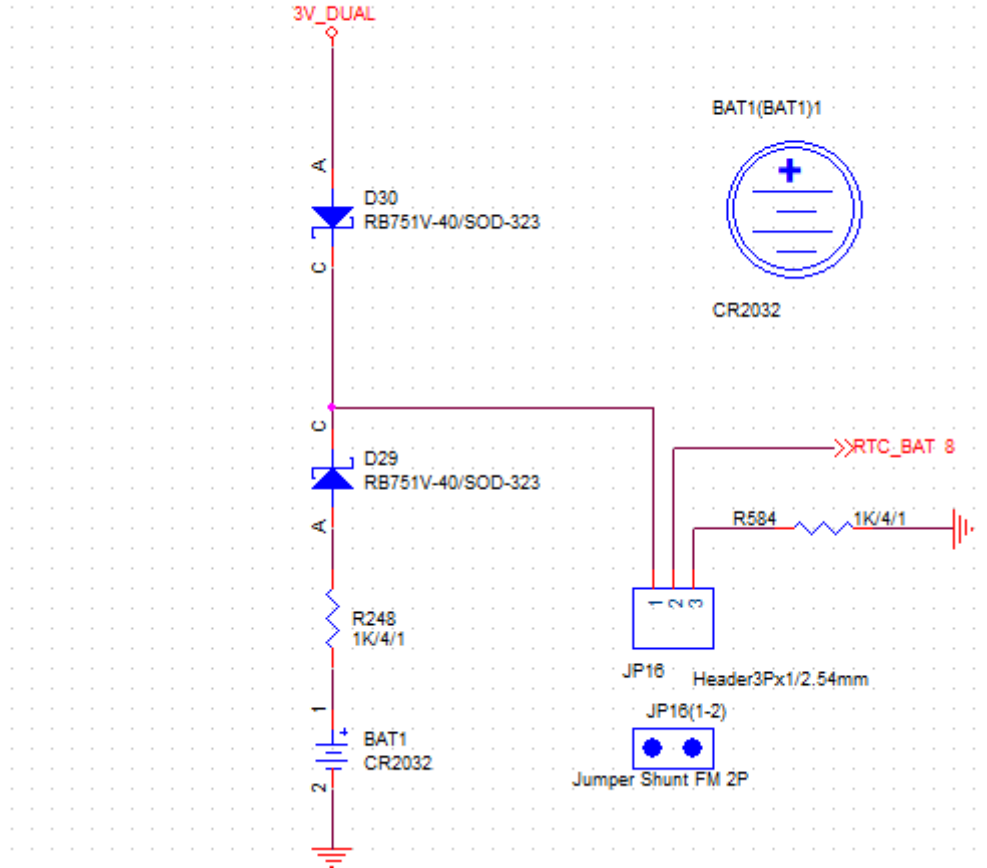


Figure 13 VBAT

5 Mechanical

5.1 PCOM-B702GT Dimension

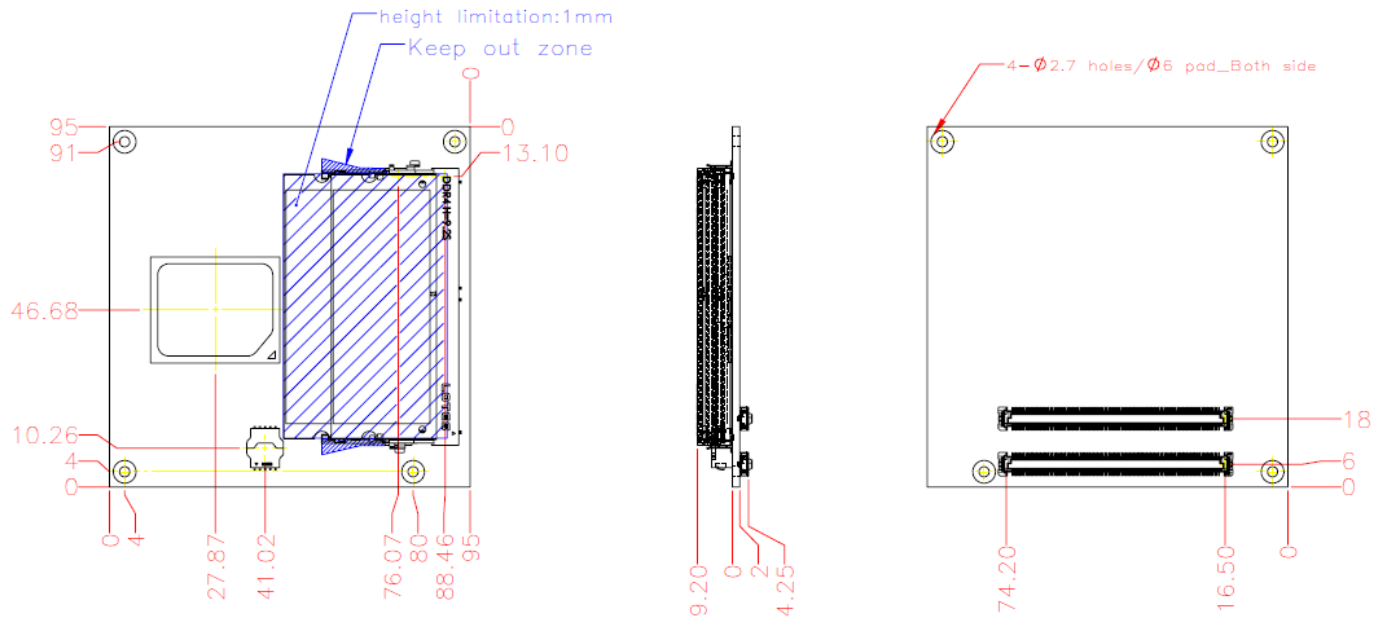


Figure 13 Mechanical – Top, Side and Bottom View

6 Pin out

PCOM-B702GT AB & CD row connectors PIN OUT

Pin	Signal	Description	I/O	Type	Power / Tolerance	PU / PD	Note
A1	GND	GND(FIXED)	-	-	-	-	-
A2	L1_MDIN3	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs	I/O	Analog	3.3V max Suspend	-	-
A3	L1_MDIP3	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs	I/O	Analog	3.3V max Suspend	-	-
A4	L1_100#	Gigabit Ethernet Controller 0 100 Mbit / sec link indicator, active low.	OD	CMOS	3.3V Suspend / 3.3V	-	-
A5	L1_1000#	Gigabit Ethernet Controller 0 1000 Mbit / sec link indicator, active low.	OD	CMOS	3.3V Suspend / 3.3V	-	-
A6	L1_MDIN2	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs	I/O	Analog	3.3V max Suspend	-	-
A7	L1_MDIP2	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs	I/O	Analog	3.3V max Suspend	-	-
A8	L1_LINK#	Gigabit Ethernet Controller 0 link	OD	CMOS	3.3V Suspend	PU 10k ohm to	-

		indicator, active low.			/ 3.3V	3VSB	
A9	L1_MDIN1	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs	I/O	Analog	3.3V max Suspend	-	-
A10	L1_MDIP1	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs	I/O	Analog	3.3V max Suspend	-	-
A11	GND	GND(FIXED)	-	-	-	-	-
A12	L1_MDIN0	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs	I/O	Analog	3.3V max Suspend	-	-
A13	L1_MDIP0	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs	I/O	Analog	3.3V max Suspend	-	-
A14	GBE_CTREF_CN	Reference voltage for Carrier Board Ethernet channel 0 magnetics center tap.	-	-	GND min 3.3V max	Placeholder 0 ohm to V_1P5_L2	-
A15	SLP_S3_CN	Indicates system is in Suspend to RAM state. Active low output. An inverted copy of SUS_S3# on the Carrier Board may be used to enable the non-standby power on a typical ATX supply.	O	CMOS	3.3V Suspend / 3.3V	PD 470 ohm	-
A16	SATA0_PCIE16_TXP	Serial ATA or SAS	O	SATA	AC	-	-

		Channel 0 transmit differential pair.			coupled on Module		
A17	SATA0_PCIE16_TXN	Serial ATA or SAS Channel 0 transmit differential pair.	O	SATA	AC coupled on Module	-	-
A18	SLP_S4_CN	Indicates system is in Suspend to Disk state. Active low output.	O	CMOS	3.3V Suspend / 3.3V	PD 470 ohm -	Through 0 ohm to kbc_slp_S45_N
A19	SATA0_PCIE16_RXP	Serial ATA or SAS Channel 0 receive differential pair.	I	SATA	AC coupled on Module	-	-
A20	SATA0_PCIE16_RXN	Serial ATA or SAS Channel 0 receive differential pair.	I	SATA	AC coupled on Module	-	-
A21	GND	GND(FIXED)	-	-	-	-	-
A22	PCIE_TX15+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A23	PCIE_TX15-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A24	SLP_S5_CN	Indicates system is in Soft Off state.	O	CMOS	3.3V Suspend / 3.3V	PD 470 ohm	Through 0 ohm to kbc_slp_S45_N
A25	PCIE_TX14+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A26	PCIE_TX14-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-

A27	BATLOW_N	Indicates that external battery is low. This port provides a battery-low signal to the Module for orderly transitioning to power saving or power cut-off ACPI modes.	I	CMOS	3.3V Suspend / 3.3V	PU 1K ohm to 3VSB	-
A28	SATA_LED_N	SATA activity indicator, active low.	I/O	CMOS	3.3V / 3.3V	PU 4.7K ohm to 3VSB	-
A29	RSVD	Reserved Pin	-	-	-	-	-
A30	RSVD	Reserved Pin	-	-	-	-	-
A31	GND	GND(FIXED)	-	-	-	-	-
A32	RSVD	Reserved Pin	-	-	-	-	-
A33	RSVD	Reserved Pin	-	-	-	-	-
A34	BIOS_DIS0#	Selection straps to determine the BIOS boot device. The Carrier should only float these or pull them low. Shared pin with ESPI_SAFS	I	CMOS	NA	PU 10K ohm to 3.3V	-
A35	THERMTRIP_N_CN	Active low output indicating that the CPU has entered thermal shutdown	O	CMOS	3.3V / 3.3V	PU 10K ohm to 3VSB	-
A36	PCIE_TX13+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A37	PCIE_TX13-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A38	GND	GND	-	-	-	-	-
A39	PCIE_TX12+	PCI Express Differential	O	PCIE	AC coupled	-	-

		Transmit Pairs			on Module		
A40	PCIE_TX12-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A41	GND	GND(FIXED)	-	-	-	-	-
A42	SOC_USB2_DN2	USB differential pairs, channels 2. All USB ports except USB7, if implemented, shall be host ports.	I/O	USB	3.3V Suspend / 3.3V	-	-
A43	SOC_USB2_DP2	USB differential pairs, channels 2. All USB ports except USB7, if implemented, shall be host ports.	I/O	USB	3.3V Suspend / 3.3V	-	-
A44	USB_OC2_3#	USB over-current sense, USB channels 2 and 3. A pull-up for this line shall be present on the Module. Do not pull this line high on the Carrier Board	I	CMOS	3.3V Suspend / 3.3V	Go through diode then PU 10K ohm	-
A45	SOC_USB2_DN0	USB differential pairs, channels 0. All USB ports except USB7, if implemented, shall be host ports.	I/O	USB	3.3V Suspend / 3.3V	-	-
A46	SOC_USB2_DP0	USB differential pairs, channels 0. All USB ports except USB7, if implemented, shall be host ports.	I/O	USB	3.3V Suspend / 3.3V	-	-
A47	+V3P3_RTC	Real-time clock circuit-power input.	-	PWR	-	-	-

		Nominally +3.0V.					
A48	RSVD	Reserved Pin	-	-	-	-	-
A49	GBE0_SDP	Gigabit Ethernet Controller 0 Software-Definable Pins. Can also be used for IEEE1588 support such as a 1pps signal. See section 4.3.4 for details.	I/O	CMOS	3.3V Suspend / 3.3V		-
A50	SOC_LPC_SERIRQ	LPC serial interrupt / Shared pin with ESPI_CS1#	I/O	CMOS	3.3V / 3.3V	PU 10K ohm to 3.3V	-
A51	GND	GND(FIXED)	-	-	-	-	-
A52	PCIE_TX_DP13	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A53	PCIE_TX_DN13	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A54	GPIO	General purpose input pins. Pulled high internally on the Module.	I	CMOS	3.3V / 3.3V	PU 10k ohm to 3.3V	-
A55	PCIE_TX_DP12	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A56	PCIE_TX_DN12	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A57	GND	GND	-	-	-	-	-
A58	PCIE_TX_DP11	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-

A59	PCIE_TX_DN11	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A60	GND	GND(FIXED)	-	-	-	-	-
A61	PCIE_TX_DP10	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A62	PCIE_TX_DN10	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A63	GPI1	General purpose input pins. Pulled high internally on the Module.	I	CMOS	3.3V / 3.3V	PU 10k ohm to 3.3V	-
A64	PCIE_TX_DP9	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A65	PCIE_TX_DN9	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A66	GND	GND	-	-	-	-	-
A67	GPI2	General purpose input pins. Pulled high internally on the Module.	I	CMOS	3.3V / 3.3V	PU 10k ohm to 3.3V	-
A68	PCIE_TX_DP8	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A69	PCIE_TX_DN8	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A70	GND	GND(FIXED)	-	-	-	-	-
A71	PCIE_TX8+	PCI Express Differential	O	PCIE	AC coupled	-	-

		Transmit Pairs			on Module		
A72	PCIE_TX8-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A73	GND	GND	-	-	-	-	-
A74	PCIE_TX9+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A75	PCIE_TX9-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A76	GND	GND	-	-	-	-	-
A77	PCIE_TX10+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A78	PCIE_TX10-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A79	GND	GND	-	-	-	-	-
A80	GND	GND(FIXED)	-	-	-	-	-
A81	PCIE_TX11+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A82	PCIE_TX11-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A83	GND	GND	-	-	-	-	-
A84	NCSI_TX_EN_CN	NCSI Transmit Enable (PD 10K on Carrier when NC-SI is not used on Carrier)	I	-	3.3V Suspend / 3.3V		-

A85	GPI3	General purpose input pins. Pulled high internally on the Module.	I	CMOS	3.3V / 3.3V	PU 10k ohm to 3.3V	-
A86	RSVD	Reserved Pin	-	-	-	-	-
A87	RSVD	Reserved Pin	-	-	-	-	-
A88	CLK3_PCIE_P_CN	Reference clock output for all PCI Express and PCI Express Graphics lanes.	O	PCIE	PCIE	-	-
A89	CLK3_PCIE_N_CN	Reference clock output for all PCI Express and PCI Express Graphics lanes.	O	PCIE	PCIE	-	-
A90	GND	GND(FIXED)	-	-	-	-	-
A91	SPI_PWR_CN	Power supply for Carrier Board SPI – sourced from Module – nominally 3.3V. The Module shall provide a minimum of 100mA on SPI_POWER. Carriers shall use less than 100mA of SPI_POWER. SPI_POWER shall only be used to power SPI devices on the Carrier	O	-	3.3V Suspend / 3.3V	-	-
A92	SPI_MISO_CN	Data into Module from Carrier SPI	I	CMOS	3.3V Suspend / 3.3V	-	-
A93	GPO0	General purpose output pins. Upon a hardware reset, these outputs should be low.	O	CMOS	3.3V / 3.3V	-	-
A94	SPI_CLK_CN	Clock from Module	O	CMOS	3.3V	-	-

		to Carrier SPI			Suspend / 3.3V		
A95	SPI_MOSI_CN	Data out from Module to Carrier SPI	O	CMOS	3.3V Suspend / 3.3V	-	-
A96	TPM_PP	Trusted Platform Module (TPM) Physical Presence pin. Active high. TPM chip has an internal pull down. This signal is used to indicate Physical Presence to the TPM.	I	CMOS	3.3V / 3.3V	-	-
A97	TYPE10_CN	Dual use pin. Indicates to the Carrier Board that a Type 10 module is installed. Indicates to the Carrier that a Rev 1.0/2.0 module is installed	-	-	-	Place test point	
A98	SER0_TX	General purpose serial port transmitter	O	CMOS	3.3V / 12V	Placeholde r PD 4.7K	-
A99	SER0_RX	General purpose serial port receiver	I	CMOS	3.3V / 12V	Go through diode PU 47K to 3.3V	-
A100	GND	GND(FIXED)	-	-	-	-	-
A101	SER1_TX	General purpose serial port transmitter / CAN_TX	O	CMOS	3.3V / 12V	Placeholde r PD 4.7K	-
A102	SER1_RX	General purpose serial port receiver / CAN_RX	I	CMOS	3.3V / 12V	Go through diode PU 47K to 3.3V	-
A103	LID#_CN	LID button. Low active signal used by the ACPI	I	CMOS	3.3V Suspend / 12V	Go through diode PU 47K to	-

		operating system for a LID switch.				3VSB	
A104	+V12_A	Primary power input: +12V nominal.	-	PWR	+12V	-	-
A105	+V12_A	Primary power input: +12V nominal.	-	PWR	+12V	-	-
A106	+V12_A	Primary power input: +12V nominal.	-	PWR	+12V	-	-
A107	+V12_A	Primary power input: +12V nominal.	-	PWR	+12V	-	-
A108	+V12_A	Primary power input: +12V nominal.	-	PWR	+12V	-	-
A109	+V12_A	Primary power input: +12V nominal.	-	PWR	+12V	-	-
A110	GND	GND(FIXED)	-	-	-	-	-
B1	GND	GND(FIXED)	-	-	-	-	-
B2	L1_LINK#/ACT#	Gigabit Ethernet Controller 1 activity indicator, active low.	O D	CMOS	3.3V Suspend / 3.3V	-	-
B3	SOC_LPC_FRAME_N	LPC frame indicates the start of an LPC cycle / Shared pin with ESPI_CS0#	O	CMOS	3.3V / 3.3V	PU 8.2k ohm to 3.3V	-
B4	SOC_LPC_AD0	LPC multiplexed address, command and data bus / Shared pin with ESPI IO	I/O	CMOS	3.3V / 3.3V	-	-
B5	SOC_LPC_AD1	LPC multiplexed address, command and data bus / Shared pin with	I/O	CMOS	3.3V / 3.3V	-	-

		ESPI IO					
B6	SOC_LPC_AD2	LPC multiplexed address, command and data bus / Shared pin with ESPI IO	I/O	CMOS	3.3V / 3.3V	-	-
B7	SOC_LPC_AD3	LPC multiplexed address, command and data bus / Shared pin with ESPI IO	I/O	CMOS	3.3V / 3.3V	-	-
B8	LPC_DRQ0# / ESPI_ALERT0#	LPC serial DMA request / Shared pin with ESPI_ALERT	I	CMOS	3.3V / 3.3V	-	-
B9	LPC_DRQ1# / ESPI_ALERT1#	LPC serial DMA request / Shared pin with ESPI_ALERT	I	CMOS	3.3V / 3.3V	-	-
B10	LPC_CLK1_CE	LPC clock output - 33MHz nominal / Shared pin with ESPI_Clock	O	CMOS	3.3V / 3.3V	-	-
B11	GND	GND(FIXED)	-	-	-	-	-
B12	PWRBTN#_D	Power button to bring system out of S5 (soft off), active on falling edge.	I	CMOS	3.3V Suspend / 3.3V	PU 10k ohm to 3VSB	-
B13	SMB_CLK_CN	System Management Bus bidirectional clock line.	I/O	CMOS	3.3V Suspend / 3.3V	Placeholder 0 ohm	-
B14	SMB_DATA_CN	System Management Bus bidirectional data line.	I/O	CMOS	3.3V Suspend / 3.3V	Placeholder 0 ohm	-

B15	SMB_ALRT_N_CN	System Management Bus Alert – active low input can be used to generate an SMI# (System Management Interrupt) or to wake the system.	I	CMOS	3.3V Suspend / 3.3V	Go through 0 ohm	-
B16	SATA1_PCIE17_TXP	Serial ATA or SAS Channel 1 transmit differential pair.	O	SATA	AC coupled on Module	-	-
B17	SATA1_PCIE17_TXN	Serial ATA or SAS Channel 1 transmit differential pair.	O	SATA	AC coupled on Module	-	-
B18	SUS_STAT_N_CN	Indicates imminent suspend operation; used to notify LPC devices / Shared pin with ESPI_RESET	O	CMOS	3.3V Suspend / 3.3V	-	-
B19	SATA1_PCIE17_RXP	Serial ATA or SAS Channel 1 receive differential pair.	I	SATA	AC coupled on Module	-	-
B20	SATA1_PCIE17_RXN	Serial ATA or SAS Channel 1 receive differential pair.	I	SATA	AC coupled on Module	-	-
B21	GND	GND(FIXED)	-	-	-	-	-
B22	PCIE_RX15+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B23	PCIE_RX15-	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-

B24	CB_PWROK	Power OK from main power supply. A high value indicates that the power is good. This signal can be used to hold off Module startup to allow carrier based FPGAs or other configurable devices time to be programmed.	I	CMOS	3.3V / 3.3V	-	-
B25	PCIE_RX14+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B26	PCIE_RX14-	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B27	WDTO#	Output indicating that a watchdog time-out event has occurred.	O	CMOS	3.3V / 3.3V	-	-
B28	SMB_LAN_CLK_CN	Reserved Pin	-	-	-	Placeholder 0 ohm -	-
B29	SMB_LAN_DAT_CN	Reserved Pin	-	-	-	Placeholder 0 ohm -	-
B30	SMB_LAN_ALT_CN	Reserved Pin	-	-	-	Placeholder 0 ohm -	-
B31	GND	GND(FIXED)	-	-	-	-	-
B32	SPKR_CN	Output for audio enunciator	O	CMOS	3.3V / 3.3V	NC	-
B33	I2C_CLK_CN	General purpose I2C port clock output	I/O	CMOS	3.3V Suspend / 3.3V	Placeholder PU 10k ohm to 3.3V	-
B34	I2C_DAT_CN	General purpose I2C port data I/O line	I/O	CMOS	3.3V Suspend / 3.3V	Placeholder PU 10k ohm to	-

						3.3V	
B35	PM_THRM_N	Input from off-Module temp sensor indicating an over-temp situation	I	CMOS	3.3V / 3.3V		-
B36	PCIE_RX13+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B37	PCIE_RX13-	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B38	GND	GND	-	-	-	-	-
B39	PCIE_RX12+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B40	PCIE_RX12-	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B41	GND	GND(FIXED)	-	-	-	-	-
B42	SOC_USB2_DN3	USB differential pairs, channels 3. All USB ports except USB7, if implemented, shall be host ports.	I/O	USB	3.3V Suspend / 3.3V	-	-
B43	SOC_USB2_DP3	USB differential pairs, channels 3. All USB ports except USB7, if implemented, shall be host ports.	I/O	USB	3.3V Suspend / 3.3V	-	-
B44	USB_OC0_1#	USB over-current sense, USB channels 0 and 1. A	I	CMOS	3.3V Suspend / 3.3V	Go through diode then PU 10K	-

		pull-up for this line shall be present on the Module. Do not pull this line high on the Carrier Board				ohm	
B45	SOC_USB2_DN1	USB differential pairs, channels 1. All USB ports except USB7, if implemented, shall be host ports.	I/O	USB	3.3V Suspend / 3.3V	-	-
B46	SOC_USB2_DP1	USB differential pairs, channels 1. All USB ports except USB7, if implemented, shall be host ports.	I/O	USB	3.3V Suspend / 3.3V	-	-
B47	ESPI_EN	This signal is used by the Carrier to indicate the operating mode of the LPC/eSPI bus. If pulled down by the Carrier LPC mode is selected. If pulled up or left floating, eSPI is selected if available. This signal is pulled up on the Module. This signal is a “don’t care” for Modules that do not support eSPI	I	CMOS	NA	-	-
B48	USB0_HOST_PRSENT	Module USB client may detect the presence of a USB host on USB0. A high value indicates that a	I	CMOS	3.3V Suspend/ 3.3V	-	-

		host is present.					
B49	RSTBTN#_D	Reset button input. Active low request for module to reset and reboot. May be falling edge sensitive. For situations when SYS_RESET# is not able to reestablish control of the system, PWR_OK or a power cycle may be used	I	CMOS	3.3V Suspend / 3.3V	PU 4.7k ohm to 3VSB	-
B50	CBRST_CN	Reset output from Module to Carrier Board. Active low. Issued by Module chipset and may result from a low SYS_RESET#input, a low PWR_OKinput, a VCC_12Vpower input that falls below the minimum specification, a watchdog timeout, or maybe initiated by the Module software.	O	CMOS	3.3V Suspend / 3.3V		-
B51	GND	GND(FIXED)	-	-	-	-	-
B52	PCIE_RX_DP13	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B53	PCIE_RX_DN13	PCI Express Differential Receive	I	PCIE	AC coupled	-	-

		Pairs			off Module		
B54	GPO1	General purpose output pins. Upon a hardware reset, these outputs should be low.	O	CMOS	3.3V / 3.3V	-	-
B55	PCIE_RX_DP12	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B56	PCIE_RX_DN12	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B57	GPO2	General purpose output pins. Upon a hardware reset, these outputs should be low.	O	CMOS	3.3V / 3.3V	-	-
B58	PCIE_RX_DP11	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B59	PCIE_RX_DN11	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B60	GND	GND(FIXED)	-	-	-	-	-
B61	PCIE_RX_DP10	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B62	PCIE_RX_DN10	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B63	GPO3	General purpose output pins. Upon a hardware reset, these outputs	O	CMOS	3.3V / 3.3V	-	-

		should be low.					
B64	PCIE_RX_DP9	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B65	PCIE_RX_DN9	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B66	WAKE0#_CN	PCI Express wake up signal.	I	CMOS	3.3V Suspend / 3.3V	PU 1k ohm to 3VSB	-
B67	WAKE1#_CN	General purpose wake up signal. Maybe used to implement wake-up on PS2 keyboard or mouse activity	I	CMOS	3.3V Suspend / 3.3V	PU 1k ohm to 3VSB	-
B68	PCIE_RX_DP8	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B69	PCIE_RX_DN8	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B70	GND	GND(FIXED)	-	-	-	-	-
B71	PCIE_RX8+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B72	PCIE_RX8-	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B73	GND	GND	-	-	-	-	-
B74	PCIE_RX9+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off	-	-

					Module		
B75	PCIE_RX9-	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B76	GND	GND	-	-	-	-	-
B77	PCIE_RX10+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B78	PCIE_RX10-	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B79	COME_B79	GND	-	-	-	-	-
B80	GND	GND(FIXED)	-	-	-	-	-
B81	PCIE_RX11+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B82	PCIE_RX11-	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B83	GND	GND	-	-	-	-	-
B84	+5VSB	Standby power input: +5.0V nominal.	-	PWR	+5.0V	-	-
B85	+5VSB	Standby power input: +5.0V nominal.	-	PWR	+5.0V	-	-
B86	+5VSB	Standby power input: +5.0V nominal.	-	PWR	+5.0V	-	-
B87	+5VSB	Standby power input: +5.0V nominal.	-	PWR	+5.0V	-	-
B88	BIOS_DIS1#	Selection straps to determine the BIOS boot device. The Carrier should only	I	CMOS	NA	PU 10k ohm to 3VSB	-

		float these or pull them low / Shared pin with ESPI_BBS					
B89	NCSI_RX_ER_CN	NC-SI Receive error	O	-	3.3V Suspend / 3.3V	NC	-
B90	GND	GND(FIXED)	-	-	-	-	-
B91	NCSI_CLK_IN	NC-SI Clock reference for receive, transmit, and control interface. (PD 10K on Carrier when NC-SI is not used on Carrier)	I	-	3.3V Suspend / 3.3V	-	-
B92	NCSI_RXD_1	NC-SI Receive Data (from NC to BMC).	O	-	3.3V Suspend / 3.3V	Placeholder PU 10K to 3VSB	-
B93	NCSI_RXD_0	NC-SI Receive Data (from NC to BMC).	O	-	3.3V Suspend / 3.3V	Placeholder PU 10K to 3VSB	-
B94	NCSI_CRSDV	NC-SI Carrier Sense/Receive Data Valid to MC, indicating that the transmitted data from NC to BMC is valid.	O	-	3.3V Suspend / 3.3V	Placeholder PD 10K	-
B95	NCSI_TXD_1_CN	NC-SI Transmit Data (from BMC to NC). (PD 10K on Carrier when NC-SI is not used on Carrier)	I	-	3.3V Suspend / 3.3V	PD 10K	-
B96	NCSI_TXD_0_CN	NC-SI Transmit Data (from BMC to NC). (PD 10K on Carrier when NC-SI is not used on Carrier)	I	-	3.3V Suspend / 3.3V	PD 10K	-

B97	SPI_CS_CN	Chip select for Carrier Board SPI - maybe sourced from chipset SPI0 or SPI1	O	CMOS	3.3V Suspend / 3.3V	-	-
B98	NCSI_ARB_IN_CN	NC-SI hardware arbitration input.	I	-	3.3V Suspend / 3.3V	PU 10k ohm to 3VSB	-
B99	NCSI_ARB_OUT	NC-SI hardware arbitration output.	O	-	3.3V Suspend / 3.3V		-
B100	GND	GND(FIXED)	-	-	-	-	-
B101	FAN_PWMOUT_CN	Fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the fan's RPM	O	CMOS	3.3V / 12V	Go through diode then PU 10K ohm	-
B102	FAN_TACHIN_CN	Fan tachometer input for a fan with a two pulse output.	I	CMOS	3.3V / 12V	Go through diode then PU 47K ohm	-
B103	SLEEP#_CN	Sleep button. Low active signal used by the ACPI operating system to bring the system to sleep state or to wake it up again.	I	CMOS	3.3V Suspend / 12V	Go through diode then PU 10K ohm	-
B104	+V12_A	Primary power input: +12V nominal.	-	PWR	+12V	-	-
B105	+V12_A	Primary power input: +12V nominal.	-	PWR	+12V	-	-
B106	+V12_A	Primary power input: +12V nominal.	-	PWR	+12V	-	-
B107	+V12_A	Primary power input: +12V nominal.	-	PWR	+12V	-	-

B108	+V12_A	Primary power input: +12V nominal.	-	PWR	+12V	-	-
B109	+V12_A	Primary power input: +12V nominal.	-	PWR	+12V	-	-
B110	GND	GND(FIXED)	-	-	-	-	-
C1	GND	GND(FIXED)	-	-	-	-	-
C2	GND	GND	-	-	-	-	-
C3	USB3_PCIE18_RXN0	Additional transmit signal differential pairs for the SuperSpeed USB data path.	I	PCIE	AC coupled off Module	-	-
C4	USB3_PCIE18_RXP0	Additional transmit signal differential pairs for the SuperSpeed USB data path.	I	PCIE	AC coupled off Module	-	-
C5	GND	GND	-	-	-	-	-
C6	USB3_PCIE19_RXN1	Additional transmit signal differential pairs for the SuperSpeed USB data path.	I	PCIE	AC coupled off Module	-	-
C7	USB3_PCIE19_RXP1	Additional transmit signal differential pairs for the SuperSpeed USB data path.	I	PCIE	AC coupled off Module	-	-
C8	GND	GND	-	-	-	-	-
C9	USB3_PCIE18_RXN2	Additional transmit signal differential pairs for the SuperSpeed USB data path.	I	PCIE	AC coupled off Module	-	-
C10	USB3_PCIE18_RXP2	Additional transmit signal differential pairs for the SuperSpeed USB data path.	I	PCIE	AC coupled off Module	-	-

C11	GND					-	-
C12	USB3_PCIE19_RXN3	Additional transmit signal differential pairs for the SuperSpeed USB data path.	I	PCIE	AC coupled off Module	-	-
C13	USB3_PCIE19_RXP3	Additional transmit signal differential pairs for the SuperSpeed USB data path.	I	PCIE	AC coupled off Module	-	-
C14	GND	GND	-	-	-	-	-
C15	10PHY_MDC3_CN	MDIO Mode: Management Data I/O interface mode clock signal for serial data transfers between the MAC and an external PHY.	O	-	3.3V Suspend / 3.3V	Placeholder 0 ohm to LAN_MDC	-
		I2C Mode: I2C clock signal, of the 2-wire management interface used for serial data transfers between the MAC and an external PHY.	I/O OD	-	3.3V Suspend / 3.3V	-	-
C16	10PHY_MDC2_CN	MDIO Mode: Management Data I/O interface mode clock signal for serial data transfers between the MAC and an external PHY.	O	-	3.3V Suspend / 3.3V	Placeholder 0 ohm to LAN_MDC	-
		I2C Mode: I2C clock signal, of the 2-wire management interface used for serial data transfers between the MAC and an external	I/O OD	-	3.3V Suspend / 3.3V	-	-

		PHY.					
C17	LAN1_PORT0_SDPO	Software-Definable Pins. Can also be used for IEEE1588 support such as a 1pps signal	I/O	-	3.3V Suspend / 3.3V	-	-
C18	GND	GND	-	-	-	-	-
C19	PCIE_RX6+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C20	PCIE_RX6-	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C21	GND	GND(FIXED)	-	-	-	-	-
C22	PCIE_RX7+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C23	PCIE_RX7-	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C24	10G_INT2_CN	Interrupt pin from copper PHY or optical SFP Module to the 10GbE controller	I	-	3.3V Suspend / 3.3V	NC	-
C25	GND	GND	-	-	-	-	-
C26	LAN1_RX_DP1	10GBASE-KR ports, receive input differential pairs.	I	KR	AC coupled on Module	-	-
C27	LAN1_RX_DN1	10GBASE-KR ports, receive input differential pairs.	I	KR	AC coupled on Module	-	-

C28	GND	GND	-	-	-	-	-
C29	LAN1_RX_DP0	10GBASE-KR ports, receive input differential pairs.	I	KR	AC coupled on Module	-	-
C30	LAN1_RX_DN0	10GBASE-KR ports, receive input differential pairs.	I	KR	AC coupled on Module	-	-
C31	GND	GND(FIXED)	-	-	-	-	-
C32	LAN1_P1_I2C_DAT	I2C data signal of the 2-wire management interface used by the 10GbE controller to access the management registers of an external Optical SFP Module	I/O	OD	3.3V Suspend / 3.3V	PU 1K ohm to 3VSB	-
C33	LAN1_P0_I2C_DAT	I2C data signal of the 2-wire management interface used by the 10GbE controller to access the management registers of an external Optical SFP Module	I/O	OD	3.3V Suspend / 3.3V	PU 1K ohm to 3VSB	-
C34	10GPHY_RST23_CN	Output signal that resets an optical PHY on port 2 and port3 (Not used with copper PHY)	O	-	3.3V Suspend / 3.3V	To pltrst	-
C35	10GPHY_RST01_CN	Output signal that resets an optical PHY on port 0 and port1 (Not used with copper PHY)	O	-	3.3V Suspend / 3.3V	To pltrst	-

C36	10G_LED_SDA_CN	I2C Data of the 2-wire interface that transfers LED signals and PHY straps for I2C or MDIO operation of optical PHYs.	I/O	OD	3.3V Suspend / 3.3V	Placeholder 2.2K ohm to 3VSB	-
C37	10G_LED_SCL_CN	I2C Clock, of the 2-wire interface that transfers LED and strap signals for I2C or MDIO operation of optical PHYs	I/O	OD	3.3V Suspend / 3.3V	Placeholder 2.2K ohm to 3VSB	-
C38	LAN0_P1_I2C_DAT	I2C data signal of the 2-wire management interface used by the 10GbE controller to access the management registers of an external Optical SFP Module	I/O	OD	3.3V Suspend / 3.3V	PU 1K ohm to 3VSB	-
C39	LAN0_P0_I2C_DAT	I2C data signal of the 2-wire management interface used by the 10GbE controller to access the management registers of an external Optical SFP Module	I/O	OD	3.3V Suspend / 3.3V	PU 1K ohm to 3VSB	-
C40	LAN0_PORT0_SDP0	Software-Definable Pins. Can also be used for IEEE1588 support such as a 1pps signal	I/O	-	3.3V Suspend / 3.3V		-
C41	GND	GND(FIXED)	-	-	-	-	-

C42	LAN0_RX_DP1	10GBASE-KR ports, receive input differential pairs.	I	KR	AC coupled on Module	-	-
C43	LAN0_RX_DN1	10GBASE-KR ports, receive input differential pairs.	I	KR	AC coupled on Module	-	-
C44	GND	GND	-	-	-	-	-
C45	10PHY_MDC1_CN	MDIO Mode: Management Data I/O interface mode clock signal for serial data transfers between the MAC and an external PHY.	O	-	3.3V Suspend / 3.3V	- Placeholder 0 ohm to LAN_MDC	-
		I2C Mode: I2C clock signal, of the 2-wire management interface used for serial data transfers between the MAC and an external PHY.	I/O O D	-	3.3V Suspend / 3.3V	-	-
C46	10PHY_MDC0_CN	MDIO Mode: Management Data I/O interface mode clock signal for serial data transfers between the MAC and an external PHY.	O	-	3.3V Suspend / 3.3V	- Placeholder 0 ohm to LAN_MDC	-
		I2C Mode: I2C clock signal, of the 2-wire management interface used for serial data transfers between the MAC	I/O O D	-	3.3V Suspend / 3.3V	-	-

		and an external PHY.					
C47	10G_INT0_CN	Interrupt pin from copper PHY or optical SFP Module to the 10GbE controller	I	-	3.3V Suspend / 3.3V	NC	-
C48	GND	GND	-	-	-	-	-
C49	LAN0_RX_DP0	10GBASE-KR ports, receive input differential pairs.	I	KR	AC coupled on Module	-	-
C50	LAN0_RX_DN0	10GBASE-KR ports, receive input differential pairs.	I	KR	AC coupled on Module	-	-
C51	GND	GND(FIXED)	-	-	-	-	-
C52	PCIE_RX_DP0	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C53	PCIE_RX_DN0	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C54	TYPE0	The TYPE pins indicate to the Carrier Board the Pin-out Type that is implemented on the Module.	-	-	-	PD 0 ohm	-
C55	PCIE_RX_DP1	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C56	PCIE_RX_DN1	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C57	TYPE1	The TYPE pins indicate to the Carrier Board the	-	-	-	Placeholder PD 0 ohm	-

		Pin-out Type that is implemented on the Module.					
C58	PCIE_RX_DP2	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C59	PCIE_RX_DN2	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C60	GND	GND(FIXED)	-	-	-	-	-
C61	PCIE_RX_DP3	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C62	PCIE_RX_DN3	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C63	RSVD	Reserved Pin	-	-	-	-	-
C64	RSVD	Reserved Pin	-	-	-	-	-
C65	PCIE_RX_DP4	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C66	PCIE_RX_DN4	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C67	RAPID_SUTDN	Trigger for Rapid Shutdown. Must be driven to 5V though a <=50 ohm source impedance for a	I	CMOS	5.0V Suspend/ 5.0V	PD 150 ohm	-
C68	PCIE_RX_DP5	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C69	PCIE_RX_DN5	PCI Express Differential Receive	I	PCIE	AC coupled	-	-

		Pairs			off Module		
C70	GND	GND(FIXED)	-	-	-	-	-
C71	PCIE_RX_DP6	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C72	PCIE_RX_DN6	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C73	GND	GND	-	-	-	-	-
C74	PCIE_RX_DP7	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C75	PCIE_RX_DN7	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C76	GND	GND	-	-	-	-	-
C77	RSVD	Reserved Pin	-	-	-	-	-
C78	PCIE_RX24+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C79	PCIE_RX24-	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C80	GND	GND(FIXED)	-	-	-	-	-
C81	PCIE_RX25+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C82	PCIE_RX25-	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C83	RSVD	Reserved Pin	-	-	-	-	-
C84	GND	GND	-	-	-	-	-

C85	PCIE_RX26+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C86	PCIE_RX26-	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C87	GND	GND	-	-	-	-	-
C88	PCIE_RX27+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C89	PCIE_RX27-	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C90	GND	GND(FIXED)	-	-	-	-	-
C91	PCIE_RX28+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C92	PCIE_RX28-	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C93	GND	GND	-	-	-	-	-
C94	PCIE_RX29+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C95	PCIE_RX29-	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C96	GND	GND	-	-	-	-	-
C97	RSVD	Reserved Pin	-	-	-	-	-
C98	PCIE_RX30+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-

C99	PCIE_RX30-	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C100	GND	GND(FIXED)	-	-	-	-	-
C101	PCIE_RX31+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C102	PCIE_RX31-	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C103	GND	GND	-	-	-	-	-
C104	+V12_A	Primary power input: +12V nominal.	-	PWR	+12V	-	-
C105	+V12_A	Primary power input: +12V nominal.	-	PWR	+12V	-	-
C106	+V12_A	Primary power input: +12V nominal.	-	PWR	+12V	-	-
C107	+V12_A	Primary power input: +12V nominal.	-	PWR	+12V	-	-
C108	+V12_A	Primary power input: +12V nominal.	-	PWR	+12V	-	-
C109	+V12_A	Primary power input: +12V nominal.	-	PWR	+12V	-	-
C110	GND	GND(FIXED)	-	-	-	-	-
D1	GND	GND(FIXED)	-	-	-	-	-
D2	GND	GND	-	-	-	-	-
D3	USB3_PCIE18_TXN0	Additional transmit signal differential pairs for the SuperSpeed USB data path.	O	PCIE	AC coupled on Module	-	-

D4	USB3_PCIE18_TXP0	Additional transmit signal differential pairs for the SuperSpeed USB data path.	O	PCIE	AC coupled on Module	-	-
D5	GND	GND	-	-	-	-	-
D6	USB3_PCIE19_TXN1	Additional transmit signal differential pairs for the SuperSpeed USB data path.	O	PCIE	AC coupled on Module	-	-
D7	USB3_PCIE19_TXP1	Additional transmit signal differential pairs for the SuperSpeed USB data path.	O	PCIE	AC coupled on Module	-	-
D8	GND	GND	-	-	-	-	-
D9	USB3_PCIE18_TXN2	Additional transmit signal differential pairs for the SuperSpeed USB data path.	O	PCIE	AC coupled on Module	-	-
D10	USB3_PCIE18_TXP2	Additional transmit signal differential pairs for the SuperSpeed USB data path.	O	PCIE	AC coupled on Module	-	-
D11	GND	GND(FIXED)	-	-	-	-	-
D12	USB3_PCIE19_TXN3	Additional transmit signal differential pairs for the SuperSpeed USB data path.	O	PCIE	AC coupled on Module	-	-
D13	USB3_PCIE19_TXP3	Additional transmit signal differential pairs for the SuperSpeed USB data path.	O	PCIE	AC coupled on Module	-	-
D14	GND	GND	-	-	-	-	-

D15	10PHY_MDA3_CN	MDIO Mode: Management Data I/O interface mode data signal for serial data transfers between the MAC and an external PHY.	O	-	3.3V Suspend / 3.3V	- Placeholder 0 ohm to LAN_MDIO	-
		I2C Mode: I2C data signal, of the 2-wire management interface used for serial data transfers between the MAC and an external PHY.	I/O O D	-	3.3V Suspend / 3.3V	-	-
D16	10PHY_MDA2_CN	MDIO Mode: Management Data I/O interface mode data signal for serial data transfers between the MAC and an external PHY.	O	-	3.3V Suspend / 3.3V	- Placeholder 0 ohm to LAN_MDIO	-
		I2C Mode: I2C data signal, of the 2-wire management interface used for serial data transfers between the MAC and an external PHY.	I/O O D	-	3.3V Suspend / 3.3V	-	-
D17	LAN1_PORT1_SDP 0	Software-Definable Pins. Can also be used for IEEE1588 support such as a 1pps signal	I/O	-	3.3V Suspend / 3.3V		-
D18	GND	GND	-	-	-	-	-
D19	PCIE_TX6+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on	-	-

					Module		
D20	PCIE_TX6-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D21	GND(FIXED)	GND(FIXED)	-	-	-	-	-
D22	PCIE_TX7+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D23	PCIE_TX7-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D24	10G_INT3_CN	Interrupt pin from copper PHY or optical SFP Module to the 10GbE controller	I	-	3.3V Suspend / 3.3V	NC	-
D25	GND	GND	-	-	-	-	-
D26	LAN1_TX_DP1	10GBASE-KR ports, transmit output differential pairs.	O	KR	AC coupled on Carrier	-	-
D27	LAN1_TX_DN1	10GBASE-KR ports, transmit output differential pairs.	O	KR	AC coupled on Carrier	-	-
D28	GND	GND	-	-	-	-	-
D29	LAN1_TX_DP0	10GBASE-KR ports, transmit output differential pairs.	O	KR	AC coupled on Carrier	-	-
D30	LAN1_TX_DN0	10GBASE-KR ports, transmit output differential pairs.	O	KR	AC coupled on Carrier	-	-
D31	GND	GND(FIXED)	-	-	-	-	-

D32	LAN1_P1_I2C_CLK	I2C clock signal of the 2-wire management interface used by the 10GbE controller to access the management registers of an external Optical SFP Module	I/O	OD	3.3V Suspend / 3.3V	PU 1K ohm to 3VSB	-
D33	LAN1_P0_I2C_CLK	I2C clock signal of the 2-wire management interface used by the 10GbE controller to access the management registers of an external Optical SFP Module	I/O	OD	3.3V Suspend / 3.3V	PU 1K ohm to 3VSB	-
D34	10GPHY_SEL23_CN	Phy mode select pin: If high Phy2 and Phy3 are configured by MDIO. If low Phy2 and Phy3 are configured by I2C. For MDIO mode, this pin should be left not connected on the Carrier. For I2C mode pull down with 1K on Carrier	I	-	3.3V Suspend / 3.3V	-	-
D35	10GPHY_SEL01_CN	Phy mode select pin: If high Phy0 and Phy1 are configured by MDIO. If low Phy2 and Phy3 are configured by I2C. For MDIO mode,	I	-	3.3V Suspend / 3.3V	-	-

		this pin should be left not connected on the Carrier. For I2C mode pull down with 1K on Carrier					
D36	RSVD	RSVD	-	-	-	-	-
D37	RSVD	RSVD	-	-	-	-	-
D38	LAN0_P1_I2C_CLK	I2C clock signal of the 2-wire management interface used by the 10GbE controller to access the management registers of an external Optical SFP Module	I/O	OD	3.3V Suspend / 3.3V	PU 1K ohm to 3VSB	-
D39	LAN0_P0_I2C_CLK	I2C clock signal of the 2-wire management interface used by the 10GbE controller to access the management registers of an external Optical SFP Module	I/O	OD	3.3V Suspend / 3.3V	PU 1K ohm to 3VSB	-
D40	LAN0_PORT1_SDP0	Software-Definable Pins. Can also be used for IEEE1588 support such as a 1pps signal	I/O	-	3.3V Suspend / 3.3V		-
D41	GND	GND(FIXED)	-	-	-	-	-
D42	LAN0_TX_DP1	10GBASE-KR ports, transmit output differential pairs.	O	KR	AC coupled on Carrier	-	-
D43	LAN0_TX_DN1	10GBASE-KR ports, transmit output differential pairs.	O	KR	AC coupled on Carrier	-	-

D44	GND	GND	-	-	-	-	-
D45	10PHY_MDA1_CN	MDIO Mode: Management Data I/O interface mode data signal for serial data transfers between the MAC and an external PHY.	O	-	3.3V Suspend / 3.3V	Placeholder 0 ohm to LAN_MDIO	-
		I2C Mode: I2C data signal, of the 2-wire management interface used for serial data transfers between the MAC and an external PHY.	I/O O D	-	3.3V Suspend / 3.3V	-	-
D46	10PHY_MDA0_CN	MDIO Mode: Management Data I/O interface mode data signal for serial data transfers between the MAC and an external PHY.	O	-	3.3V Suspend / 3.3V	Placeholder 0 ohm to LAN_MDIO	-
		I2C Mode: I2C data signal, of the 2-wire management interface used for serial data transfers between the MAC and an external PHY.	I/O O D	-	3.3V Suspend / 3.3V	-	-
D47	10G_INT1_CN	Interrupt pin from copper PHY or optical SFP Module to the 10GbE controller	I	-	3.3V Suspend / 3.3V	NC	-
D48	GND	GND	-	-	-	-	-
D49	LAN0_TX_DP0	10GBASE-KR ports, transmit output differential	O	KR	AC coupled on	-	-

		pairs.			Carrier		
D50	LAN0_TX_DN0	10GBASE-KR ports, transmit output differential pairs.	O	KR	AC coupled on Carrier	-	-
D51	GND	GND(FIXED)	-	-	-	-	-
D52	PCIE_TX_DP0	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D53	PCIE_TX_DN0	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D54	CFG9	Reserved Pin	-	-	-	-	-
D55	PCIE_TX_DP1	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D56	PCIE_TX_DN1	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D57	TYPE2	The TYPE pins indicate to the Carrier Board the Pin-out Type that is implemented on the Module.	-	-	-	PD 0 ohm	-
D58	PCIE_TX_DP2	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D59	PCIE_TX_DN2	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D60	GND	GND(FIXED)	-	-	-	-	-
D61	PCIE_TX_DP3	PCI Express Differential	O	PCIE	AC coupled	-	-

		Transmit Pairs			on Module		
D62	PCIE_TX_DN3	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D63	RSVD	Reserved Pin	-	-	-	-	-
D64	RSVD	Reserved Pin	-	-	-	-	-
D65	PCIE_TX_DP4	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D66	PCIE_TX_DN4	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D67	GND	GND	-	-	-	-	-
D68	PCIE_TX_DP5	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D69	PCIE_TX_DN5	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D70	GND	GND(FIXED)	-	-	-	-	-
D71	PCIE_TX_DP6	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D72	PCIE_TX_DN6	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D73	GND	GND	-	-	-	-	-
D74	PCIE_TX_DP7	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D75	PCIE_TX_DN7	PCI Express Differential	O	PCIE	AC coupled	-	-

		Transmit Pairs			on Module		
D76	GND	GND	-	-	-	-	-
D77	RSVD	Reserved Pin	-	-	-	-	-
D78	PCIE_TX24+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D79	PCIE_TX24-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D80	GND	GND(FIXED)	-	-	-	-	-
D81	PCIE_TX25+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D82	PCIE_TX25-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D83	RSVD	Reserved Pin	-	-	-	-	-
D84	GND	GND	-	-	-	-	-
D85	PCIE_TX26+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D86	PCIE_TX26-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D87	GND	GND	-	-	-	-	-
D88	PCIE_TX27+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D89	PCIE_TX27-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D90	GND	GND(FIXED)	-	-	-	-	-

D91	PCIE_TX28+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D92	PCIE_TX28-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D93	GND	GND	-	-	-	-	-
D94	PCIE_TX29+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D95	PCIE_TX29-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D96	GND	GND	-	-	-	-	-
D97	RSVD	Reserved Pin	-	-	-	-	-
D98	PCIE_TX30+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D99	PCIE_TX30-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D100	GND	GND(FIXED)	-	-	-	-	-
D101	PCIE_TX31+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D102	PCIE_TX31-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D103	GND	GND	-	-	-	-	-
D104	+V12_A	Primary power input: +12V nominal.	-	PWR	+12V	-	-
D105	+V12_A	Primary power	-	PWR	+12V	-	-

		input: +12V nominal.					
D106	+V12_A	Primary power input: +12V nominal.	-	PWR	+12V	-	-
D107	+V12_A	Primary power input: +12V nominal.	-	PWR	+12V	-	-
D108	+V12_A	Primary power input: +12V nominal.	-	PWR	+12V	-	-
D109	+V12_A	Primary power input: +12V nominal.	-	PWR	+12V	-	-
D110	GND	GND(FIXED)	-	-	-	-	-

Table 25 PCOM-B702GT AB & CD Row Connectors Pin Out

7 Industry Specifications

Low Pin Count Interface Specification, Revision 1.0 (LPC)

<http://www.intel.com/design/chipsets/industry/lpc.htm>

Universal Serial Bus (USB) Specification, Revision 2.0 <http://www.usb.org/home>

PCI Specification, Revision 2.3 <https://www.pcisig.com/specifications>

Serial ATA Specification, Revision 3.0 <http://www.serialata.org/>

PCI Express Base Specification, Revision 2.0 <https://www.pcisig.com/specifications>

PICMG® COM Express Module™ Base Specification <http://www.picmg.org/>

PICMG®COM Express Carrier Board Design Guide <http://www.picmg.org/>