COM Express Carrier Design Guide

Carrier Design Guideline for

PCOM-B706GT

Rev. 0.2

Revision history

Rev.	Date	Note
R0.1	2023/8	1st Release
R0.2	2025/12	For R1 PCB

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1 Introduction

The Carrier Design Guide provides the guideline of designing your own carrier board based on Portwell's COM Express Modular product PCOM-B706GT. PCOM-B706GT is Type 7, 125x95mm Modular board, more information is included in PCOM-B706GT User's Guide and can be downloaded from Portwell download center (Or contact your Portwell sales representative for acquiring PCOM-B706GT User's Guide). This carrier design guide is dedicated for the designers designing a COM Express Type 7 carrier board which will have an excellent compatibility with Portwell's PCOM-B706GT modular product.

The layout guideline provided, each interface has three sections, which are detail PCOM-B706GT pin out, pin name, power rail, PU/PD, AC couple capacitor etc. information are included. Second part contains PCB layout guide, impedance, maximum trace, trace width, and trace spacing etc. Third section provides the available trace length of which designers are able to optimize the high-speed signals such as PCIE, SATA, USB etc.

2 PCOM-B706GT

2.1 PCOM-B706GT Block Diagram

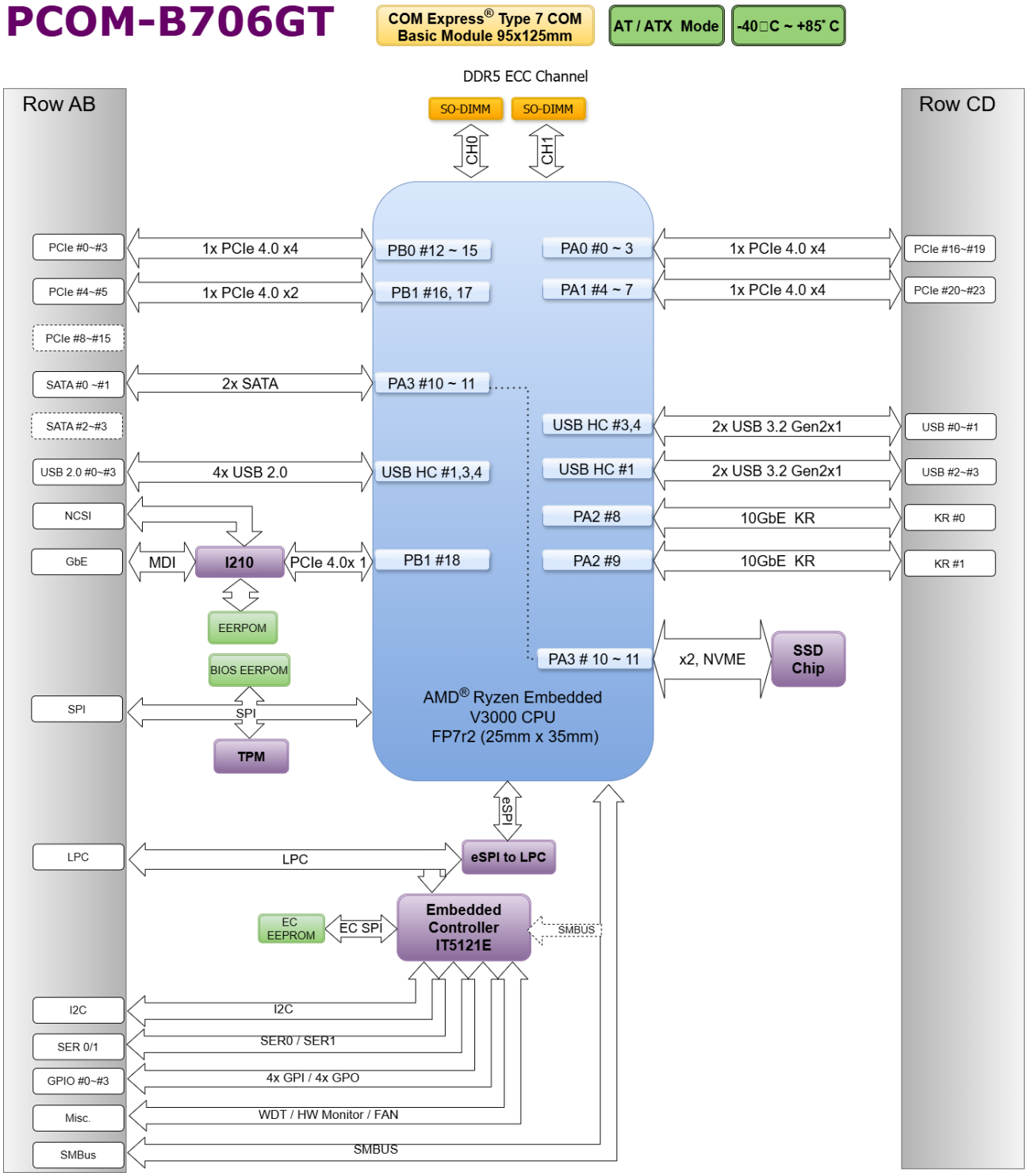


Figure 1 PCOM-B706GT Block Diagram

2.2 PCOM-B706GT Pin-out

PCOM-B706GT Type7 Pin-Out							
Pin	Row A	Pin	Row B	Pin	Row C	Pin	Row D
A1	GND(FIXED)	B1	GND(FIXED)	C1	GND(FIXED)	D1	GND(FIXED)
A2	GBE0_MDI3-	B2	GBE0_ACT#	C2	GND	D2	GND
A3	GBE0_MDI3+	B3	LPC_FRAME#	C3	USB_SSRX0-	D3	USB_SSTX0-
A4	GBE0_LINK100#	B4	LPC_AD0	C4	USB_SSRX0+	D4	USB_SSTX0+
A5	GBE0_LINK1000#	B5	LPC_AD1	C5	GND	D5	GND
A6	GBE0_MDI2-	B6	LPC_AD2	C6	USB_SSRX1-	D6	USB_SSTX1-
A7	GBE0_MDI2+	B7	LPC_AD3	C7	USB_SSRX1+	D7	USB_SSTX1+
A8	GBE0_LINK#	B8	NC	C8	GND	D8	GND
A9	GBE0_MDI1-	B9	NC	C9	USB_SSRX2-	D9	USB_SSTX2-
A10	GBE0_MDI1+	B10	LPC_CLK	C10	USB_SSRX2+	D10	USB_SSTX2+
A11	GND(FIXED)	B11	GND(FIXED)	C11	GND(FIXED)	D11	GND(FIXED)
A12	GBE0_MDI0-	B12	PWRBTN#	C12	USB_SSRX3-	D12	USB_SSTX3-
A13	GBE0_MDI0+	B13	SMB_CK	C13	USB_SSRX3+	D13	USB_SSTX3+
A14	NC	B14	SMB_DAT	C14	GND	D14	GND
A15	SUS_S3#	B15	SMB_ALERT#	C15	NC	D15	NC
A16	SATA0_TX+	B16	SATA1_TX+	C16	NC	D16	NC
A17	SATA0_TX-	B17	SATA1_TX-	C17	10G_SDP2 (1588_PPS_OUT_0_3V3)	D17	10G_SDP3 (1588_PPS_OUT_1_3V3)
A18	SUS_S4#	B18	SUS_STAT#	C18	GND	D18	GND
A19	SATA0_RX+	B19	SATA1_RX+	C19	NC	D19	NC
A20	SATA0_RX-	B20	SATA1_RX-	C20	NC	D20	NC
A21	GND(FIXED)	B21	GND(FIXED)	C21	GND(FIXED)	D21	GND(FIXED)
A22	NC	B22	NC	C22	NC	D22	NC
A23	NC	B23	NC	C23	NC	D23	NC
A24	SUS_S5#	B24	PWR_OK	C24	NC	D24	NC
A25	NC	B25	NC	C25	GND	D25	GND
A26	NC	B26	NC	C26	NC	D26	NC
A27	BATLOW#	B27	WDT	C27	NC	D27	NC
A28	(S)ATA_ACT#	B28	NC	C28	GND	D28	GND
A29	NC	B29	NC	C29	NC	D29	NC
A30	NC	B30	NC	C30	NC	D30	NC

PCOM-B706GT Type7 Pin-Out							
Pin	Row A	Pin	Row B	Pin	Row C	Pin	Row D
A1	GND(FIXED)	B1	GND(FIXED)	C1	GND(FIXED)	D1	GND(FIXED)
A2	GBE0_MDI3-	B2	GBE0_ACT#	C2	GND	D2	GND
A3	GBE0_MDI3+	B3	LPC_FRAME#	C3	USB_SSRX0-	D3	USB_SSTX0-
A4	GBE0_LINK100#	B4	LPC_AD0	C4	USB_SSRX0+	D4	USB_SSTX0+
A5	GBE0_LINK1000#	B5	LPC_AD1	C5	GND	D5	GND
A6	GBE0_MDI2-	B6	LPC_AD2	C6	USB_SSRX1-	D6	USB_SSTX1-
A7	GBE0_MDI2+	B7	LPC_AD3	C7	USB_SSRX1+	D7	USB_SSTX1+
A8	GBE0_LINK#	B8	NC	C8	GND	D8	GND
A9	GBE0_MDI1-	B9	NC	C9	USB_SSRX2-	D9	USB_SSTX2-
A10	GBE0_MDI1+	B10	LPC_CLK	C10	USB_SSRX2+	D10	USB_SSTX2+
A11	GND(FIXED)	B11	GND(FIXED)	C11	GND(FIXED)	D11	GND(FIXED)
A12	GBE0_MDI0-	B12	PWRBTN#	C12	USB_SSRX3-	D12	USB_SSTX3-
A13	GBE0_MDI0+	B13	SMB_CK	C13	USB_SSRX3+	D13	USB_SSTX3+
A14	NC	B14	SMB_DAT	C14	GND	D14	GND
A15	SUS_S3#	B15	SMB_ALERT#	C15	NC	D15	NC
A16	SATA0_TX+	B16	SATA1_TX+	C16	NC	D16	NC
A17	SATA0_TX-	B17	SATA1_TX-	C17	10G_SDP2 (1588_PPS_OUT_0_3V 3)	D17	10G_SDP3 (1588_PPS_OUT_1_3V 3)
A18	SUS_S4#	B18	SUS_STAT#	C18	GND	D18	GND
A19	SATA0_RX+	B19	SATA1_RX+	C19	PCIE_RX6+	D19	PCIE_TX6+
A20	SATA0_RX-	B20	SATA1_RX-	C20	PCIE_RX6-	D20	PCIE_TX6-
A21	GND(FIXED)	B21	GND(FIXED)	C21	GND(FIXED)	D21	GND(FIXED)
A22	NC	B22	NC	C22	PCIE_RX7+	D22	PCIE_TX7+
A23	NC	B23	NC	C23	PCIE_RX7-	D23	PCIE_TX7-
A24	SUS_S5#	B24	PWR_OK	C24	NC	D24	NC
A25	NC	B25	NC	C25	GND	D25	GND
A26	NC	B26	NC	C26	NC	D26	NC
A27	BATLOW#	B27	WDT	C27	NC	D27	NC
A28	(S)ATA_ACT#	B28	NC	C28	GND	D28	GND

A61	PCIE_TX2+	B61	PCIE_RX2+	C61	PCIE_RX19+	D61	PCIE_TX19+
A62	PCIE_TX2-	B62	PCIE_RX2-	C62	PCIE_RX19-	D62	PCIE_TX19-
A63	GPI1	B63	GPO3	C63	NC	D63	NC
A64	PCIE_TX1+	B64	PCIE_RX1+	C64	NC	D64	NC
A65	PCIE_TX1-	B65	PCIE_RX1-	C65	PCIE_RX20+	D65	PCIE_TX20+
A66	GND	B66	WAKE0#	C66	PCIE_RX20-	D66	PCIE_TX20-
A67	GPI2	B67	WAKE1#	C67	RAPID_SHUTDOWN	D67	GND
A68	PCIE_TX0+	B68	PCIE_RX0+	C68	PCIE_RX21+	D68	PCIE_TX21+
A69	PCIE_TX0-	B69	PCIE_RX0-	C69	PCIE_RX21-	D69	PCIE_TX21-
A70	GND(FIXED)	B70	GND(FIXED)	C70	GND(FIXED)	D70	GND(FIXED)
A71	NC	B71	NC	C71	PCIE_RX22+	D71	PCIE_TX22+
A72	NC	B72	NC	C72	PCIE_RX22-	D72	PCIE_TX22-
A73	GND	B73	GND	C73	GND	D73	GND
A74	NC	B74	NC	C74	PCIE_RX23+	D74	PCIE_TX23+
A75	NC	B75	NC	C75	PCIE_RX23-	D75	PCIE_TX23-
A76	GND	B76	GND	C76	GND	D76	GND
A77	NC	B77	NC	C77	NC	D77	NC
A78	NC	B78	NC	C78	NC	D78	NC
A79	GND	B79	GND	C79	NC	D79	NC
A80	GND(FIXED)	B80	GND(FIXED)	C80	GND(FIXED)	D80	GND(FIXED)
A81	NC	B81	NC	C81	NC	D81	NC
A82	NC	B82	NC	C82	NC	D82	NC
A83	GND	B83	GND	C83	NC	D83	NC
A84	NCSI_TX_EN	B84	VCC_5V_SBY	C84	GND	D84	GND
A85	GPI3	B85	VCC_5V_SBY	C85	NC	D85	NC
A86	NC	B86	VCC_5V_SBY	C86	NC	D86	NC
A87	NC	B87	VCC_5V_SBY	C87	GND	D87	GND
A88	PCIE_CK_REF+	B88	BIOS_DIS1#	C88	NC	D88	NC
A89	PCIE_CK_REF-	B89	NC	C89	NC	D89	NC
A90	GND(FIXED)	B90	GND(FIXED)	C90	GND(FIXED)	D90	GND(FIXED)

A91	SPI_POWER	B91	NCSI_CLK_IN	C91	NC	D91	NC
A92	SPI_MISO	B92	NCSI_RXD1	C92	NC	D92	NC
A93	GPO0	B93	NCSI_RXD0	C93	GND	D93	GND
A94	SPI_CLK	B94	NCSI_CRS_DV	C94	NC	D94	NC
A95	SPI_MOSI	B95	NCSI_TXD1	C95	NC	D95	NC
A96	NC	B96	NCSI_TXD0	C96	GND	D96	GND
A97	TYPE10#	B97	SPI_CS#	C97	NC	D97	NC
A98	SER0_TX	B98	NCSI_ARB_IN	C98	NC	D98	NC
A99	SER0_RX	B99	NCSI_ARB_OUT	C99	NC	D99	NC
A100	GND(FIXED)	B100	GND(FIXED)	C100	GND(FIXED)	D100	GND(FIXED)
A101	SER1_TX	B101	FAN_PWMOUT	C101	NC	D101	NC
A102	SER1_RX	B102	FAN_TACHIN	C102	NC	D102	NC
A103	LID#	B103	SLEEP#	C103	GND	D103	GND
A104	VCC_12V	B104	VCC_12V	C104	VCC_12V	D104	VCC_12V
A105	VCC_12V	B105	VCC_12V	C105	VCC_12V	D105	VCC_12V
A106	VCC_12V	B106	VCC_12V	C106	VCC_12V	D106	VCC_12V
A107	VCC_12V	B107	VCC_12V	C107	VCC_12V	D107	VCC_12V
A108	VCC_12V	B108	VCC_12V	C108	VCC_12V	D108	VCC_12V
A109	VCC_12V	B109	VCC_12V	C109	VCC_12V	D109	VCC_12V
A110	GND(FIXED)	B110	GND(FIXED)	C110	GND(FIXED)	D110	GND(FIXED)

Table 1 PCOM-B706GT Pin-Out

3 COM Express Interface

3.1 PCIe

PCOM-B706GT PCIe #0 ~ #31 Tx signal

Pin#	Pin Name	COM e 2.0/2.1 Specification (Signals Requiring Module Termination)	Pin Typ	B706GT Module	Pwr Rail /Tolerance(Volt)
A68	PCIE_TX0+	AC coupled on the Module	O PCIE	0.22uF AC coupled on the Module(Gen3/4).	AC coupled on Module
A69	PCIE_TX0−				
A64	PCIE_TX1+				
A65	PCIE_TX1−				
A61	PCIE_TX2+				
A62	PCIE_TX2−				
A58	PCIE_TX3+				
A59	PCIE_TX3−				
A55	PCIE_TX4+				
A56	PCIE_TX4−				
A52	PCIE_TX5+				
A53	PCIE_TX5−				
D19	PCIE_TX6+				
D20	PCIE_TX6−				
D22	PCIE_TX7+				
D23	PCIE_TX7−				
A71	PCIE_TX8+			0.22uF AC coupled on the Module(Gen3/4).	
A72	PCIE_TX8−				
A74	PCIE_TX9+				
A75	PCIE_TX9−				
A77	PCIE_TX10+				
A78	PCIE_TX10−				
A81	PCIE_TX11+				
A82	PCIE_TX11−				
A39	PCIE_TX12+				
A40	PCIE_TX12−				
A36	PCIE_TX13+				
A37	PCIE_TX13−				
A25	PCIE_TX14+				
A26	PCIE_TX14−				
A22	PCIE_TX15+				
A23	PCIE_TX15−				
D52	PCIE_TX16+				
D53	PCIE_TX16−				
D55	PCIE_TX17+				
D56	PCIE_TX17−				
D58	PCIE_TX18+				
D59	PCIE_TX18−				
D61	PCIE_TX19+				
D62	PCIE_TX19−				
D65	PCIE_TX20+				
D66	PCIE_TX20−				
D68	PCIE_TX21+				
D69	PCIE_TX21−				
D71	PCIE_TX22+				
D72	PCIE_TX22−				
D74	PCIE_TX23+				
D75	PCIE_TX23−				
D78	PCIE_TX24+				
D79	PCIE_TX24−				
D81	PCIE_TX25+				
D82	PCIE_TX25−				
D85	PCIE_TX26+				
D86	PCIE_TX26−				
D88	PCIE_TX27+				
D89	PCIE_TX27−				
D91	PCIE_TX28+				
D92	PCIE_TX28−				
D94	PCIE_TX29+				
D95	PCIE_TX29−				
D98	PCIE_TX30+				
D99	PCIE_TX30−				
D101	PCIE_TX31+				
D102	PCIE_TX31−				

Table 2 B706GT PCIE TX

PCOM-B706GT PCIe #0 ~ #31 Rx signal

Pin#	Pin Name	COMe 3.0 Specification (Signals Requiring Module Termination)	Pin Typ	B706GT Module	Pwr Rail / Tolerance(Volt)
B68	PCIE_RX0+	AC coupled off the Module.	I PCIE	AC coupled off Module	AC coupled off Module
B69	PCIE_RX0-				
B64	PCIE_RX1+				
B65	PCIE_RX1-				
B61	PCIE_RX2+				
B62	PCIE_RX2-				
B58	PCIE_RX3+				
B59	PCIE_RX3-				
B55	PCIE_RX4+				
B56	PCIE_RX4-				
B52	PCIE_RX5+				
B53	PCIE_RX5-				
C19	PCIE_RX6+				
C20	PCIE_RX6-				
C22	PCIE_RX7+				
C23	PCIE_RX7-				
B71	PCIE_RX8+				
B72	PCIE_RX8-				
B74	PCIE_RX9+				
B75	PCIE_RX9-				
B77	PCIE_RX10+				
B78	PCIE_RX10-				
B81	PCIE_RX11+				
B82	PCIE_RX11-				
B39	PCIE_RX12+				
B40	PCIE_RX12-				
B36	PCIE_RX13+				
B37	PCIE_RX13-				
B25	PCIE_RX14+				
B26	PCIE_RX14-				
B22	PCIE_RX15+				
B23	PCIE_RX15-				
C52	PCIE_RX16+				
C53	PCIE_RX16-				
C55	PCIE_RX17+				
C56	PCIE_RX17-				
C58	PCIE_RX18+				
C59	PCIE_RX18-				
C61	PCIE_RX19+				
C62	PCIE_RX19-				
C65	PCIE_RX20+				
C66	PCIE_RX20-				
C68	PCIE_RX21+				
C69	PCIE_RX21-				
C71	PCIE_RX22+				
C72	PCIE_RX22-				
C74	PCIE_RX23+				
C75	PCIE_RX23-				
C78	PCIE_RX24+				
C79	PCIE_RX24-				
C81	PCIE_RX25+				
C82	PCIE_RX25-				
C85	PCIE_RX26+				
C86	PCIE_RX26-				
C88	PCIE_RX27+				
C89	PCIE_RX27-				
C91	PCIE_RX28+				
C92	PCIE_RX28-				
C94	PCIE_RX29+				
C95	PCIE_RX29-				
C98	PCIE_RX30+				
C99	PCIE_RX30-				
C101	PCIE_RX31+				
C102	PCIE_RX31-				
A88	PCIE_CLK_REF+	Reference clock output for all PCI Express and PCI Express Graphics lanes.	O PCIE	-	PCIE
A89	PCIE_CLK_REF-				

Table 3 B706GT PCIE RX

3.1.1 AC Coupling Capacitor

PCIE / PEG AC Coupling : Device Down

While PCIE devices are designed on COM Express Carrier Board, the AC coupling Capacitor should be added on the carrier, please refer to below diagram.

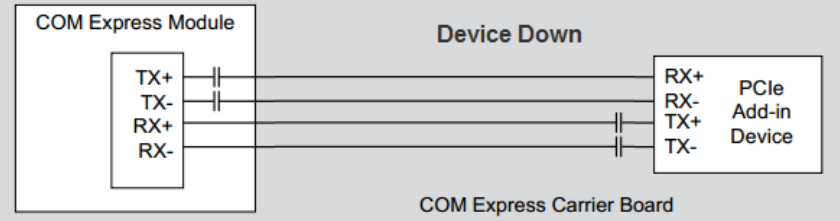


Figure 2 PCIE AC Coupling Capacitor - Device Down

(From PICMG COM Express Carrier Board Design Guide)

PCIE / PEG AC Coupling : Add-In Card

While PCIE devices are designed as Add In Card, the AC coupling Capacitor should be on PCIe Add-In Card, rather than on the COM Express Carrier Board, please refer to below diagram.

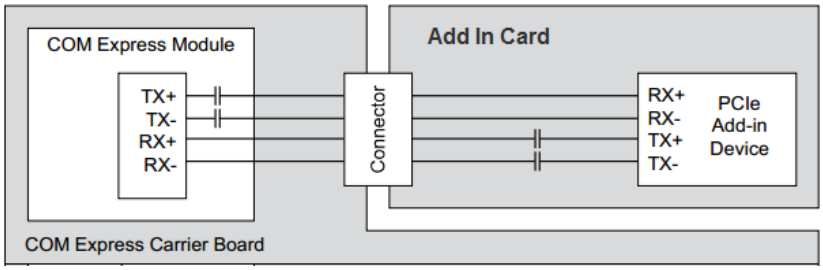


Figure 3 PCIE AC Coupling Capacitor - Add In Card

(From PICMG COM Express Carrier Board Design Guide)

3.1.2 PCB layout guideline - PCIe/PEG

Parameter	PCIe Gen2 / Gen3	PCIe Gen4
Bandwidth	5G / 8G	16 G
Maximum signal line length (coupled traces) TX and RX	12.0/10 inch (Add In Card/ Device Down)	10/9 inch (Add In Card/ Device Down)
Differential impedance	85 Ω +/-10%	85 Ω +/-10%
Single-ended Impedance	50 Ω +/-10%	50 Ω +/-10%
Trace width (W)	4.5 mil PCB stack-up dependent	4.5 mil PCB stack-up dependent
Spacing between differential pairs (intra-pair) (S)	4.5 mil PCB stack-up dependent	4.5 mil PCB stack-up dependent
Spacing between RX and TX pairs (inter-pair) (s)	Microstrip > 7H Stripline > 5H	Microstrip > 9H Stripline > 5H
Length matching between differential pairs (intra-pair)	Max. 5mils	Max. 5mils
Reference plane	GND referenced preferred	GND referenced preferred
Spacing from edge of plane	Min. 10*W mils (W=trace width)	Min. 10*W mils (W=trace width)
Via Usage	Max. 2 vias/ Max. 1 vias (Add In Card/ Device Down)	Max. 2 vias/ Max. 1 vias (Add In Card/ Device Down)

Table 4 PCIE/PEG Layout information

3.1.3 Passive Devices

AC Cap value (Gen2)	Min = 75nf Max = 200nf	PCOM-B706GT AC Cap value 220nF
AC Cap value (Gen3/Gen4)	Min = 176nf Max = 265nf	

Table 5 PCIE/PEG AC coupling capacitor value

3.1.4 Reference schematic - PCOM-C701 ZR1

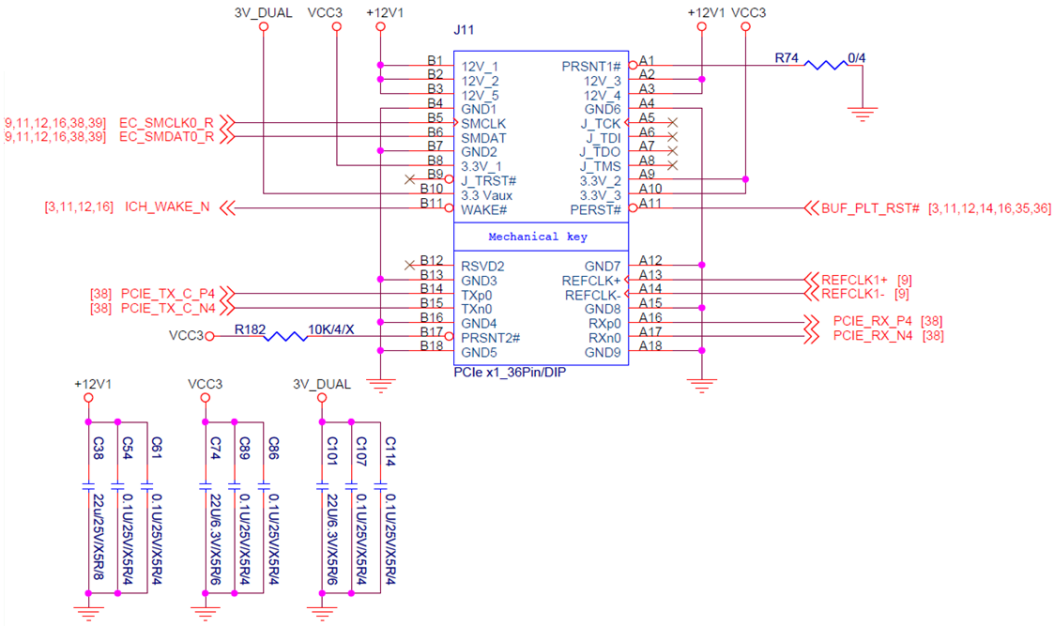


Figure 4 PCIEx1 reference schematic-1

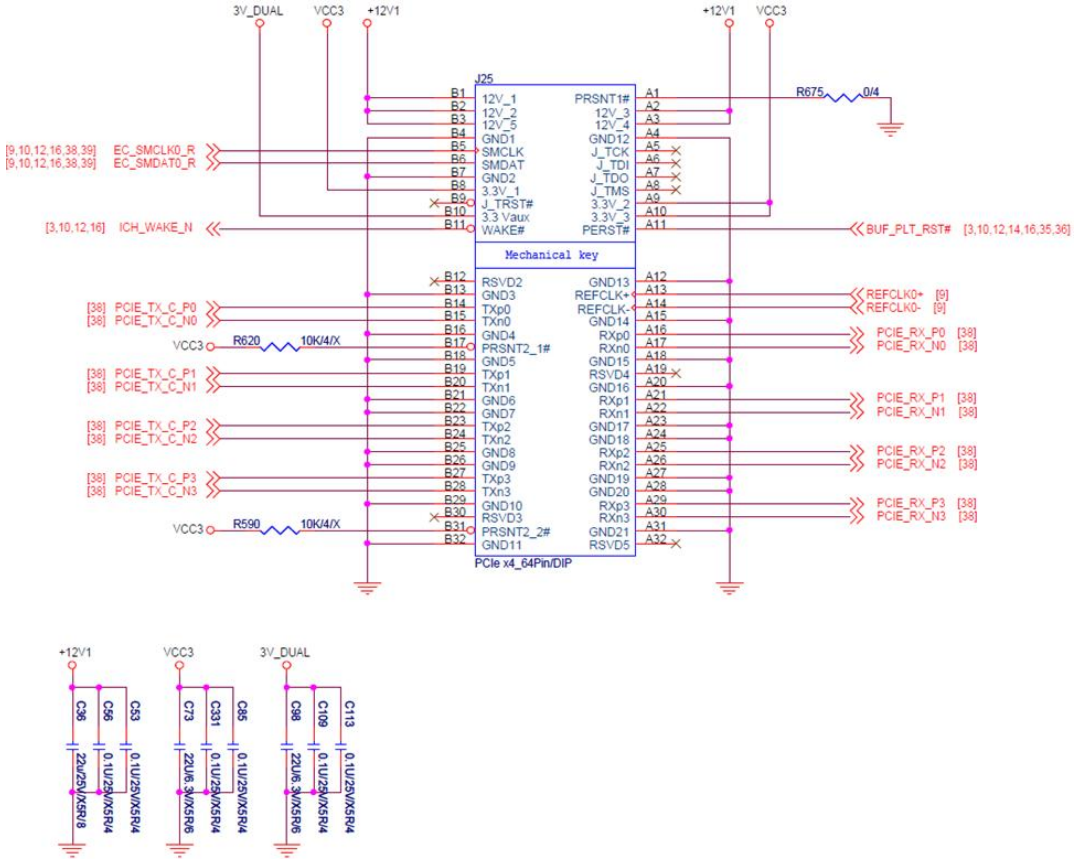


Figure 5 PCIEx4 reference schematic-2

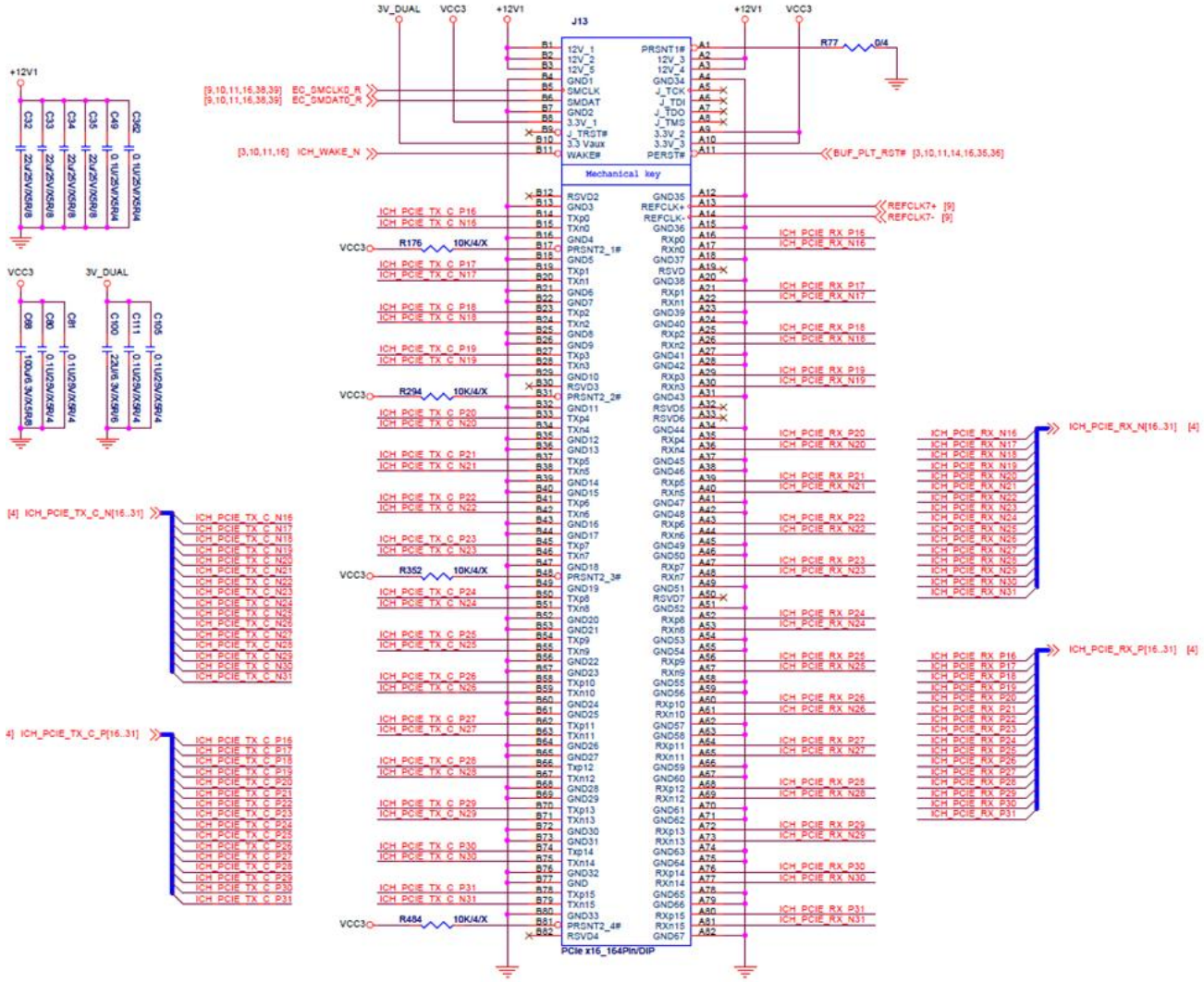


Figure 6 PCIEx16 reference schematic-3

3.1.5 Max trace length and available carrier trace length - PCIe (Device Down)

PCIe Device Down Topology

PIN	Name	Module Length	Max Length	Available Carrier length (Device Down Topology)
A68	PCIE_TX0+	2597.92	9000	6402.08
A69	PCIE_TX0-	2600.45	9000	6399.55
A64	PCIE_TX1+	2548.03	9000	6451.97
A65	PCIE_TX1-	2546.97	9000	6453.03
A61	PCIE_TX2+	2789.57	9000	6210.43
A62	PCIE_TX2-	2790.41	9000	6209.59
A58	PCIE_TX3+	2662.08	9000	6337.92
A59	PCIE_TX3-	2666.26	9000	6333.74
A55	PCIE_TX4+	2631.55	9000	6368.45
A56	PCIE_TX4-	2634.46	9000	6365.54
A52	PCIE_TX5+	2772.68	9000	6227.32
A53	PCIE_TX5-	2767.82	9000	6232.18
D19	PCIE_TX6+			
D20	PCIE_TX6-			
D22	PCIE_TX7+			
D23	PCIE_TX7-			
A71	PCIE_TX8+			
A72	PCIE_TX8-			
A74	PCIE_TX9+			
A75	PCIE_TX9-			
A77	PCIE_TX10+			
A78	PCIE_TX10-			
A81	PCIE_TX11+			
A82	PCIE_TX11-			
A39	PCIE_TX12+			
A40	PCIE_TX12-			
A36	PCIE_TX13+			
A37	PCIE_TX13-			
A25	PCIE_TX14+			
A26	PCIE_TX14-			
A22	PCIE_TX15+			

A23	PCIE_TX15-			
D52	PCIE_TX16+	2388.34	9000	6611.66
D53	PCIE_TX16-	2390.53	9000	6609.47
D55	PCIE_TX17+	2334.05	9000	6665.95
D56	PCIE_TX17-	2336.47	9000	6663.53
D58	PCIE_TX18+	2144.51	9000	6855.49
D59	PCIE_TX18-	2144.54	9000	6855.46
D61	PCIE_TX19+	2043.25	9000	6956.75
D62	PCIE_TX19-	2044.71	9000	6955.29
D65	PCIE_TX20+	1980.57	9000	7019.43
D66	PCIE_TX20-	1985.22	9000	7014.78
D68	PCIE_TX21+	1756.89	9000	7243.11
D69	PCIE_TX21-	1759.33	9000	7240.67
D71	PCIE_TX22+	1679.25	9000	7320.75
D72	PCIE_TX22-	1682.14	9000	7317.86
D74	PCIE_TX23+	1665.65	9000	7334.35
D75	PCIE_TX23-	1665.94	9000	7334.06
D78	PCIE_TX24+			
D79	PCIE_TX24-			
D81	PCIE_TX25+			
D82	PCIE_TX25-			
D85	PCIE_TX26+			
D86	PCIE_TX26-			
D88	PCIE_TX27+			
D89	PCIE_TX27-			
D91	PCIE_TX28+			
D92	PCIE_TX28-			
D94	PCIE_TX29+			
D95	PCIE_TX29-			
D98	PCIE_TX30+			
D99	PCIE_TX30-			
D101	PCIE_TX31+			
D102	PCIE_TX31-			
B68	PCIE_RX0+	2190.68	9000	6809.32
B69	PCIE_RX0-	2186.77	9000	6813.23
B64	PCIE_RX1+	2310.45	9000	6689.55
B65	PCIE_RX1-	2306.61	9000	6693.39
B61	PCIE_RX2+	2247.03	9000	6752.97

B62	PCIE_RX2-	2248.92	9000	6751.08
B58	PCIE_RX3+	2295.32	9000	6704.68
B59	PCIE_RX3-	2290.97	9000	6709.03
B55	PCIE_RX4+	2389.89	9000	6610.11
B56	PCIE_RX4-	2385.53	9000	6614.47
B52	PCIE_RX5+	2641.51	9000	6358.49
B53	PCIE_RX5-	2643.16	9000	6356.84
C19	PCIE_RX6+			
C20	PCIE_RX6-			
C22	PCIE_RX7+			
C23	PCIE_RX7-			
B71	PCIE_RX8+			
B72	PCIE_RX8-			
B74	PCIE_RX9+			
B75	PCIE_RX9-			
B77	PCIE_RX10+			
B78	PCIE_RX10-			
B81	PCIE_RX11+			
B82	PCIE_RX11-			
B39	PCIE_RX12+			
B40	PCIE_RX12-			
B36	PCIE_RX13+			
B37	PCIE_RX13-			
B25	PCIE_RX14+			
B26	PCIE_RX14-			
B22	PCIE_RX15+			
B23	PCIE_RX15-			
C52	PCIE_RX16+	2775.38	9000	6224.62
C53	PCIE_RX16-	2773.26	9000	6226.74
C55	PCIE_RX17+	2720.6	9000	6279.4
C56	PCIE_RX17-	2716.64	9000	6283.36
C58	PCIE_RX18+	2723.86	9000	6276.14
C59	PCIE_RX18-	2725.05	9000	6274.95
C61	PCIE_RX19+	2603.47	9000	6396.53
C62	PCIE_RX19-	2600.87	9000	6399.13
C65	PCIE_RX20+	2540.48	9000	6459.52
C66	PCIE_RX20-	2535.8	9000	6464.2
C68	PCIE_RX21+	2519.16	9000	6480.84

C69	PCIE_RX21-	2522.26	9000	6477.74
C71	PCIE_RX22+	2539.99	9000	6460.01
C72	PCIE_RX22-	2539.75	9000	6460.25
C74	PCIE_RX23+	2377.17	9000	6622.83
C75	PCIE_RX23-	2373.81	9000	6626.19
C78	PCIE_RX24+			
C79	PCIE_RX24-			
C81	PCIE_RX25+			
C82	PCIE_RX25-			
C85	PCIE_RX26+			
C86	PCIE_RX26-			
C88	PCIE_RX27+			
C89	PCIE_RX27-			
C91	PCIE_RX28+			
C92	PCIE_RX28-			
C94	PCIE_RX29+			
C95	PCIE_RX29-			
C98	PCIE_RX30+			
C99	PCIE_RX30-			
C101	PCIE_RX31+			
C102	PCIE_RX31-			
A88	PCIE_CLK_REF+	3318.07	-	-
A89	PCIE_CLK_REF-	3320.29	-	-

Table 6 PCIE carrier available traces - Device Down

3.1.6 Max trace length and available carrier trace length - PCIe (Add In Card)

PCIe Add In Card topology

PIN	Name	Module Length	Max Length	Available Carrier length ((AIC Topology)
A68	PCIE_TX0+	2597.92	9000	6402.08
A69	PCIE_TX0-	2600.45	9000	6399.55
A64	PCIE_TX1+	2548.03	9000	6451.97
A65	PCIE_TX1-	2546.97	9000	6453.03
A61	PCIE_TX2+	2789.57	9000	6210.43
A62	PCIE_TX2-	2790.41	9000	6209.59
A58	PCIE_TX3+	2662.08	9000	6337.92
A59	PCIE_TX3-	2666.26	9000	6333.74
A55	PCIE_TX4+	2631.55	9000	6368.45
A56	PCIE_TX4-	2634.46	9000	6365.54
A52	PCIE_TX5+	2772.68	9000	6227.32
A53	PCIE_TX5-	2767.82	9000	6232.18
D19	PCIE_TX6+			
D20	PCIE_TX6-			
D22	PCIE_TX7+			
D23	PCIE_TX7-			
A71	PCIE_TX8+			
A72	PCIE_TX8-			
A74	PCIE_TX9+			
A75	PCIE_TX9-			
A77	PCIE_TX10+			
A78	PCIE_TX10-			
A81	PCIE_TX11+			
A82	PCIE_TX11-			
A39	PCIE_TX12+			
A40	PCIE_TX12-			
A36	PCIE_TX13+			
A37	PCIE_TX13-			
A25	PCIE_TX14+			
A26	PCIE_TX14-			
A22	PCIE_TX15+			

A23	PCIE_TX15-			
D52	PCIE_TX16+	2388.34	9000	6611.66
D53	PCIE_TX16-	2390.53	9000	6609.47
D55	PCIE_TX17+	2334.05	9000	6665.95
D56	PCIE_TX17-	2336.47	9000	6663.53
D58	PCIE_TX18+	2144.51	9000	6855.49
D59	PCIE_TX18-	2144.54	9000	6855.46
D61	PCIE_TX19+	2043.25	9000	6956.75
D62	PCIE_TX19-	2044.71	9000	6955.29
D65	PCIE_TX20+	1980.57	9000	7019.43
D66	PCIE_TX20-	1985.22	9000	7014.78
D68	PCIE_TX21+	1756.89	9000	7243.11
D69	PCIE_TX21-	1759.33	9000	7240.67
D71	PCIE_TX22+	1679.25	9000	7320.75
D72	PCIE_TX22-	1682.14	9000	7317.86
D74	PCIE_TX23+	1665.65	9000	7334.35
D75	PCIE_TX23-	1665.94	9000	7334.06
D78	PCIE_TX24+			
D79	PCIE_TX24-			
D81	PCIE_TX25+			
D82	PCIE_TX25-			
D85	PCIE_TX26+			
D86	PCIE_TX26-			
D88	PCIE_TX27+			
D89	PCIE_TX27-			
D91	PCIE_TX28+			
D92	PCIE_TX28-			
D94	PCIE_TX29+			
D95	PCIE_TX29-			
D98	PCIE_TX30+			
D99	PCIE_TX30-			
D101	PCIE_TX31+			
D102	PCIE_TX31-			
B68	PCIE_RX0+	2190.68	9000	6809.32
B69	PCIE_RX0-	2186.77	9000	6813.23
B64	PCIE_RX1+	2310.45	9000	6689.55
B65	PCIE_RX1-	2306.61	9000	6693.39
B61	PCIE_RX2+	2247.03	9000	6752.97

B62	PCIE_RX2-	2248.92	9000	6751.08
B58	PCIE_RX3+	2295.32	9000	6704.68
B59	PCIE_RX3-	2290.97	9000	6709.03
B55	PCIE_RX4+	2389.89	9000	6610.11
B56	PCIE_RX4-	2385.53	9000	6614.47
B52	PCIE_RX5+	2641.51	9000	6358.49
B53	PCIE_RX5-	2643.16	9000	6356.84
C19	PCIE_RX6+			
C20	PCIE_RX6-			
C22	PCIE_RX7+			
C23	PCIE_RX7-			
B71	PCIE_RX8+			
B72	PCIE_RX8-			
B74	PCIE_RX9+			
B75	PCIE_RX9-			
B77	PCIE_RX10+			
B78	PCIE_RX10-			
B81	PCIE_RX11+			
B82	PCIE_RX11-			
B39	PCIE_RX12+			
B40	PCIE_RX12-			
B36	PCIE_RX13+			
B37	PCIE_RX13-			
B25	PCIE_RX14+			
B26	PCIE_RX14-			
B22	PCIE_RX15+			
B23	PCIE_RX15-			
C52	PCIE_RX16+	2775.38	9000	6224.62
C53	PCIE_RX16-	2773.26	9000	6226.74
C55	PCIE_RX17+	2720.6	9000	6279.4
C56	PCIE_RX17-	2716.64	9000	6283.36
C58	PCIE_RX18+	2723.86	9000	6276.14
C59	PCIE_RX18-	2725.05	9000	6274.95
C61	PCIE_RX19+	2603.47	9000	6396.53
C62	PCIE_RX19-	2600.87	9000	6399.13
C65	PCIE_RX20+	2540.48	9000	6459.52
C66	PCIE_RX20-	2535.8	9000	6464.2
C68	PCIE_RX21+	2519.16	9000	6480.84

C69	PCIE_RX21-	2522.26	9000	6477.74
C71	PCIE_RX22+	2539.99	9000	6460.01
C72	PCIE_RX22-	2539.75	9000	6460.25
C74	PCIE_RX23+	2377.17	9000	6622.83
C75	PCIE_RX23-	2373.81	9000	6626.19
C78	PCIE_RX24+			
C79	PCIE_RX24-			
C81	PCIE_RX25+			
C82	PCIE_RX25-			
C85	PCIE_RX26+			
C86	PCIE_RX26-			
C88	PCIE_RX27+			
C89	PCIE_RX27-			
C91	PCIE_RX28+			
C92	PCIE_RX28-			
C94	PCIE_RX29+			
C95	PCIE_RX29-			
C98	PCIE_RX30+			
C99	PCIE_RX30-			
C101	PCIE_RX31+			
C102	PCIE_RX31-			
A88	PCIE_CLK_REF+	3120	-	-
A89	PCIE_CLK_REF-	3122.37	-	-

Table 7 PCIE carrier available traces - Add In Card

3.2 USB 2.0/3.0

PCOM- B706GT USB2.0

Pin#	Pin Name	COM e 2.0/2.1 Specification (Signals Requiring Module Termination)	Pin Typ	B706GT Module	Pwr Rail /Tolerance(Volt)
A45	USB0-	No termination is required on USB pairs.	I/O USB	SoC to Com Express Row connector.	3.3V Suspend/3.3V
A46	USB0+				
B45	USB1-				
B46	USB1+				
A42	USB2-				
A43	USB2+				
B42	USB3-				
B43	USB3+				
B44	USB_0_1_OC#	Pulled up to 3.3V standby on module with a 10K Ω resistor	I CMOS	PU 10k ohm	3.3V Suspend/3.3V
A44	USB_2_3_OC#				

Table 8 B706GT USB 2.0

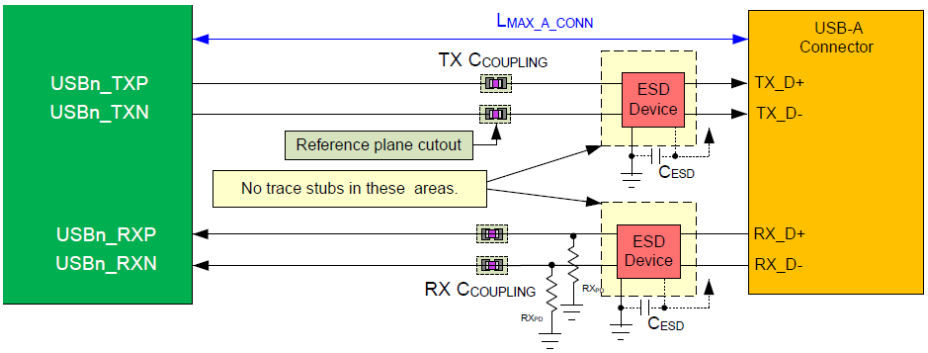
PCOM- B706GT USB3.0

Pin#	Pin Name	COM e 2.0/2.1 Specification (Signals Requiring Module Termination)	Pin Typ	B706GT Module	Pwr Rail /Tolerance(Volt)
C3	USB_SSRX0-	AC coupled off Module.	I PCIE	0.33uF AC coupled on the Module for AMD	AC coupled off Module.
C4	USB_SSRX0+				
C6	USB_SSRX1-				
C7	USB_SSRX1+				
C9	USB_SSRX2-				
C10	USB_SSRX2+				
C12	USB_SSRX3-				
C13	USB_SSRX3+				
D3	USB_SSTX0-	AC coupled on Module.	O PCIE	0.22uF AC coupled on the Module	AC coupled on Module
D4	USB_SSTX0+				
D6	USB_SSTX1-				
D7	USB_SSTX1+				
D9	USB_SSTX2-				
D10	USB_SSTX2+				
D12	USB_SSTX3-				
D13	USB_SSTX3+				

Table 9 B706GT USB 3.0

Note

RX_{PD}: pull-down resistor to VSS, it is recommended to reserve



3.2.1 PCB layout guideline - USB2.0/3.0

Parameter	Trace Routing	Trace Routing
Transfer rate / Port	480 Mbit/s	5/10 Gbit/s
Maximum signal line length (coupled traces)	Max. 12.0 inches	Max. 5 inches/
Differential Impedance	85 Ω +/-10%	85 Ω +/-10%
Single-ended Impedance	50 Ω +/-10%	50 Ω +/-10%
Trace width (W)	4.5 mil PCB stack-up dependent	4.5 mil PCB stack-up dependent
Spacing between differential pairs (intra-pair) (S)	4.5 mil PCB stack-up dependent	4.5 mil PCB stack-up dependent
Spacing between RX and TX, RX and RX pairs (inter-pair) (s)	Microstrip > 7H Stripline > 7H	Microstrip > 10H Stripline > 8H
Spacing between TX and TX pairs (inter-pair) (s)	Microstrip > 7H Stripline > 7H	Microstrip > 7H Stripline > 6H
Length matching between differential pairs (intra-pair)	5 mils	3 mils
Reference plane	GND referenced preferred	GND referenced preferred
Spacing from edge of plane	Min. 10*W mils (W=trace width)	Min. 10*W mils (W=trace width)
Via Usage	Max. 1 vias	Max. 1 vias

Table 10 USB 2.0 / 3.0 Layout information

3.2.2 Reference schematic - PCOM-C701 ZR1

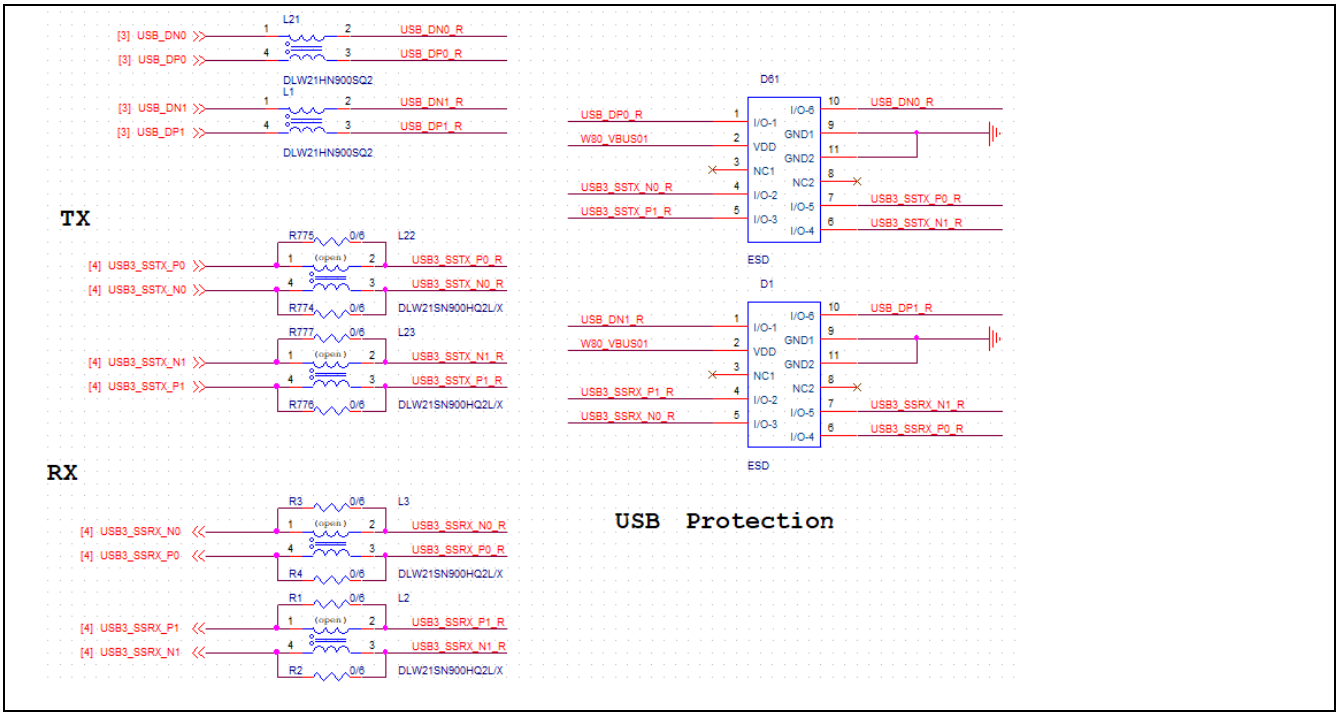


Figure 7 USB 2.0 / 3.0 Reference schematic 1

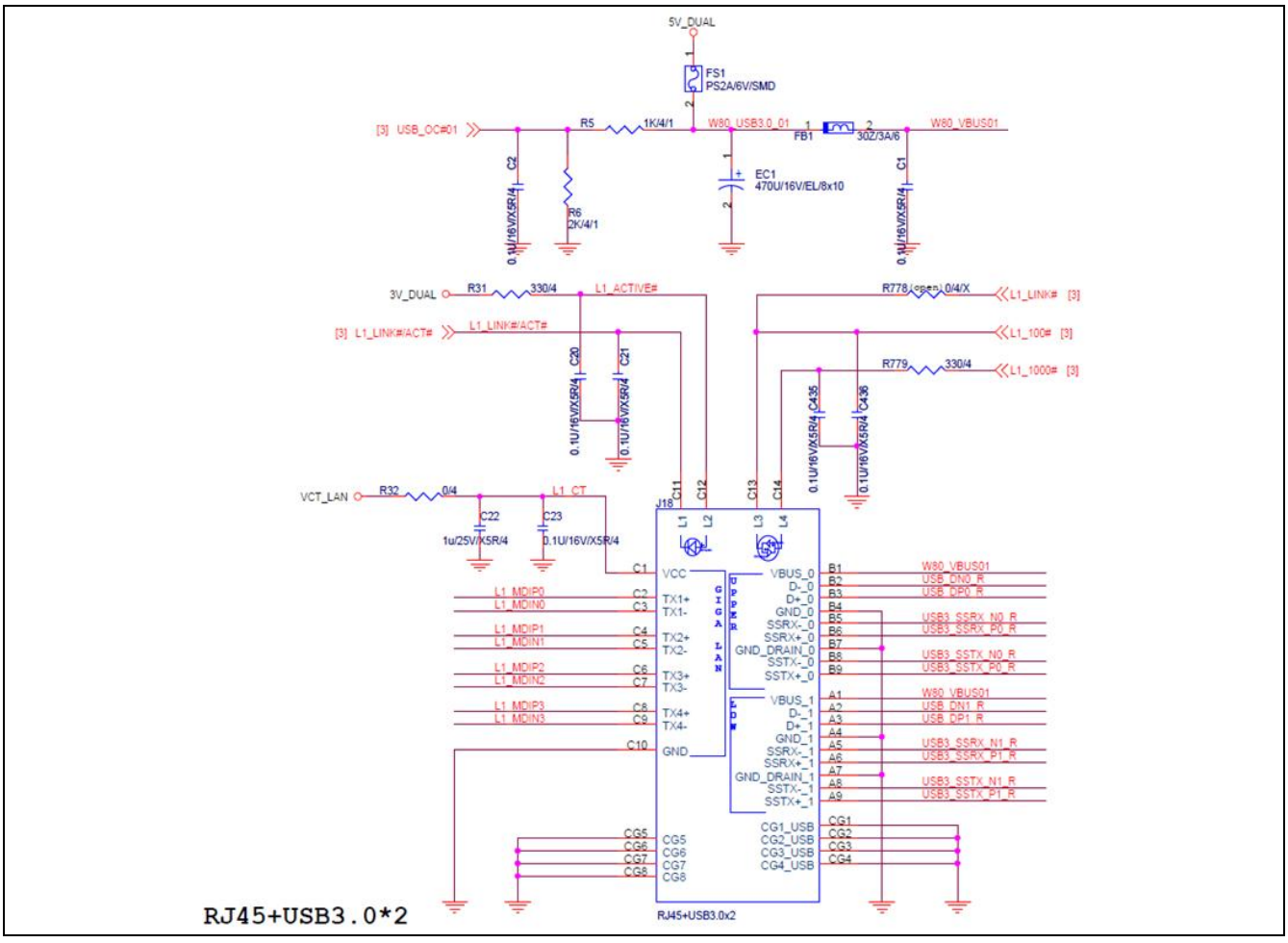


Figure 8 USB 2.0 / 3.0 Reference schematic 2

3.2.3 Max trace length and available carrier trace length - USB 2.0 / 3.0

PIN	Name	Module Length	Max Length	Available Carrier length
A45	USB0-	3838.17	12000	8161.83
A46	USB0+	3839.37	12000	8160.63
B45	USB1-	3663.29	12000	8336.71
B46	USB1+	3666.17	12000	8333.83
A42	USB2-	4243.59	12000	7756.41
A43	USB2+	4243.77	12000	7756.23
B42	USB3-	3626.54	12000	8373.46
B43	USB3+	3623.34	12000	8376.66
C3	USB_SSRX0-	3759.5	5000	1240.5
C4	USB_SSRX0+	3760.68	5000	1239.32
C6	USB_SSRX1-	3546.27	5000	1453.73
C7	USB_SSRX1+	3545.53	5000	1454.47
C9	USB_SSRX2-	3448.82	5000	1551.18
C10	USB_SSRX2+	3448.19	5000	1551.81
C12	USB_SSRX3-	3339.2	5000	1660.8
C13	USB_SSRX3+	3338.37	5000	1661.63
D3	USB_SSTX0-	3353.06	5000	1646.94
D4	USB_SSTX0+	3351.04	5000	1648.96
D6	USB_SSTX1-	3152.88	5000	1847.12
D7	USB_SSTX1+	3153.07	5000	1846.93
D9	USB_SSTX2-	2914.49	5000	2085.51
D10	USB_SSTX2+	2915.7	5000	2084.3
D12	USB_SSTX3-	2481.53	5000	2518.47
D13	USB_SSTX3+	2482.3	5000	2517.7

Table 11 Carrier available traces - USB 2.0 / 3.0

3.3 GbE LAN

PCOM-B706GT LAN

Pin#	Pin Name	COM e 2.0/2.1 Specification (Signals Requiring Module Termination)	Pin Typ	B706GT Module	Pwr Rail /Tolerance(Volt)
A12	GBE0_MDI0-	-	I/O Analog	Media Dependent Interface signal. I210 chip on Module.	3.3V max Suspend
A13	GBE0_MDI0+				
A9	GBE0_MDI1-				
A10	GBE0_MDI1+				
A6	GBE0_MDI2-				
A7	GBE0_MDI2+				
A2	GBE0_MDI3-				
A3	GBE0_MDI3+				
A8	GBE0_LINK#	-	OD CMOS	Gigabit Ethernet Controller 0 link indicator, active low.	3.3V Suspend/3.3V
A4	GBE0_LINK100#	-	OD CMOS	Gigabit Ethernet Controller 0 100 Mbit / sec link indicator, active low.	3.3V Suspend/3.3V
A5	GBE0_LINK1000#	-	OD CMOS	Gigabit Ethernet Controller 0 1000 Mbit / sec link indicator, active low.	3.3V Suspend/3.3V
A14	GBE0_CTREF	-	REF	Reserved resistor NP (Reference voltage for Carrier Board Ethernet channel 0 magnetics center	GND min 3.3V max
B2	GBE0_ACT#	-	OD CMOS	I210 chip to Com Express Row connector.	3.3V Suspend/3.3V

Table 12 B706GT LAN

3.3.1 PCB layout guideline - LAN

Parameter	Trace Routing
Differential Impedance	100 Ω +/-10%
Single-ended Impedance	50 Ω +/-10%
Trace width (W)	3.5 mil PCB stack-up dependent
Spacing between differential pairs (intra-pair) (S)	6.5 mil PCB stack-up dependent
Spacing between RX and TX pairs (inter-pair) (s)	Microstrip > 7H Stripline > 6H
Length matching between RX and TX pairs (inter-pair)	Max. 5mils
Spacing from edge of plane	Min. 10*W mils (W=trace width)

Table 13 LAN Layout information

3.3.2 Reference schematic - PCOM-C701-BMC ZR2

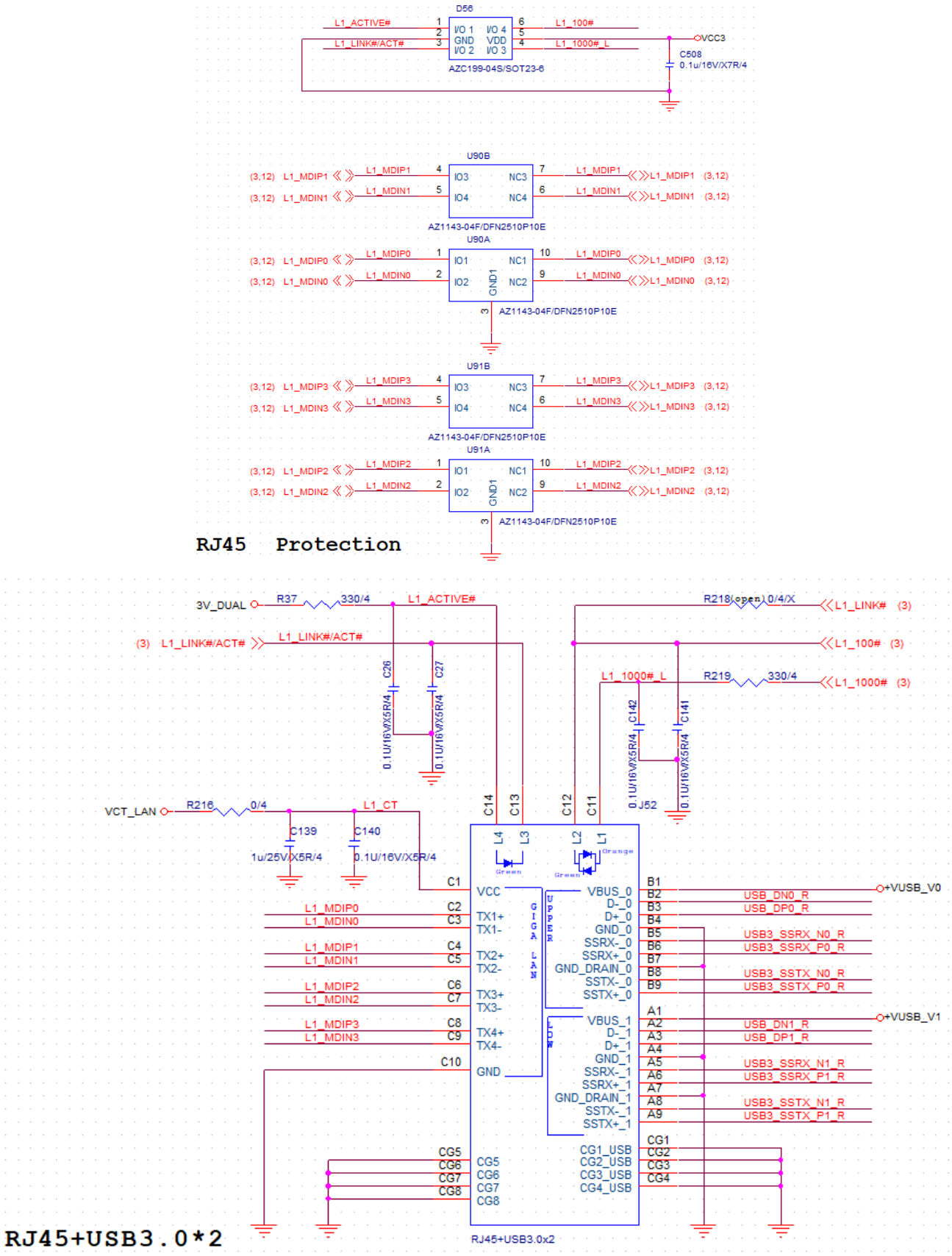


Figure 9 Reference schematic – LAN

3.3.3 Max trace length and available carrier trace length - LAN

PIN	Name	Module Length	Max Length	Available Carrier length
A13	GBE0_MDI0+	707.32	4000	3292.68
A12	GBE0_MDI0-	707.41	4000	3292.59
A10	GBE0_MDI1+	712.98	4000	3287.02
A9	GBE0_MDI1-	712.4	4000	3287.6
A7	GBE0_MDI2+	704.92	4000	3295.08
A6	GBE0_MDI2-	704.93	4000	3295.07
A3	GBE0_MDI3+	712.93	4000	3287.07
A2	GBE0_MDI3-	714.39	4000	3285.61

Table 14 Carrier available traces - LAN

3.4 SATA

PCOM-B706GT SATA

Pin#	Pin Name	COM e 2.0/2.1 Specification (Signals Requiring Module Termination)	Pin Typ	B706GT Module	Pwr Rail /Tolerance(Volt)
A16	SATA0_TX+	AC coupled on the Module	O SATA	0.01uF AC coupled on the Module(Gen3).	AC coupled on Module
A17	SATA0_TX−				
A19	SATA0_RX+		I SATA		
A20	SATA0_RX−				
B16	SATA1_TX+		O SATA		
B17	SATA1_TX−				
B19	SATA1_RX+		I SATA		
B20	SATA1_RX−				
A28	(S)ATA_ACT#		O/D(I/O) CMOS	PU 10k ohm	3.3V / 3.3V
B18	SUS_STAT#	Indicates imminent suspend operation; used to notify LPC devices	O CMOS	–	3.3VSuspend/ 3.3V

Table 15 B706GT SATA

3.4.1 PCB layout guideline -SATA

Parameter	Trace Routing
Transfer Rate	Up to 6.0 Gbit/s
Maximum signal line length (coupled traces)	5 inches
Differential Impedance	85 Ω +/-10%
Single-ended Impedance	50 Ω +/-10%
Trace width (W)	4.5 mil PCB stack-up dependent
Spacing between differential pairs (intra-pair) (S)	4.5mil PCB stack-up dependent
Spacing between RX and TX,pairs (inter-pair) (s)	Microstrip > 7H Stripline > 7H
Spacing between TX and TX pairs (inter-pair) (s)	Microstrip > 5H Stripline > 5H
Length matching between differential pairs (intra-pair)	Max. 5mils
Spacing from edge of plane	Min. 10*W mils (W=trace width)
Via Usage	A maximum of 1 vias is recommended.
AC Coupling capacitors	10nF

Table 16 SATA layout information

3.4.2 Reference schematic - PCOM-C701 ZR1

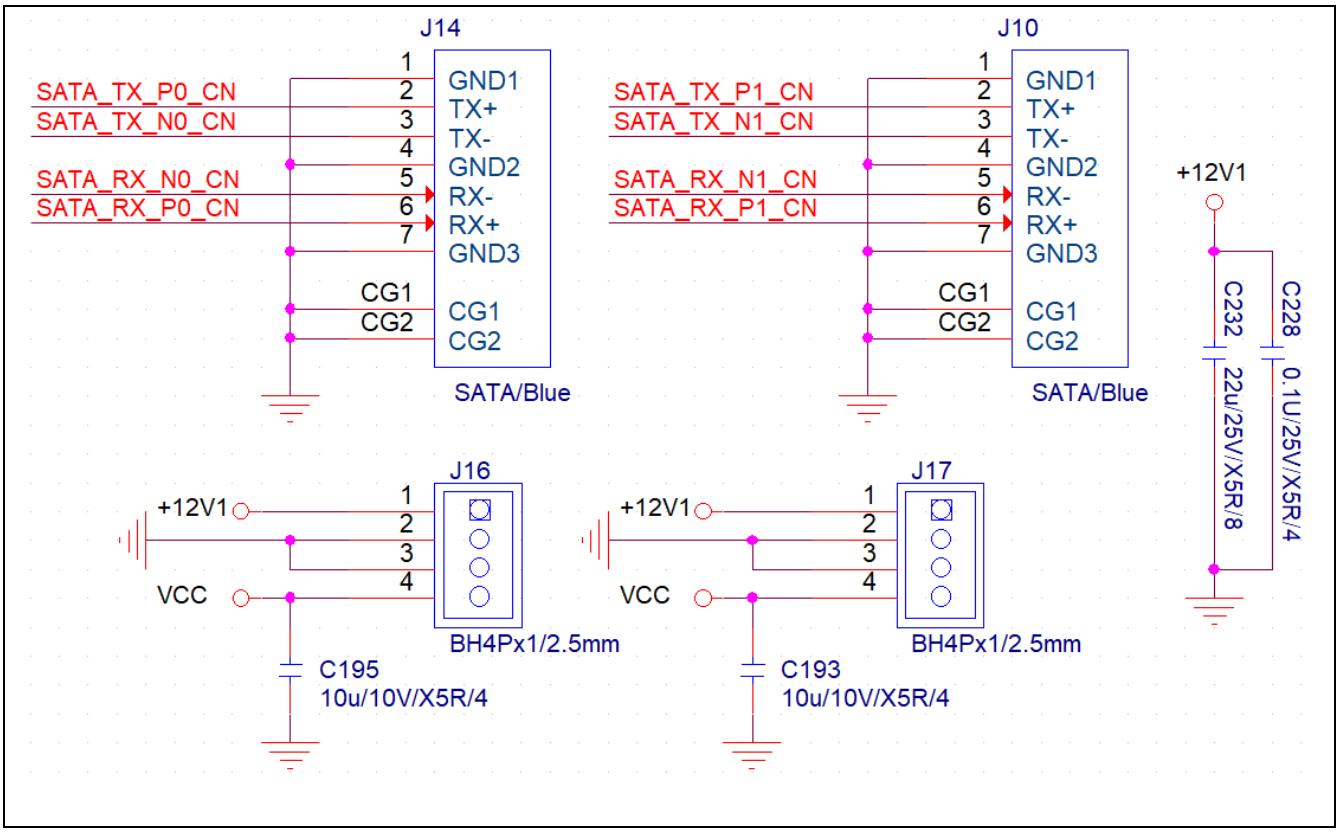


Figure 10 Reference schematic –SATA

3.4.3 Max trace length and available carrier trace length - SATA

PIN	Name	Module Length	Max Length	Available Carrier length
A16	SATA0_TX+	3463.74	5000	1536.26
A17	SATA0_TX-	3463.76	5000	1536.24
A19	SATA0_RX+	3429.12	5000	1570.88
A20	SATA0_RX-	3429.97	5000	1570.03
B16	SATA1_TX+	3197.3	5000	1802.7
B17	SATA1_TX-	3194.63	5000	1805.37
B19	SATA1_RX+	2954.73	5000	2045.27
B20	SATA1_RX-	2953.78	5000	2046.22

Table 17 Carrier available traces - SATA

3.5 NCSI

PCOM-B706GT NCSI

Pin#	Pin Name	Description	Pin Typ	B706GT Module follow intel	Pwr Rail /Tolerance(Volt)
A84	NCSI_TX_EN	NC-SI Transmit enable.	I CMOS	PD 10k ohm to GND	3.3V Suspend /3.3V
B91	NCSI_CLK_IN	NC-SI Clock reference for receive, transmit, and control interface			
B95	NCSI_TXD1	NC-SI Transmit Data		PU 10k ohm V_3P3M	
B96	NCSI_TXD0				
B98	NCSI_ARB_IN	NC-SI hardware arbitration input.		–	
B99	NCSI_ARB_OUT	NC-SI hardware arbitration output.	O CMOS		
B92	NCSI_RXD1	NC-SI Receive Data		PU 10k ohm V_3P3M	
B93	NCSI_RXD0				
B94	NCSI_CRS_DV	NC-SI Carrier Sense/Receive Data Valid to MC, indicating that the transmitted data from NC to BMC is valid.		PD 10k ohm to GND	

Table 18 B706GT NCSI

3.5.1 PCB layout guideline - NCSI

Parameter	Trace Routing
when using 4-point multi drop connections	5.5 inches
when using a point-to-point connection to the MC.	8 inches
Single-ended Impedance	50 Ω+/-10%
Trace width (W)	PCB stack-up dependent
Trace-to-trace space	12 mils (3h) PCB stack-up dependent

Table 19 NCSI Layout information

Note:

1. The clock-to-data signals length match should be done using the NC-SI timing analysis spreadsheet to ensure the timing restrictions are met while maintaining the routing length for both clock and data paths below the maximum values specified.

2. Intel I210 Layout check list NCSI recommend : total skew from the clock source to all devices should be less than 1 ns (less than or equal to ~5.5 inches trace length skew).

3.5.2 Max trace length and available carrier trace length - NCSI

PIN	Name	Module Length	Max Length	Available Carrier length
A84	NCSI_TX_EN	2045.05	8000	5954.95
B95	NCSI_TXD1	2281.6	8000	5718.4
B96	NCSI_TXD0	2295.39	8000	5704.61
B92	NCSI_RXD1	2245.19	8000	5754.81
B93	NCSI_RXD0	2259.79	8000	5740.21
B94	NCSI_CRS_DV	2183.95	8000	5816.05
B91	NCSI_CLK_IN	2102.83	8000	5897.17
B98	NCSI_ARB_IN	2742.4	8000	5257.6
B99	NCSI_ARB_OUT	2643.22	8000	5356.78

Table 20 Carrier available traces – NCSI

3.6 10GbE LAN

Pin#	Pin Name	Description	Pin Typ	B706GT Module	Pwr Rail /Tolerance(Volt)
D49	10G_KR_TX0+	10GBASE-KR ports, transmit output differential pairs.	O KR	no AC coupled on the Module reserve 0 ohm	
D50	10G_KR_TX0-				
D42	10G_KR_TX1+				
D43	10G_KR_TX1-				
C49	10G_KR_RX0+	10GBASE-KR ports, receive input differential pairs.	I KR	no AC coupled on the Module reserve 0 ohm	
C50	10G_KR_RX0-				
C42	10G_KR_RX1+				
C43	10G_KR_RX1-				
D39	10G_SFP_SCL0	reserve path,same C46 pin 10G_PHY_MDC_SCL0	I/O OD CMOS		3.3V Suspend /3.3V
C38	10G_SFP_SDA0	reserve path,same D46 pin 10G_PHY_MDIO_SDA0	I/O OD CMOS		3.3V Suspend /3.3V
C46	10G_PHY_MDC_SCL0	**MDIO Mode:** Management Data I/O Interface mode clock signal for serial data transfers between the MAC and an external PHY. ---------- **I2C Mode:** I2C Clock signal, of the 2-wire management interface used for serial data transfers between the MAC and an external PHY.	O CMOS ------- I/O OD CMOS	PU 10k ohm to +3V_Dual	3.3V Suspend /3.3V
D46	10G_PHY_MDIO_SDA0	**MDIO Mode:** Management Data I/O Interface mode clock signal for serial data transfers between the MAC and an external PHY. ---------- **I2C Mode:** I2C Clock signal, of the 2-wire management interface used for serial data transfers between the MAC and an external PHY.	O CMOS ------- I/O OD CMOS	PU 10k ohm to +3V_Dual	3.3V Suspend /3.3V
C40	10G_SDP0	Software-Definable Pins. Can also be used for IEEE1588 support	I/O CMOS	PU 2.2k ohm +3V_Dual	3.3V Suspend /3.3V
D40	10G_SDP1				
C17	10G_SDP2				
D17	10G_SDP3				
C47	10G_INT0	Interrupt pin from copper PHY or optical SFP Module to the 10GbE controller.	I CMOS	PU 1k ohm +3V_Dual	3.3V Suspend /3.3V

Table 21 B706GT 10GbE LAN

3.6.1 PCB layout guideline -10GbE LAN

Parameter	Trace Routing
Differential Impedance	85 Ω +/-10%
Single-ended Impedance	50 Ω +/-10%
Trace width (W)	4.5 mil PCB stack-up dependent
Spacing between differential pairs (intra-pair) (S)	4.5 mil PCB stack-up dependent
Spacing to other signals (Tx to Rx)	Microstrip > 7H Stripline > 7H PCB stack-up dependent
Length matching between differential pairs (intra-pair)	Max. 5mils

Table 22 10GbE LAN layout information

Note:

1. Implementations with SFP+ connectors do not require AC coupling capacitors on the motherboard as the SFP+ module provides the AC-coupling capacitors for both the transmit and receive lanes. (Refer to SFF-8431 specification.)

2. Implementation with a PHY/re-timer between SFP+ connector and the processor may require AC coupling capacitors depending on whether the PHY/re-timer has an integrated AC coupling capacitor or not. Implementations with PHY/re-timer must follow the recommendations from the vendor

3.6.2 Reference schematic – AMD PDG

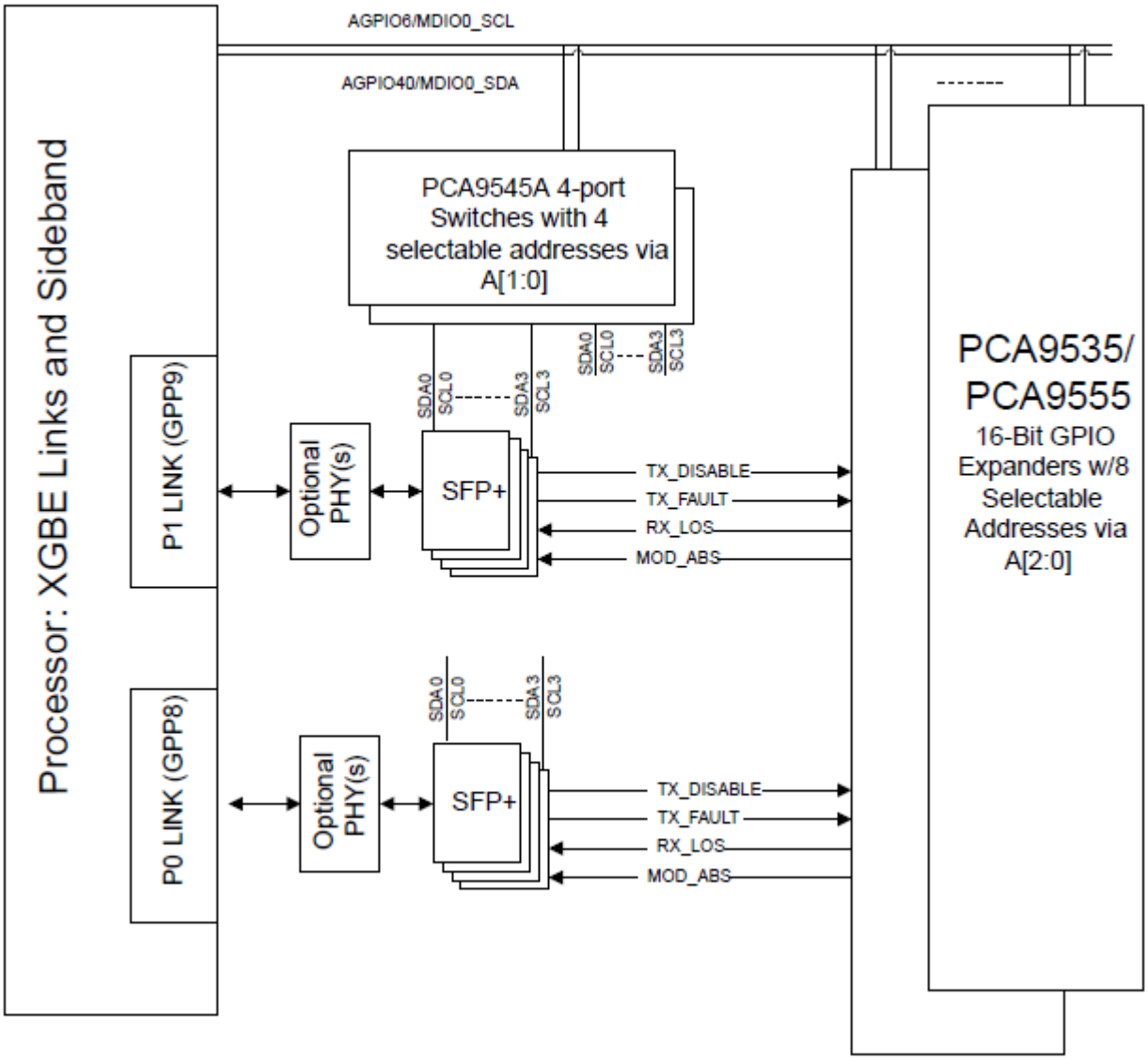


Figure 11 Reference schematic – 10GbE LAN

3.6.3 Max trace length and available carrier trace length - 10GbE LAN

PIN	Name	Module Length	Max Length	Available Carrier length
D49	10G_TX0+	2632.13	6000	3367.87
D50	10G_TX0-	2631.12	6000	3368.88
D42	10G_TX1+	2404.72	6000	3595.28
D43	10G_TX1-	2408.4	6000	3591.6
C49	10G_RX0+	2805.45	6000	3194.55
C50	10G_RX0-	2805.87	6000	3194.13
C42	10G_RX1+	2711.31	6000	3288.69
C43	10G_RX1-	2712.04	6000	3287.96

Table 23 Carrier available traces - 10GbE LAN

3.7 UART

PCOM- B706GT UART

Pin#	Pin Name	Description	Pin Typ	B706GT Module	Pwr Rail /Tolerance(Volt)
A98	SER0_TX	General purpose serial port transmitter	O CMOS	Series connection Schottky diode	3.3V / 12V
A99	SER0_RX	General purpose serial port receiver	I CMOS		
A101	SER1_TX	General purpose serial port transmitter / CAN_TX	O CMOS		
A102	SER1_RX	General purpose serial port receiver / CAN_RX	I CMOS		

Table 24 B706GT UART

3.7.1 Reference schematic - PCOM-C701 ZR1

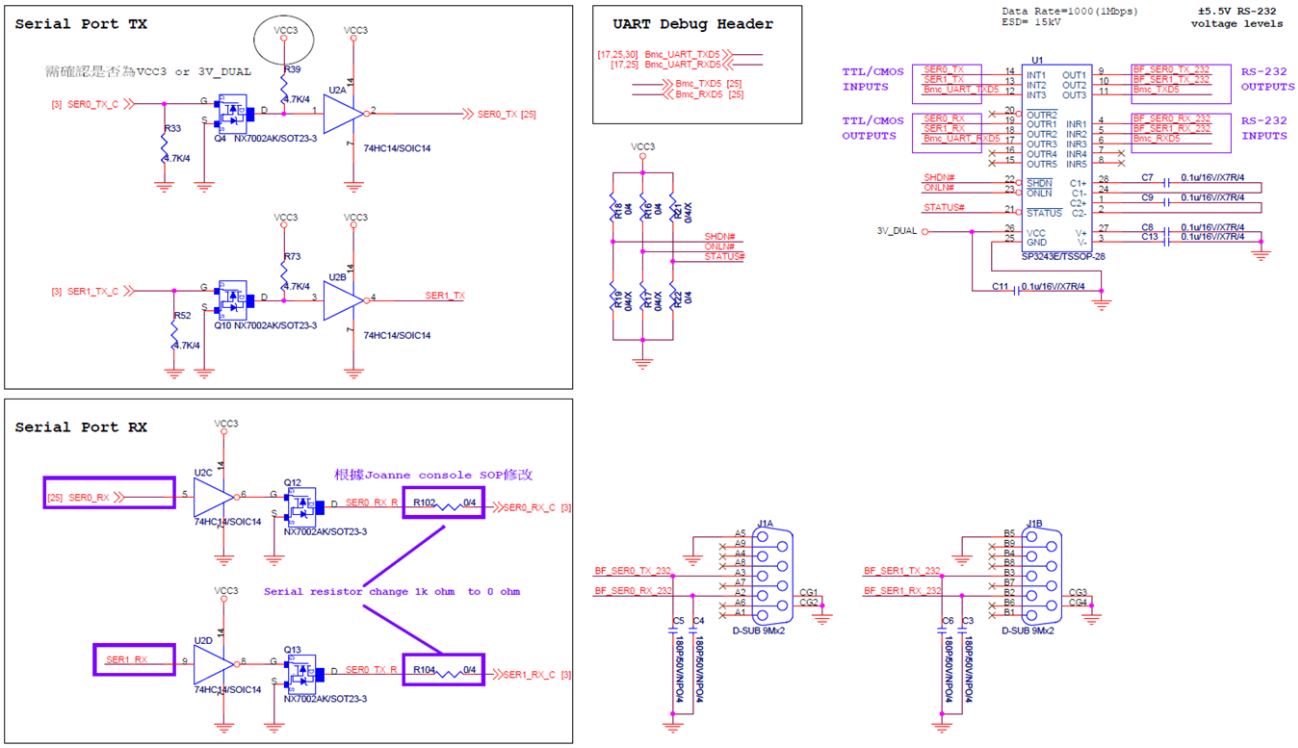


Figure 12 Reference schematic –UART

3.8 I2C

PCOM-B706GT I2C

Pin#	Pin Name	Description	Pin Typ	B706GT Module	Pwr Rail /Tolerance(Volt)
B33	I2C_CLK	General purpose I2C port clock output	I/O OD CMOS	PU 2.2k ohm to +3V_Dual.	3.3V Suspend/ 3.3V
B34	I2C_DAT	General purpose I2C port data I/O line			

Table 25 B706GT I2C

3.9 SMBus

PCOM- B706GT SMBus

Pin#	Pin Name	Description	Pin Typ	B706GT Module	Pwr Rail /Tolerance(Volt)
B13	SMB_CK	System Management Bus bidirectional clock line	I/O OD CMOS	PU 2.2K ohm to +3V_Dual.	3.3V Suspend/ 3.3V
B14	SMB_DAT	System Management Bus bidirectional data line			
B15	SMB_ALERT#	System Management Bus Alert – active low input can be used to generate an SMI# (System Management Interrupt) or to wake the system.	I CMOS		

Table 26 B706GT SMBus

3.10 GPIO

PCOM- B706GT GPIO

Pin#	Pin Name	Description	Pin Typ	B706GT Module	Pwr Rail /Tolerance(Volt)
A54	GPI0	General purpose input pins. Pulled high internally on the Module.	I CMOS	PU 5.6k ohm to +3.3V.	3.3V/3.3V
A63	GPI1				
A67	GPI2				
A85	GPI3				
A93	GPO0	–	O CMOS	EC to Com Express Row connector.	3.3V/ 3.3V
B54	GPO1				
B57	GPO2				
B63	GPO3				

Table 27 B706GT GPIO

3.11 LPC

PCOM-B706GT LPC

Pin#	Pin Name	Description	Pin Typ	B706GT Module	Pwr Rail /Tolerance(Volt)
A50	LPC_SERIRQ	LPC Mode: LPC serial interrup	I/O CMOS	PU 4.7k ohm to +3.3V	3.3V/3.3V
B3	LPC_FRAME#	LPC frame indicates the start of an LPC cycle	O CMOS	Bridge to Com Express Row connector	
B4	LPC_AD0	LPC Mode: LPC multiplexed address, command and data bus	I/O CMOS		
B5	LPC_AD1				
B6	LPC_AD2				
B7	LPC_AD3				
B8	LPC_DRQ0#	LPC Mode: LPC serial DMA request	I CMOS	NC	
B9	LPC_DRQ1#				
B10	LPC_CLK	LPC clock output	O CMOS	Bridge to Com Express Row connector	

Table 28 B706GT LPC

3.11.1 Reference schematic - PCOM-C701 ZR1

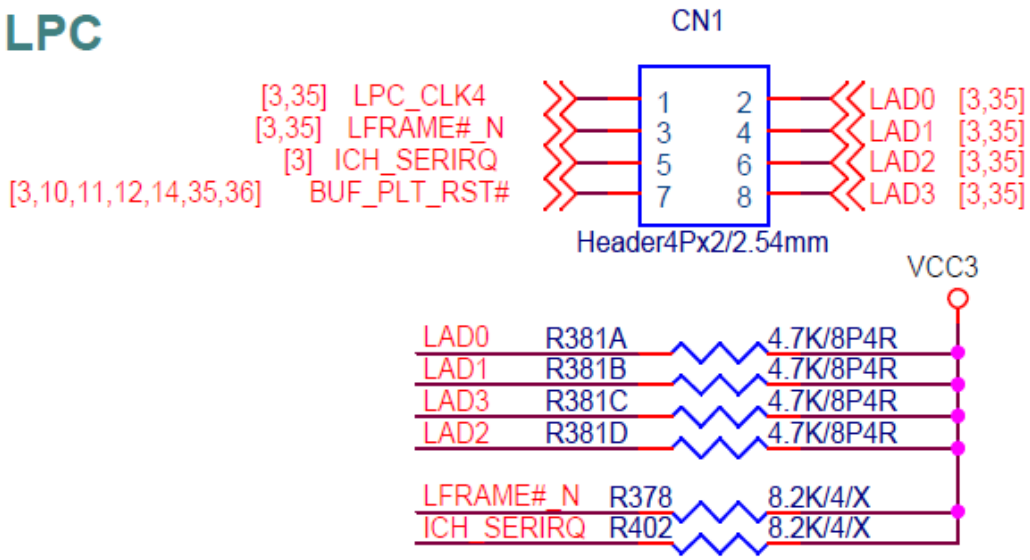


Figure 13 Reference schematic –LPC

3.12 SPI

An external SPI BIOS is designed on the Carrier board, which allows the Module boot from the Carrier SPI BIOS. To achieve this function, the BIOS_DIS0# and BIOS_DIS1# must be designed as a selectable method on the Carrier.

PCOM-B706GT SPI

Pin#	Pin Name	Description	Pin Typ	B706GT Module	Pwr Rail /Tolerance(Volt)
A34	BIOS_DIS0#	Selection strap to determine the BIOS boot device. The Carrier should only float these or pull them low	I CMOS	PU 10k ohm to +3V_Dual	NA
B88	BIOS_DIS1#				
A91	SPI_POWER	Power supply for Carrier Board SPI – sourced from Module – nominally 3.3V. The Module shall provide a minimum of 100mA on SPI_POWER	O	+3V_Dual	3.3V Suspend/ 3.3V
A92	SPI_MISO	Data in to Module from Carrier SPI	I CMOS	Level Translator to Com Express Row connector	
A95	SPI_MOSI	Data out from Module to Carrier SPI	O CMOS		
A94	SPI_CLK	Clock from Module to Carrier SPI			
B97	SPI_CS#	-	O CMOS		

Table 29 PCOM-B706GT SPI

3.12.1 Reference schematic - PCOM-C701-BMC ZR3

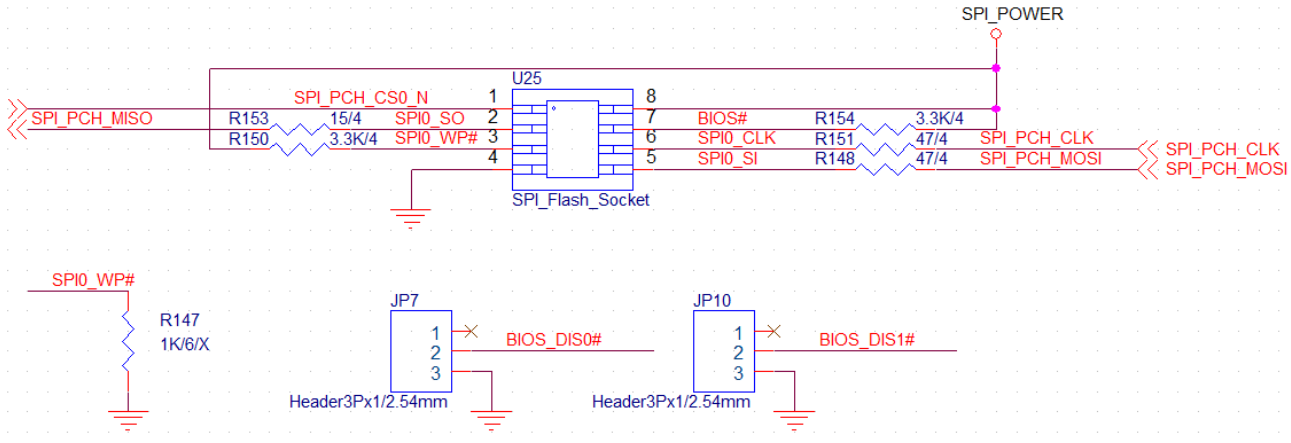


Figure 14 Reference schematic –SPI

4 Power

PCOM-B706GT is designed for both AT and ATX power mode, which depends on the power mode design on carrier board. The following ATX and AT mode power sequences are provided for the carrier design guideline.

4.1 Power sequence

The AT power sequence is based on PCOM-B706GT with evaluation carrier PCOM-C701-BMC-ZR3

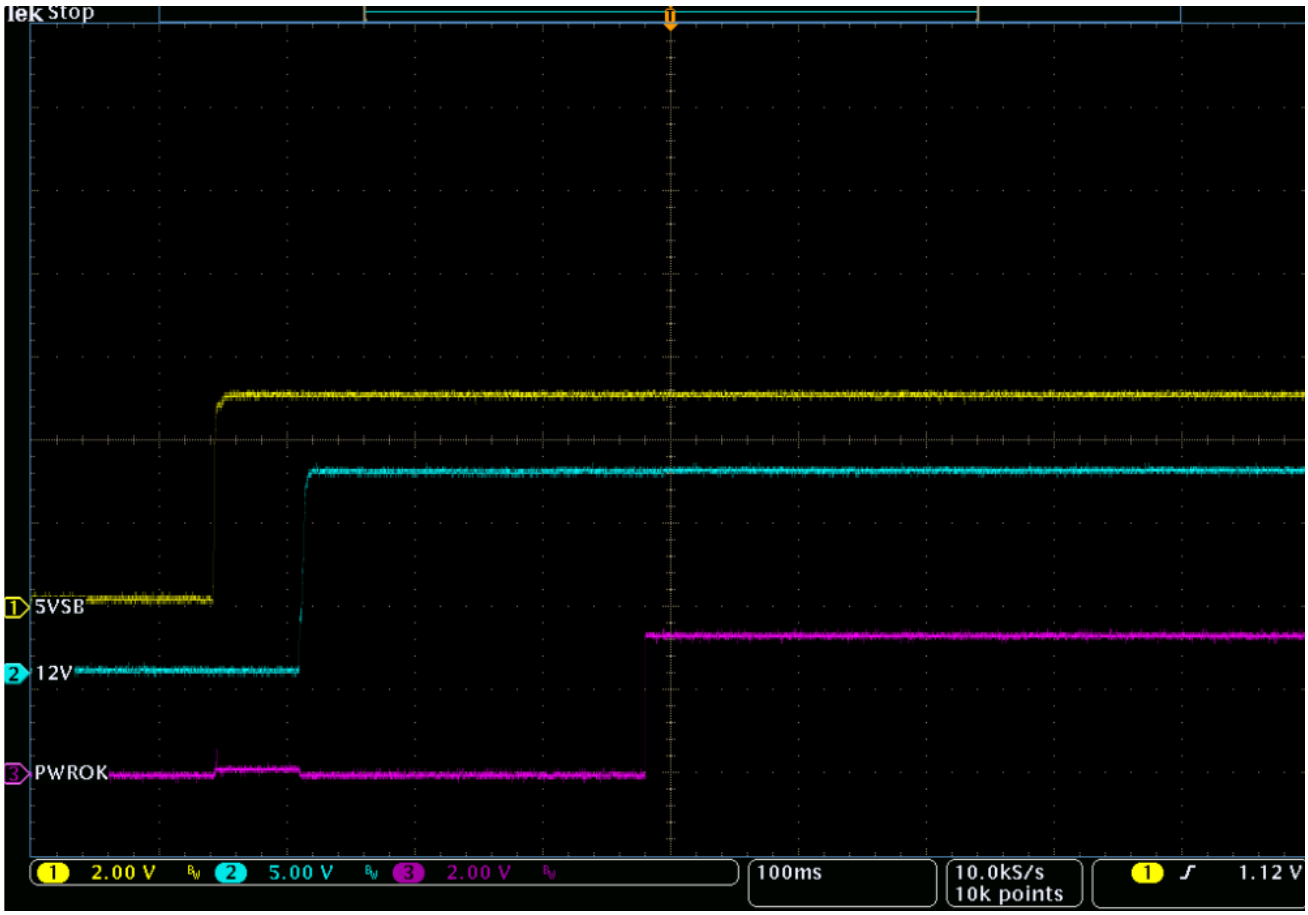


Figure 15 Power Sequence under AT Mode

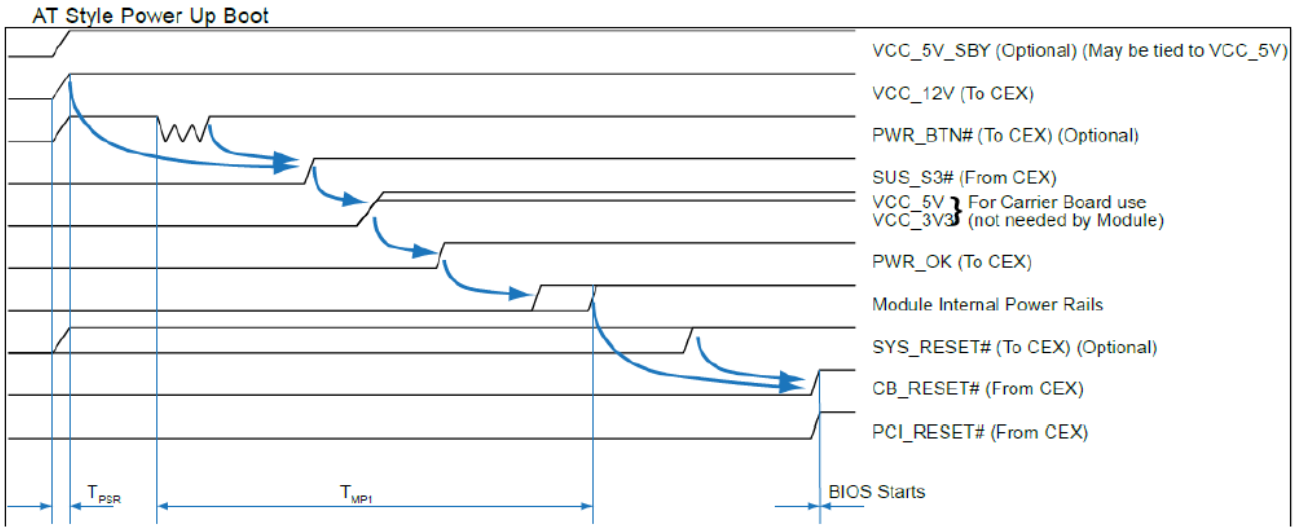


Figure 16 Carrier Power Sequence under AT Mode

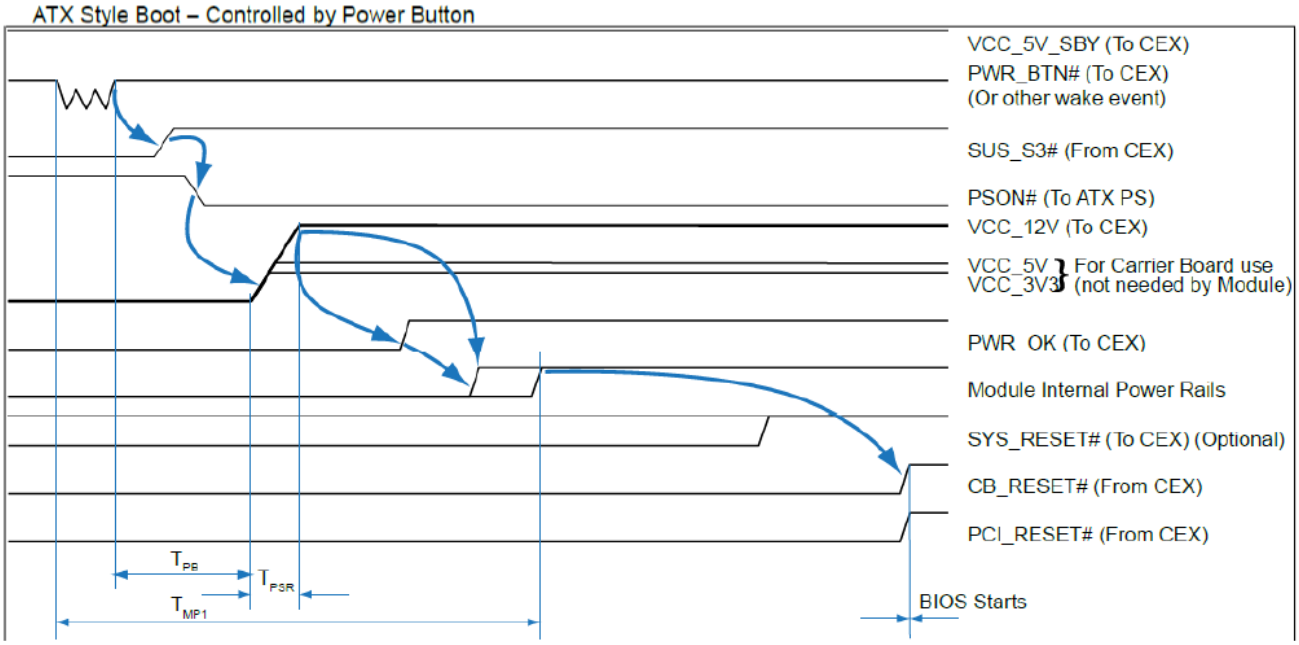


Figure 17 Carrier Power Sequence under ATX Mode

5 Mechanical

5.1 PCOM-B706GT Dimension

PCOM-B706GT top side view dimension

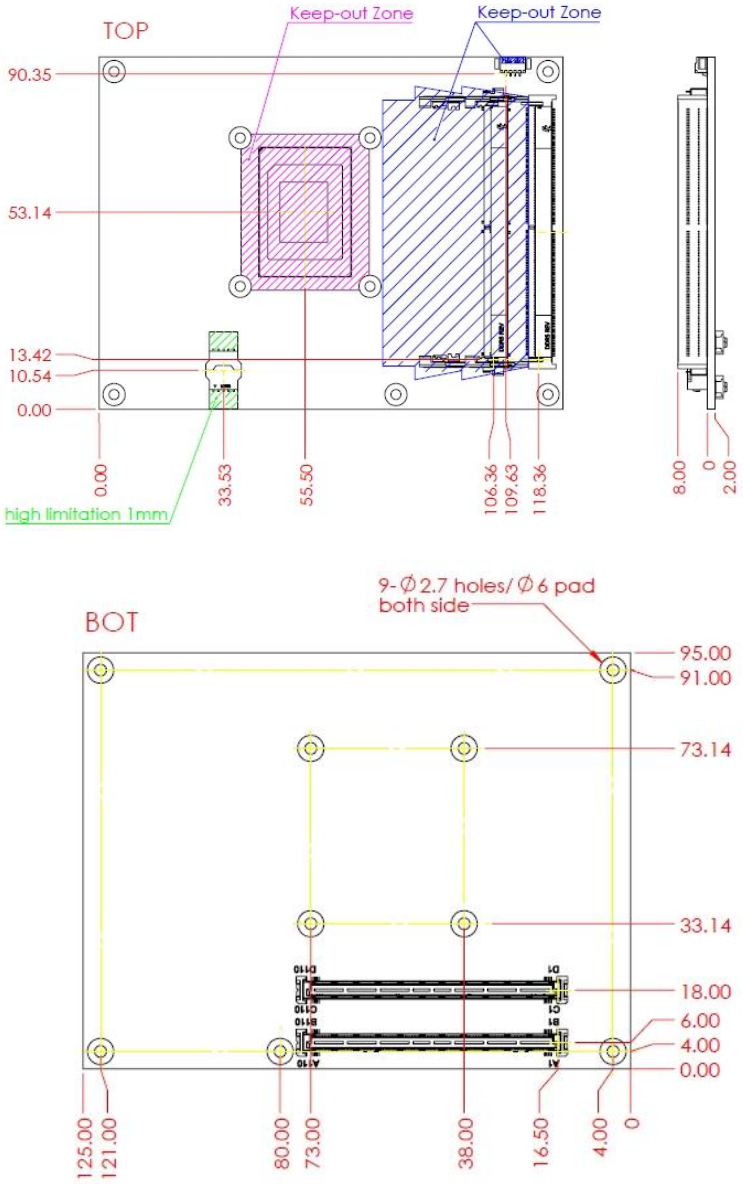


Figure 18 PCOM-B706GT Dimension – TOP & Bottom

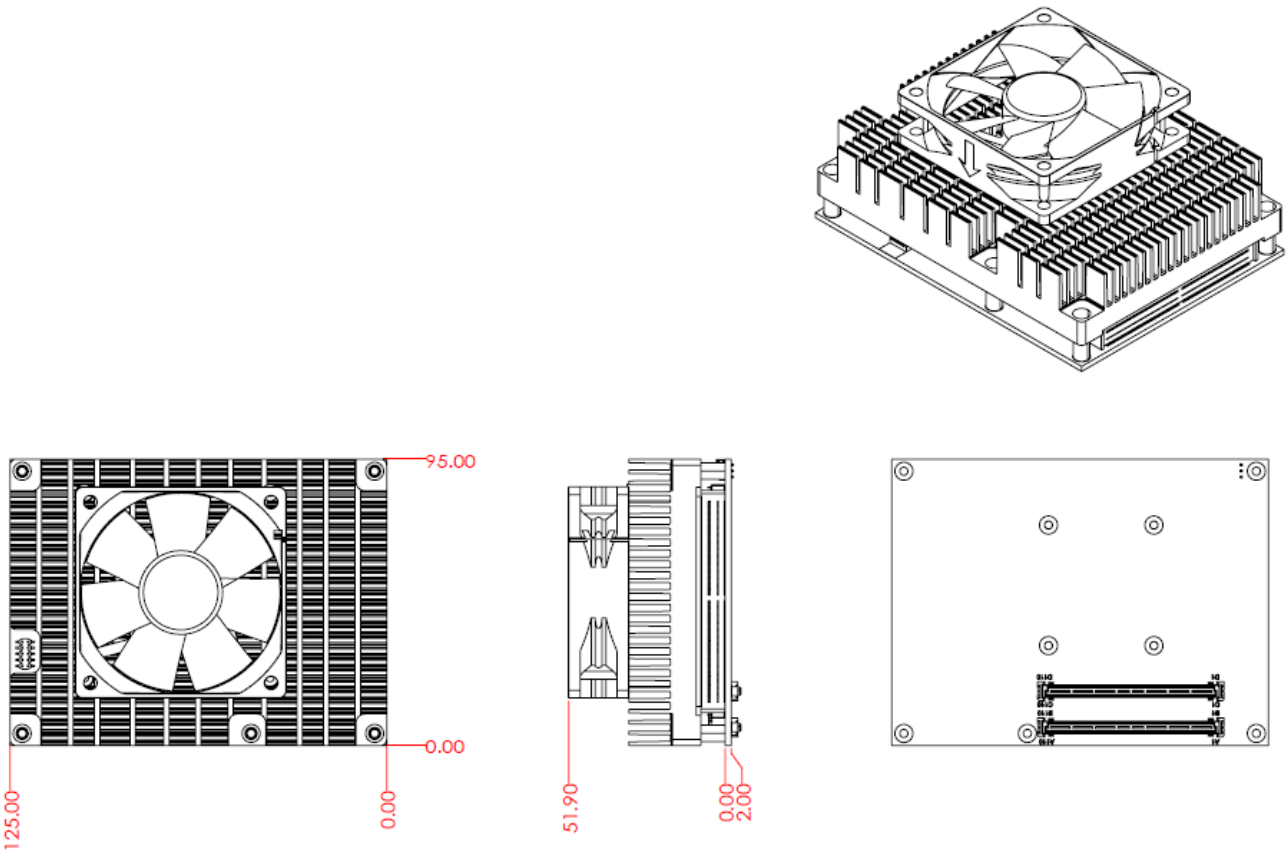


Figure 19 PCOM-B706GT side view dimension, along with a heat sink / cooler.

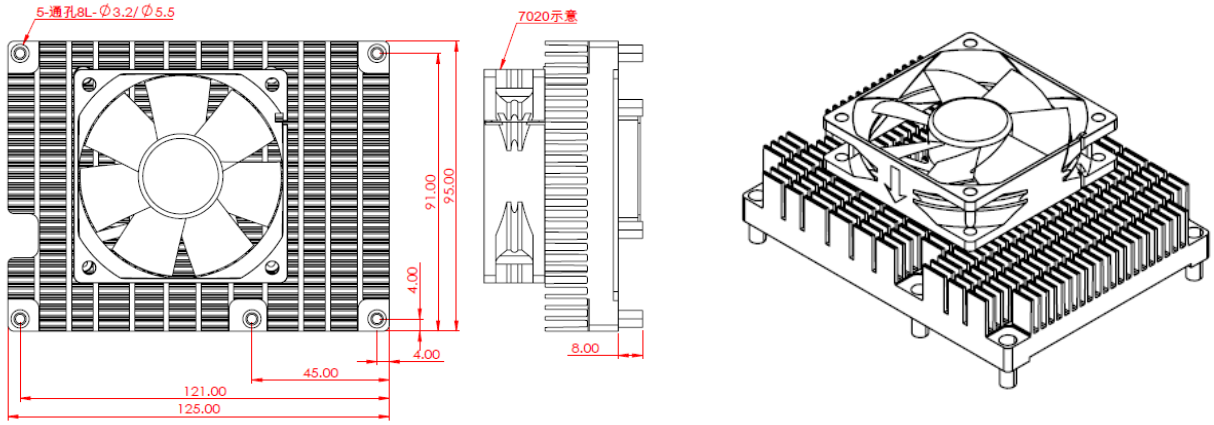


Figure 20 PCOM-B706GT Dimension - Side view

6 COM Express Module and Carrier protection design

6.1 Module protection

PCOM-B706GT Type 7, Schottky diode protection has been design on the COM Express module for Serial Port, FAN(PWMOUT & TACHIN), LID and SLEEP. Please refer to Fig.21 Module circuit protection schematic.

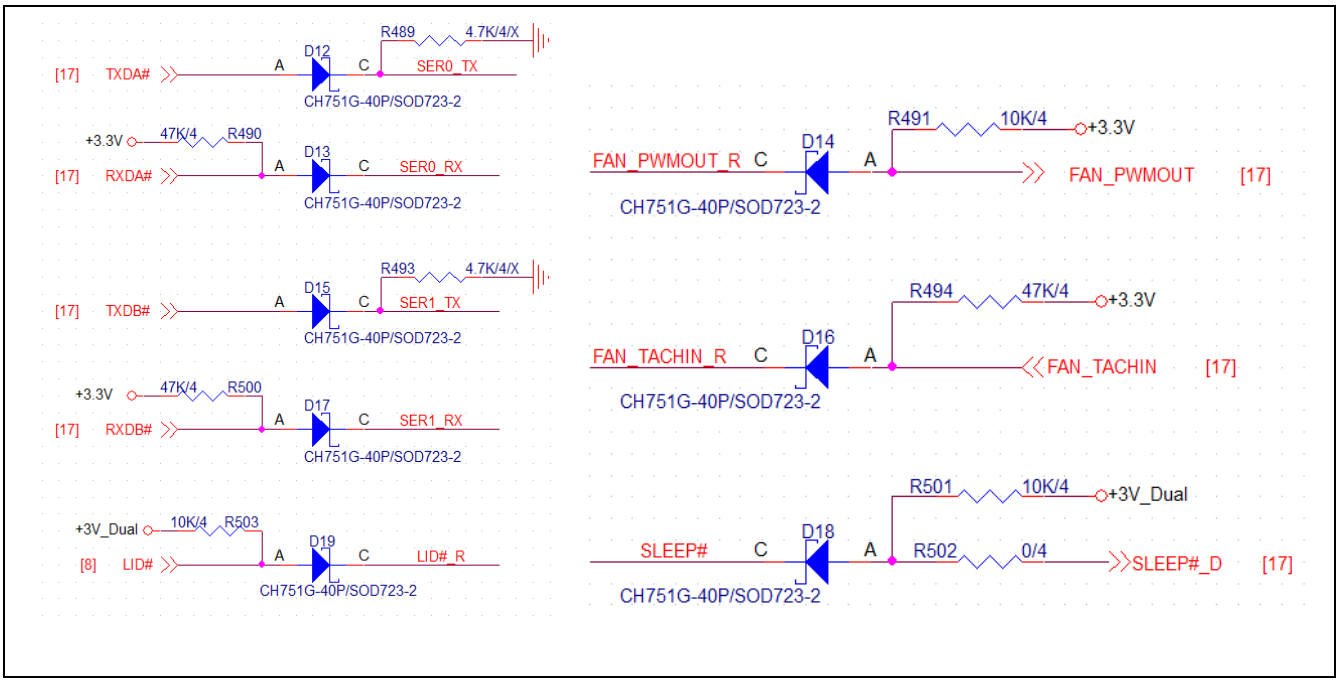


Figure 21 Circuit protection on Module

6.2 Carrier protection

Avoiding Carrier accidentally exposure to VCC_12V pool, a circuit protection design should be implemented on the Carrier, please refer to Fig.22 Carrier circuit protection schematic.

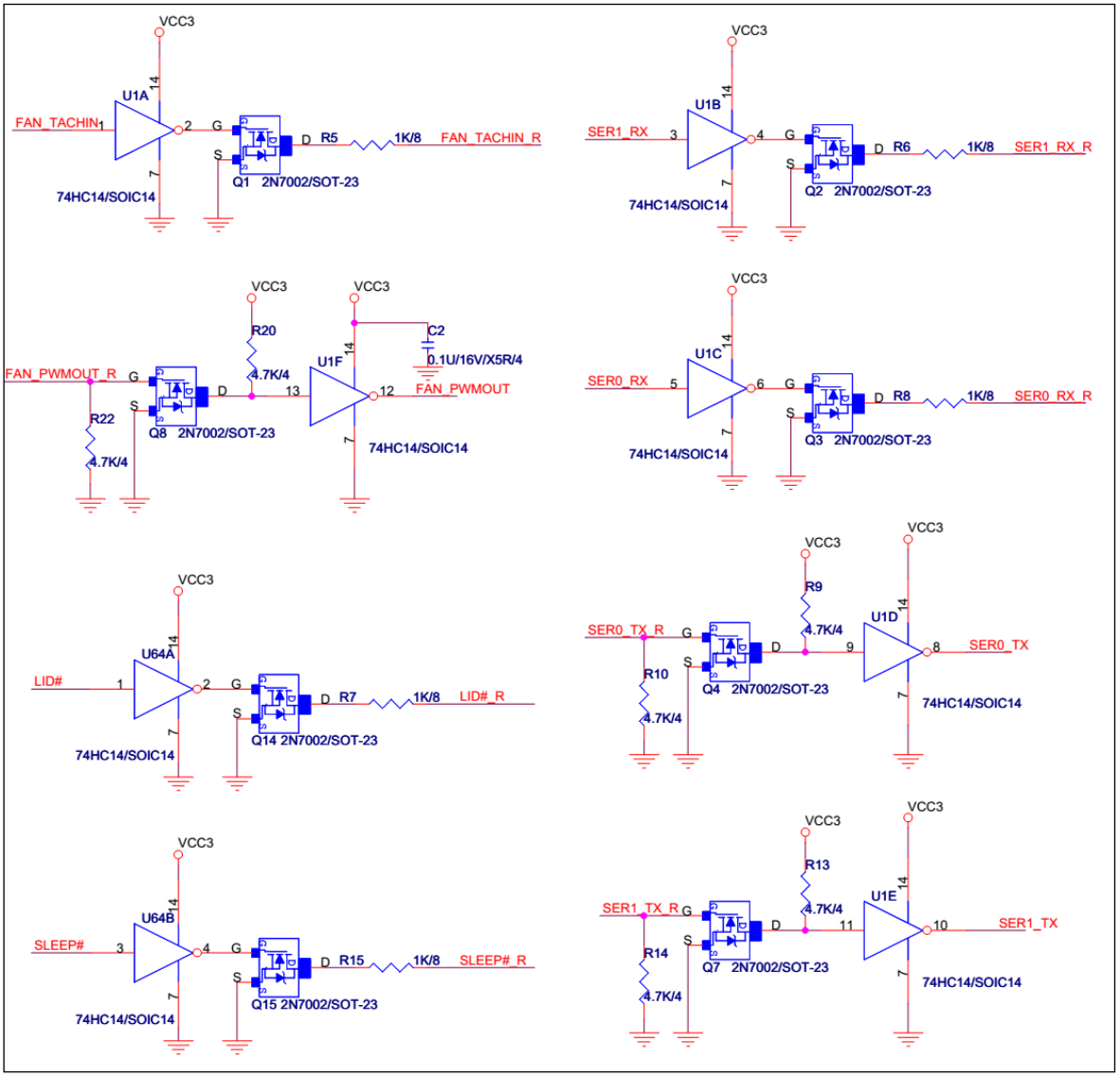


Figure 22 Circuit protection on Carrier

7 Industry Specifications

Low Pin Count Interface Specification, Revision 1.0 (LPC)
http://www.intel.com/design/chipsets/industry/lpc.htm
Universal Serial Bus (USB) Specification, Revision 2.0 http://www.usb.org/home
PCI Specification, Revision 2.3 https://www.pcisig.com/specifications
Serial ATA Specification, Revision 3.0 http://www.serialata.org/
PCI Express Base Specification, Revision 2.0 https://www.pcisig.com/specifications
PICMG® COM Express Module™ Base Specification http://www.picmg.org/
PICMG®COM Express Carrier Board Design Guide http://www.picmg.org/