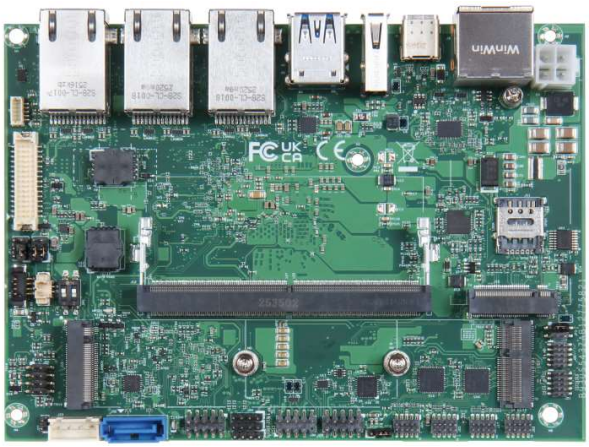
Portwell



PEB-2775 Series

3.5” Embedded Board

User Manual

Version R 1.1

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Revision History

R 1.0	Official Release Rev. 1.0
R 1.1	Update with OOB functions

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Chapter 1

System Overview

1 Introduction

1. Introduction

The PEB-2775 is a new standard product for 3.5” product line, based on Intel Twin Lake platform.
Twin Lake is a pin-to-pin backward compatible platform with Alder Lake-N and Amston Lake. PEB-2775 feature in Intel® Twin Lake and Amston Lake processors, including Intel® Processor N150/N355 and Atom® x7433RE. It delivers a sku of 15W, contains 8 cores and 32 EU counts in SoC.

The PEB-2775 supports one DDR5 SO-DIMM socket (up to 16GB), one M.2 E-Key (2230) for PCIe/USB devices, one M.2 M-Key (2280) for PCIe/SATA storage, and one M.2 B-Key (3042/3052) for wireless modules. It supports triple independent displays via HDMI 2.0, Type-C and LVDS.
I/O-rich and robust, the board offers dual Intel® 2.5GbE LAN, one 1GbE LAN(support OOB function), dual USB 3.2 Gen2 ports, one USB2.0 port, dual USB 2.0 headers, 2* RS-232/422/485, 4* RS-232, audio I/O, GPIO, I2C, SMBus, and onboard TPM 2.0. Its wide operating temperature range (up to -40° C to 85° C for industrial SKUs) and 9~36V DC input ensure reliability in harsh environments.
Whether used in some kind of application request for low power, high performance solution to process high resolution image for digital signage, factory inspecting machine, surveillance system and Edge AI.

Chapter 2

System Overview

2 Specifications
2.1 Supported Operating Systems
2.2 Mechanical Dimensions
2.3 Power Consumption
2.4 Environmental Specifications

2. Specifications

Main Processor	◆ Intel® Processor N150 ◆ Intel® Processor N355 ◆ Intel® Atom x7433RE
System BIOS	◆ AMI UEFI BIOS
Main Memory	◆ 1x non-ECC DDR5 4800MT/s SO-DIMM up to 16GB ◆ 1DPC, 1-channel
Graphics	◆ Intel® Graphics Gen12 with up to 24 EUs ◆ HDMI: 2x HDMI port on rear I/O (HDMI 2.0, 3840x2160 @ 60Hz) ◆ Type-C: 1x Type-C port on rear I/O (Type-C, 3840x2160 @ 60Hz) ◆ LVDS: 1x LVDS on board connector (Dual channel, 24bit, 1920x1200 @60Hz)
Expansion Interface	◆ 1x M.2 E key 2230 ◆ 1x M.2 B key 3042/3052 (3042 need additional bracket) ◆ 1x M.2 M key 2280
Storage Interface	◆ 1x SATA port
Input/Output	◆ Serial Port: 2x RS-232/422/485, 4x RS/232 on board pin header ◆ USB port: 3x USB 3.2 Gen2(1x Typc-C, 2x Type A/1x USB2.0 on rear I/O(Type A), 2x USB 2.0 on board pin header ◆ Audio Interface: line-in, line-out, mic-in on board pin header ◆ 1x SMbus & 1x I2C on board pin header ◆ 1x 4-pin smart fan header
Ethernet	◆ 1x Intel® GbE Controller(I210) ◆ 2x Intel® 2.5GbE Controller(I226)
OOB Function	◆ Remote Power ON/OFF/RESET ◆ Serial Over LAN ◆ Health/Sensor/SEL ◆ BIOS recovery
High Drive GPIO	◆ 1x pin-header for GPIO(8bit)
Mechanical and environmental specifications	◆ Operating temperature: 0 ~ 60° C (Twin Lake)/ -40 to +85° C (Amston Lake) ◆ Storage temperature: -40 ~ 85° C ◆ Humidity: 5 ~ 95% non-condensing

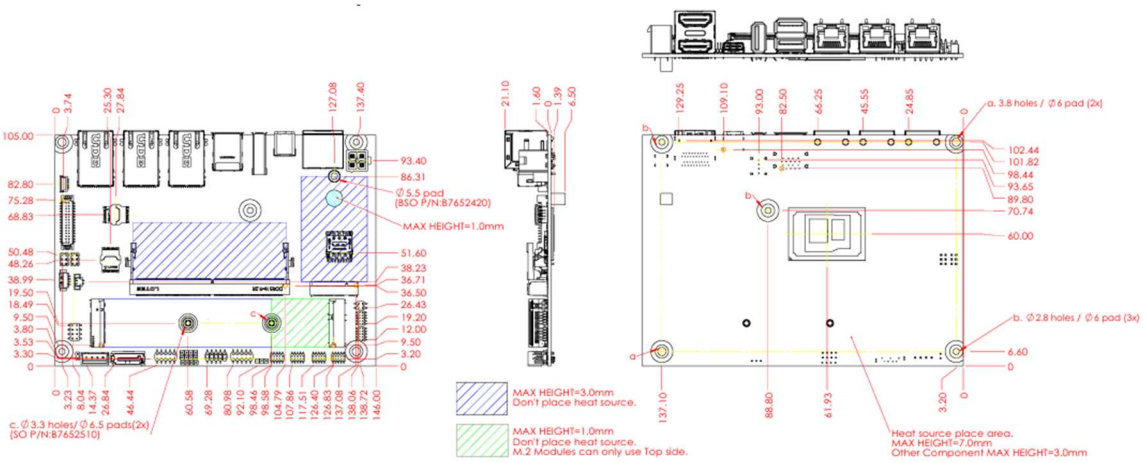
	◆ Power supply voltage: 9 ~36V 1x ATX/AT 4-pin connector on board ◆ Board size: 146mm x 102 mm (5.7" x 4")
Certification	◆ CE/FCC

2.1 Supported Operating Systems

The PEB-2775 supports the following operating systems.

	Windows IoT Enterprise	Ubuntu
Twin Lake	Windows 11 LTSC (24H2)	24.04
Amston Lake	Windows 10 LTSC (21H2) Windows 11 LTSC (24H2)	22.04/24.04

2.2 Mechanical Dimensions



2.3 Power Consumption

Test Configuration	
CPU Type	Intel® Atom™ x7433RE@1.50GHz,L3:6MBytes
SBC BIOS	Portwell, Inc. PEB-2775 BIOS Rev.: 0.0.7 (10312025)
Memory	Innodisk 32GB DDR5 4800 SODIMM (K4RAH08 6VBBCQK)
Graphic Card	Intel® UHD Graphics
Graphic Driver	Intel® UHD Graphics, Version: 32.0.101.6314
LAN Card	Intel®I210 Gigabit Network Connection
LAN Driver	Intel®I210 Gigabit Network Connection, version: 14.1.22.0

LAN Card	Intel® Ethernet Controller I226-LM
LAN Driver	Intel® Ethernet Controller I226-LM, version: 2.1.4.3
LAN Card	Intel® Ethernet Controller I226-LM#2
LAN Driver	Intel® Ethernet Controller I226-LM#2, version: 2.1.4.3
Audio Card	High Definition Audio Device
Audio Driver	High Definition Audio Device, version:10.0.26100.1150
Chip Driver	Intel® Chipset Device Software, Version: 10.1.19899.8597
USB 3.0 Driver	Intel® USB 3.20 eXtensible Host Controller – 1.20 (Microsoft), Version: 10.0.26100.1591
EC Version	0.4 (10/29/2025)
OS Edition	Windows 11 Pro (24H2)
Hard Drive	T253X2512G0C101
Power Supply	SSA-0651-1
Boot Mode Select	UEFI

Power consumption(12V)

Install Test AP PassMark BurnInTest V10

Run Full loading 10mins and Measurement current

BurnInTest Loading: 2D, 3D, CPU, Memory, Disk*1(include OS), USB*3, network*3, Serial*6

BurnInTest duty cycle setting: 3D 95%, other 100%

Item	*Power ON*	*Full Loading 10mins*
DC in (+12V)	1.27A	1.72A
Device (+12V)	0.03A	0.03A

Device (+5V)	0.12A	0.14A

Power consumption(9V)		
Adjust the PSU 9V of 5% Install Test AP PassMark BurnInTest V10 Run Full loading 10mins and Measurement current BurnInTest Loading: 2D, 3D, CPU, Memory, Disk*1(include OS), USB*3, network*3, Serial*6 BurnInTest duty cycle setting: 3D 95%, other 100%		
Item	*Power ON*	*Full Loading 10mins*
DC in (+8.55V)	2.17A	2.76A

2.4 Environmental Specifications

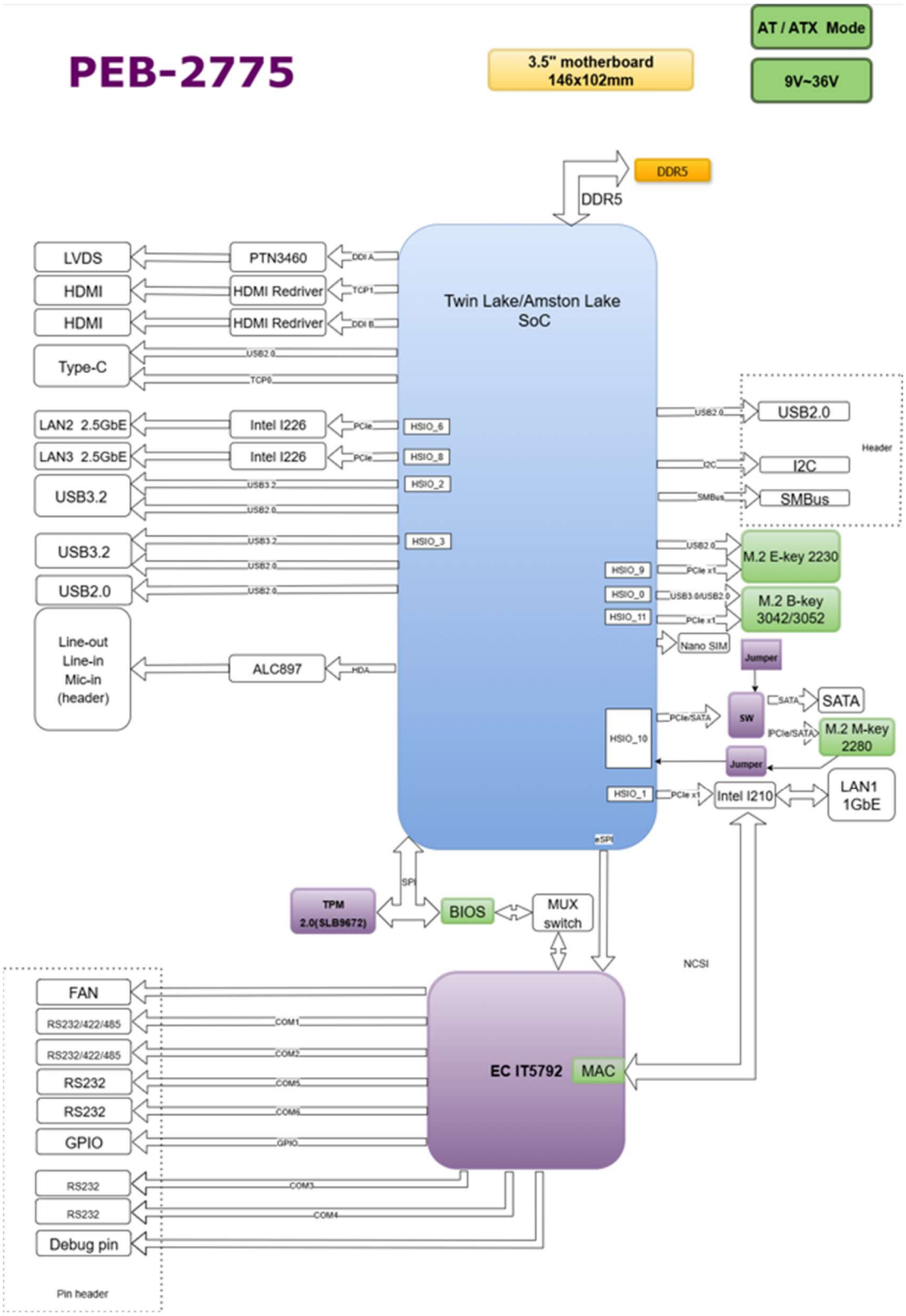
Storage Temperature : 0 ~ 60° C (Twin Lake)/ -40 to +85° C (Amston Lake)
Operation Temperature : 0~60° C
Storage Humidity : 5~95%, non-condensing
Operation Humidity: 5~95%, non-condensing

Chapter 3

System Overview

3 Block Diagram

3. Block Diagram



Chapter 4

System Overview

4 Hardware Configuration
4.1 Drawing Overview
4.2 Jumper Setting List
4.3 Connector Function List

4. Hardware Configuration

This chapter indicates jumpers、 headers, and connectors' locations. Users may find useful information related to hardware settings in this chapter.

4.1 Drawing Overview

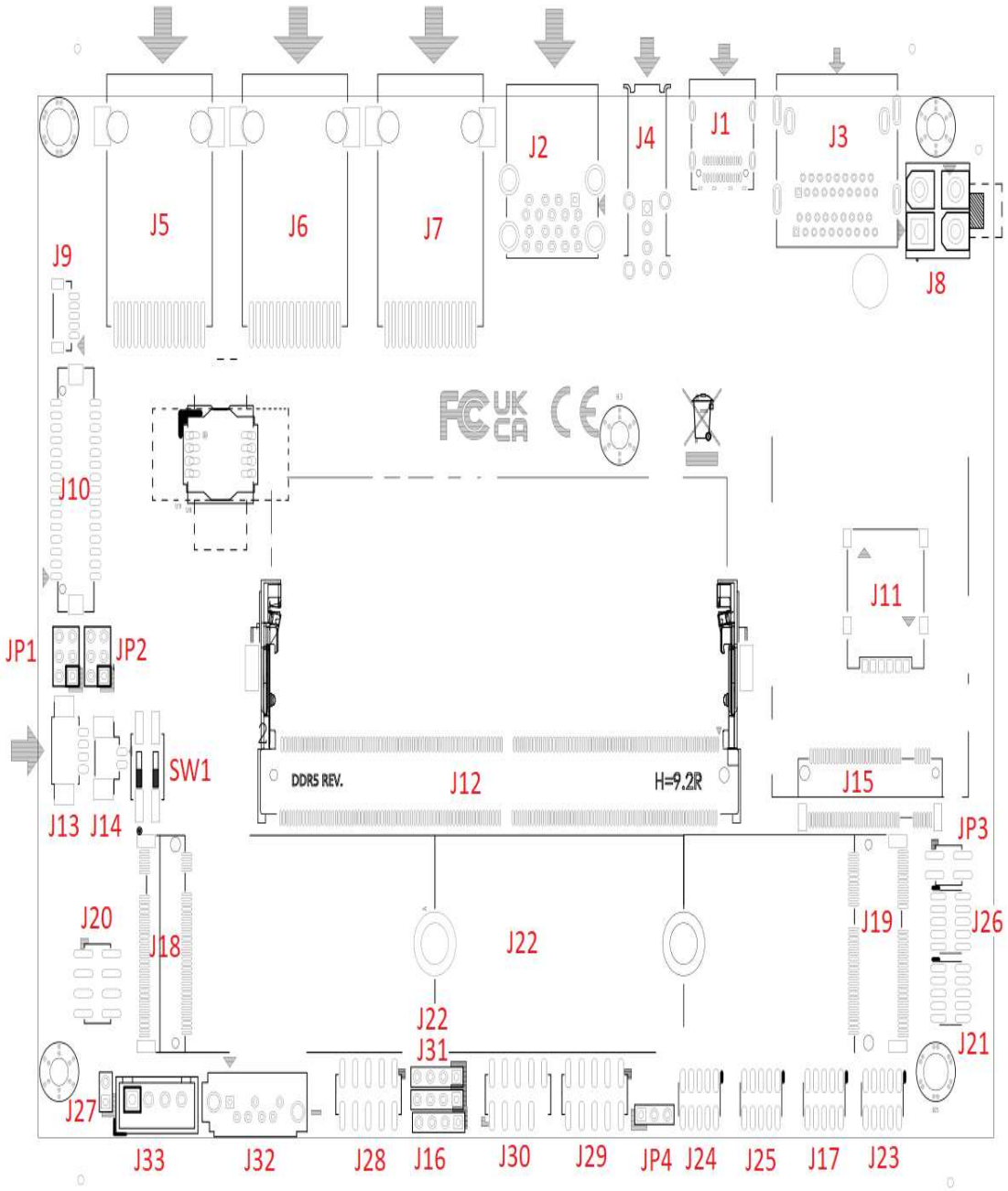


Figure1. PEB-2775 Top View

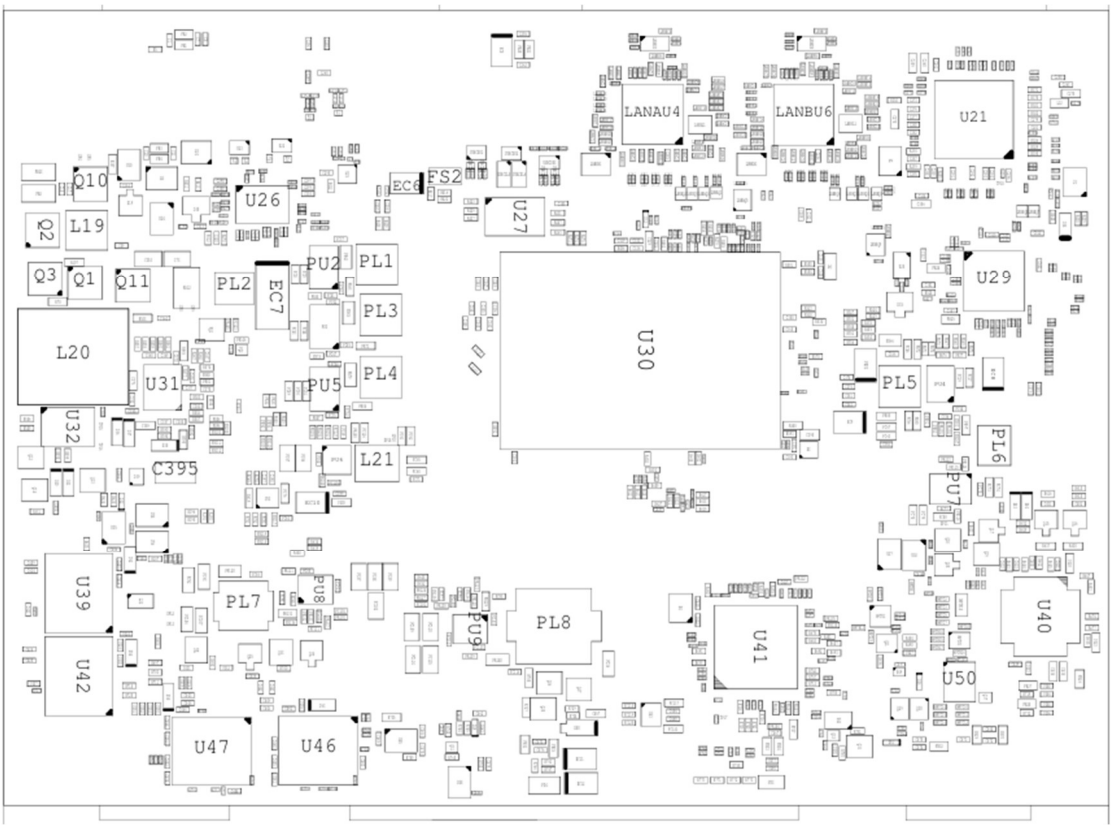


Figure1. PEB-2775 Bot View

4.2 Jumper Setting List

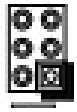
For users to customize PEB-2775 features. In the following sections, Short means covering a jumper cap over jumper pins; Open or N/C (Not Connected) means removing a jumper cap from jumper pins. Users can refer to Figure 1 for the Jumper allocations.

Jump Function List:

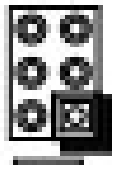
Location	Function
JP1	LVDS Power select
JP2	LVDS Backlight EN Power select
JP3	4G/ 5G select
JP4	ATX/AT mode select

SW1	M2 PCIe/SATA & External SATA Switch

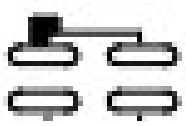
JP1 : LVDS Power select

PCB Footprint	MODE	Jumper Setting
	1-3	3.3V_Default
	3-4	12V
	3-5	5V

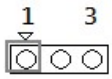
JP2 : LVDS Backlight EN Power select

PCB Footprint	MODE	Jumper Setting
	1-3, 2-4	5V, Active High_Default
	1-3, 4-6	12V, Active High
	3-5,2-4	5V, Active Low
	3-5,4-6	12V, Active Low

JP3 : 4G/5G Select

PCB Footprint	MODE	Jumper Setting
	1-2, 3-4	NC
	3-4	Thales 5G Pinout
	1-2	Sierra 4G Pinout_Default
	NC	Sierra 5G Pinout

JP4: ATX/AT model Select

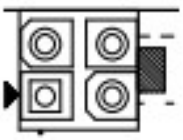
PCB Footprint	MODE	Jumper Setting
	1-2	AT model
	2-3	ATX model Default

4.3 Connector Function List

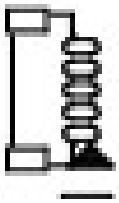
Connector	Function
J1	USB3.1 TYPE-C Connector
J2	USB3.1 TYPE-A Connector
J3	HDMI2.0 Connector
J4	USB2.0 TYPE-A Connector
J5	RJ45 Connector/ 1G
J6	RJ45 Connector/ 2.5G
J7	RJ45 Connector/ 2.5G
J8	ATX 4pin +12V Power Connector
J9	LVDS BackLight control Connector
J10	LVDS Connector
J11	Nano SIM Socket
J12	DDR5 SODIMM Socket
J13	CPU Fan Connector
J14	RTC Battery Connector
J15	M.2 Connector/B Key
J16	EC Debug header(I2C)
J17	COM3/RS232 Header
J18	M.2 Connector/M Key

J19	M.2 Connector/E Key
J20	Audio Header
J21	COM5/RS232 Header
J22	I2C Header
J23	COM4/RS232 Header
J24	COM1/RS232/422/485 Header
J25	COM2/RS232/422/485 Header
J26	COM6/RS232 Header
J27	Buzzer Header
J28	GPIO Header
J29	Front panel Header
J30	USB2.0 Header
J31	SMBus Header
J32	SATA Connector
J33	SATA Power Connector

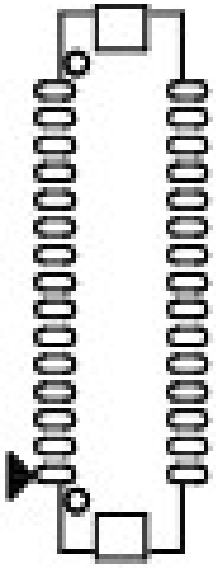
J8 : 4-PIN ATX Power(Support DC 9~36V)

PCB Footprint	Pin No.	Signal Description
	1	GND
	2	GND
	3	DC-IN(9~36V)
	4	DC-IN(9~36V)

J9 : LVDS Backlight Control

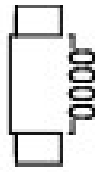
PCB Footprint	Pin No.	Signal Description
	1	VCC5
	2	CTRL
	3	VCC12
	4	GND
	5	ENABLE

J10 : LVDS

PCB Footprint	Pin No.	Signal Description	Pin No.	Signal Description
	1	LVDS_CON	2	LVDS_CON
	3	LVDS_CHA_TX_P_0	4	LVDS_CHA_TX_N_0
	5	LVDS_CHA_TX_P_1	6	LVDS_CHA_TX_N_1
	7	LVDS_CHA_TX_P_2	8	LVDS_CHA_TX_N_2
	9	LVDS_CHA_TX_P_3	10	LVDS_CHA_TX_N_3
	11	LVDS_CHA_CLK_P	12	LVDS_CHA_CLK_N
	13	LVDS_DDC_CLK	14	LVDS_DDC_DATA
	15	GND	16	GND
	17	LVDS_CHB_TX_P_0	18	LVDS_CHB_TX_N_0
	19	LVDS_CHB_TX_P_1	20	LVDS_CHB_TX_N_1
	21	LVDS_CHB_TX_P_2	22	LVDS_CHB_TX_N_2
	23	LVDS_CHB_TX_P_3	24	LVDS_CHB_TX_N_3
	25	LVDS_CHB_CLK_P	26	LVDS_CHB_CLK_N

PCB Footprint	Pin No.	Signal Description	Pin No.	Signal Description
	27	NC	28	NC
	29	GND	30	GND
	CG1	GND	CG2	GND

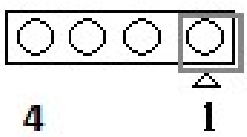
J13 : CPU Smart Fan

PCB Footprint	Pin No.	Signal Description
	1	GND
	2	VCC12
	3	FAN_TACHIN
	4	FAN_PWMOUT

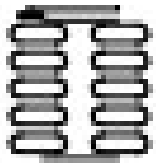
J14: RTC battery

PCB Footprint	Pin No.	Signal Description
	1	BAT3V
	2	GND

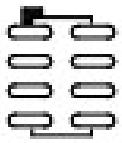
J16 : EC Debug header(I2C)

PCB Footprint	Pin No.	Signal Description
	1	3VSB
	2	CLK
	3	DAT
	4	GND

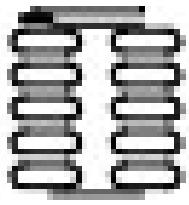
J17 : COM3 PORT(RS232)

PCB Footprint	Pin No.	Signal Description	Pin No.	Signal Description
	1	DCD#	2	RXD#
	3	TXD#	4	DTR#
	5	GND	6	DSR#
	7	RTS#	8	CTS#
	9	RI#	10	NC

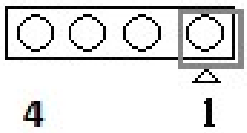
J20 : Audio

PCB Footprint	Pin No.	Signal Description	Pin No.	Signal Description
	1	MIC204	2	INPH_L
	3	AC-GND	4	INPH_R
	5	OPH_L	6	AC-GND
	7	OPH_R	8	MIC203

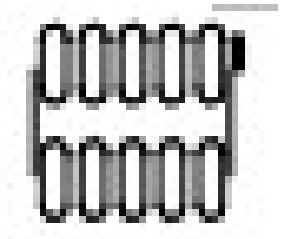
J21 : COM5 PORT(RS232)

PCB Footprint	Pin No.	Signal Description	Pin No.	Signal Description
	1	DCD#	2	RXD#
	3	TXD#	4	DTR#
	5	GND	6	DSR#
	7	RTS#	8	CTS#
	9	RI#	10	NC

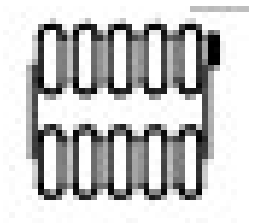
J22 : I2C

PCB Footprint	Pin No.	Signal Description
	1	3VSB
	2	SCL
	3	SDA
	4	GND

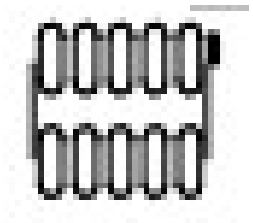
J23 : COM4 PORT(RS232)

PCB Footprint	Pin No.	Signal Description	Pin No.	Signal Description
	1	DCD#	2	RXD#
	3	TXD#	4	DTR#
	5	GND	6	DSR#
	7	RTS#	8	CTS#
	9	RI#	10	NC

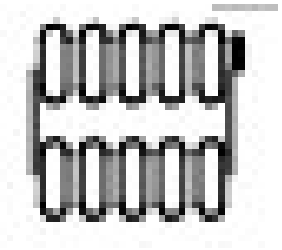
J24 : COM1 PORT(RS232/422/485)

PCB Footprint	Pin No.	Signal Description	Pin No.	Signal Description
	1	DCD#/DT-	2	RXD#/DT+
	3	TXD#/422R+	4	DTR#/422R-
	5	GND	6	DSR#
	7	RTS#	8	CTS#
	9	RI#	10	NC

J25 : COM2 PORT(RS232/422/485)

PCB Footprint	Pin No.	Signal Description	Pin No.	Signal Description
	1	DCD#/DT-	2	RXD#/DT+
	3	TXD#/422R+	4	DTR#/422R-
	5	GND	6	DSR#
	7	RTS#	8	CTS#
	9	RI#	10	NC

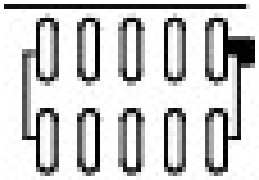
J26 : COM6 PORT(RS232)

PCB Footprint	Pin No.	Signal Description	Pin No.	Signal Description
	1	DCD#	2	RXD#
	3	TXD#	4	DTR#
	5	GND	6	DSR#
	7	RTS#	8	CTS#
	9	RI#	10	NC

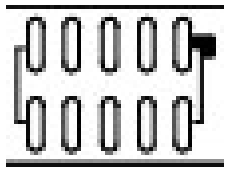
J27 : Buzzer

PCB Footprint	Pin No.	Signal Description
	1	VCC
	2	BUZZER

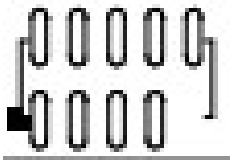
J28 : GPIO

PCB Footprint	Pin No.	Signal Description	Pin No.	Signal Description
	1	GPO0	2	GPI0
	3	GPO1	4	GPI1
	5	GPO2	6	GPI2
	7	GPO3	8	GPI3
	9	GND	10	VCC3

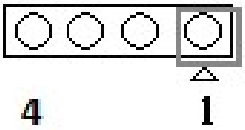
J29 : Front Panel

PCB Footprint	Pin No.	Signal Description	Pin No.	Signal Description
	1	GND	2	NC
	3	3VSB	4	SUS_LED#
	5	3VDUAL	6	SATA_LED_N#
	7	RSTBTN#	8	GND
	9	GND	10	PWRBTN#

J30 : USB 2.0

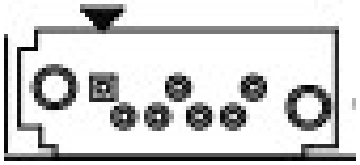
PCB Footprint	Pin No.	Signal Description	Pin No.	Signal Description
	1	VUSB	2	VUSB
	3	USB2_N_1	4	USB2_N_2
	5	USB2_P_1	6	USB2_P_2
	7	GND	8	GND
	9	NC	10	NC

J31 : SMBus

PCB Footprint	Pin No.	Signal Description
	1	3VSB
	2	CLK
	3	DATA

PCB Footprint	Pin No.	Signal Description
	4	GND

J32 : SATA

PCB Footprint	Pin No.	Signal Description
	1	GND
	2	SATA_TX+
	3	SATA_TX-
	4	GND
	5	SATA_RX-
	6	SATA_RX+
	7	GND

J33 : SATA Power

PCB Footprint	Pin No.	Signal Description
	1	VCC12
	2	GND
	3	GND
	4	VCC

Chapter 5

System Overview

5 Sample Code
5.1 Watch Dog Timer
5.2 GPIO Signal

5. Sample Code

5.1 Watch Dog Signal

```
#Define WDTCFG 0x06 // WDT Timer Coutrol Register
#Define WDTMIN 0x07 // WDT Timer Counter Register (Minute)
#Define WDTSEC 0x08 // WDT Timer Counter Register (Second)
#Define EC_IOPort 0xE300 // Default, reference to BIOS configuration

VOID Write_EC_SRAM(UINT8 Offset,UINT8 Value){
        IoWrite8(EC_IOPort+Offset,Value);
}
Byte Read_EC_SRAM(UINT8 Offset){
    IoRead8(EC_IOPort+offset,Value);
    return Value;
}
void WDT()
{
// Enable WDT 30sec
Write_EC_SRAM(WDTSEC,30);
Write_EC_SRAM(WDTCFG,0x01);    //Bit0: WDT Enable, BIT1: 0:Second Mode

// Enable WDT 5min
Write_EC_SRAM(WDTSEC,5);
Write_EC_SRAM(WDTCFG,0x03);     //Bit0: WDT Enable, BIT1: 1:Minute Mode

// Enable WDT 10min, 20sec
Write_EC_SRAM(WDTSEC,20);
Write_EC_SRAM(WDTSEC,10);
Write_EC_SRAM(WDTCFG,0x03);     //Bit0: WDT Enable, BIT1: 1:Minute Mode
}
```

5.2 GPIO Signal

```
#Define GPCR 0x2B      // GPIO Control Register, Bit7 = GPIO7, Bit6 = GPIO6, ...,
                       // 0: Output; 1: Input

#Define GPDR 0x2C      // GPIO Status Register, Bit7 = GPIO7, Bit6 = GPIO6, ...,
                       // 0: Low; 1: High

#Define EC_IOPort 0xE300      // Default, reference to BIOS configuration

VOID Write_EC_SRAM(UINT8 Offset,UINT8 Value){

IoWrite8(EC_IOPort+Offset,Value);
}

Byte Read_EC_SRAM(UINT8 Offset){
       IoRead8(EC_IOPort+offset,Value);
       return Value;
}

void GPIO()
{
   int Temp;
   // Set GPIO7 Input & get status
   Temp = Read_EC_SRAM(GPCR);
   Write_EC_SRAM(GPCR,Temp|0x80);      //Bit7: GPIO7 control, 0: Output 1: Input
   Temp = Read_EC_SRAM(GPDR);    //Bit7: GPIO7 status, 0: Output 1: Input

// Set GPIO7 Output & High
Temp = Read_EC_SRAM(GPCR);
Write_EC_SRAM(GPCR,Temp&0x7F);      //Bit7: GPIO7 control, 0: Output 1: Input
Temp = Read_EC_SRAM(GPDR);
Write_EC_SRAM(GPDR,Temp|0x80);      //Bit7: GPIO7 status, 0: Low 1: High
}
```

Chapter 6

System Overview

6 BIOS Setup
6.1 Entering Setup-Launch System Setup
6.2 Main
6.3 Configuration
6.4 Security
6.5 Boot
6.6 Save & Exit

6. BIOS Setup information

PEB-2775 is equipped with the AMI BIOS stored in Flash ROM. The following section describes the BIOS setup program. The BIOS setup program can be used to view and change the BIOS settings for the module. Only experienced users should change the default BIOS settings.

6.1 Entering Setup

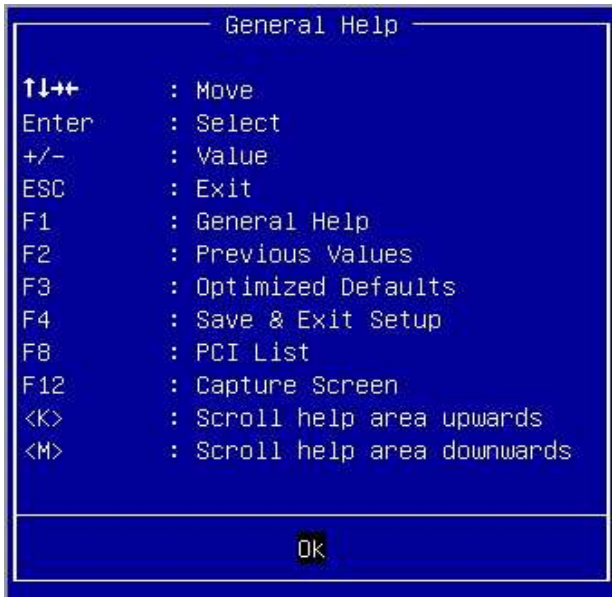
Power on the computer and the system will start POST (Power on Self-Test) Process. When the message below appears on the screen, press<Del> key will enter BIOS setup screen.

Press <Del> to enter SETUP

If the message disappears before responding and still wishes to enter Setup, please restart the system by turning it OFF and On or pressing the RESET button. It can be also restarted by pressing <Ctrl>, <Alt>, and <Delete> keys on keyboard simultaneously.

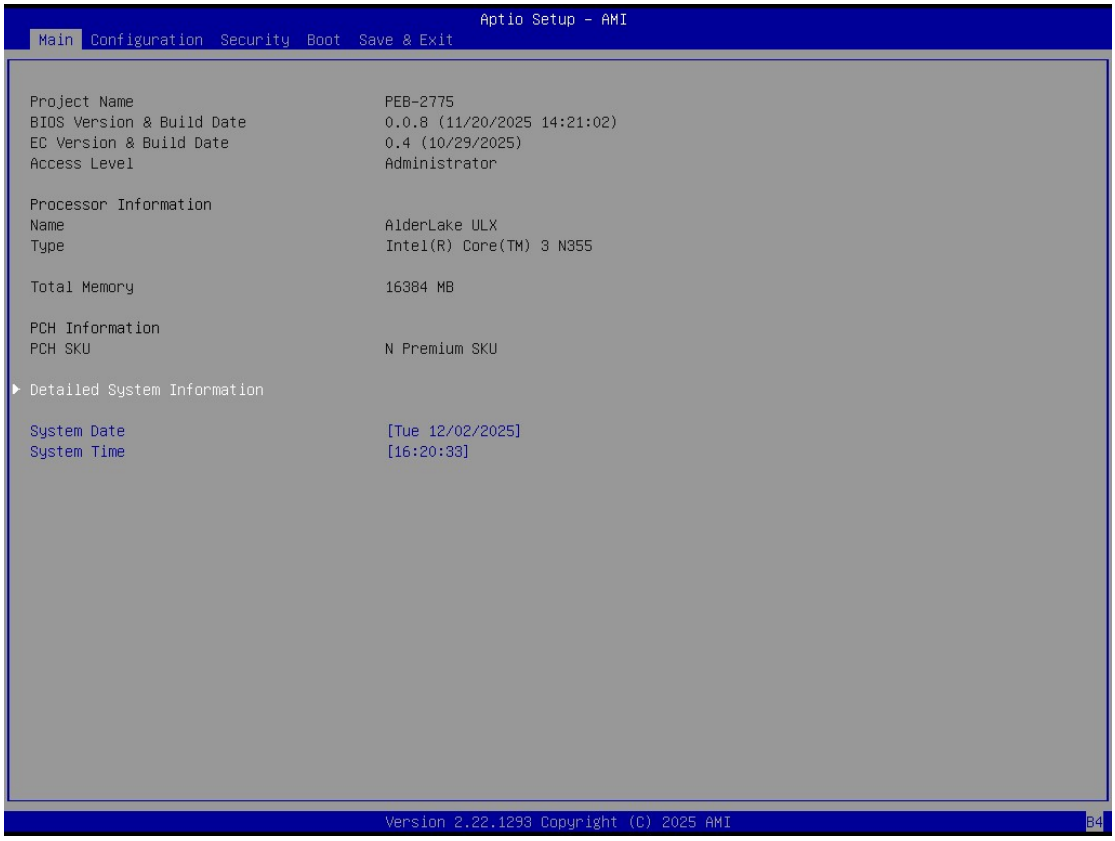
Press <F1> to Run General Help or Resume

The BIOS setup program provides a General Help screen. The menu can be easily called up from any menu by pressing <F1>. The Help screen lists all the possible keys to use and the selections for the highlighted item. Press <Esc> to exit the Help Screen.



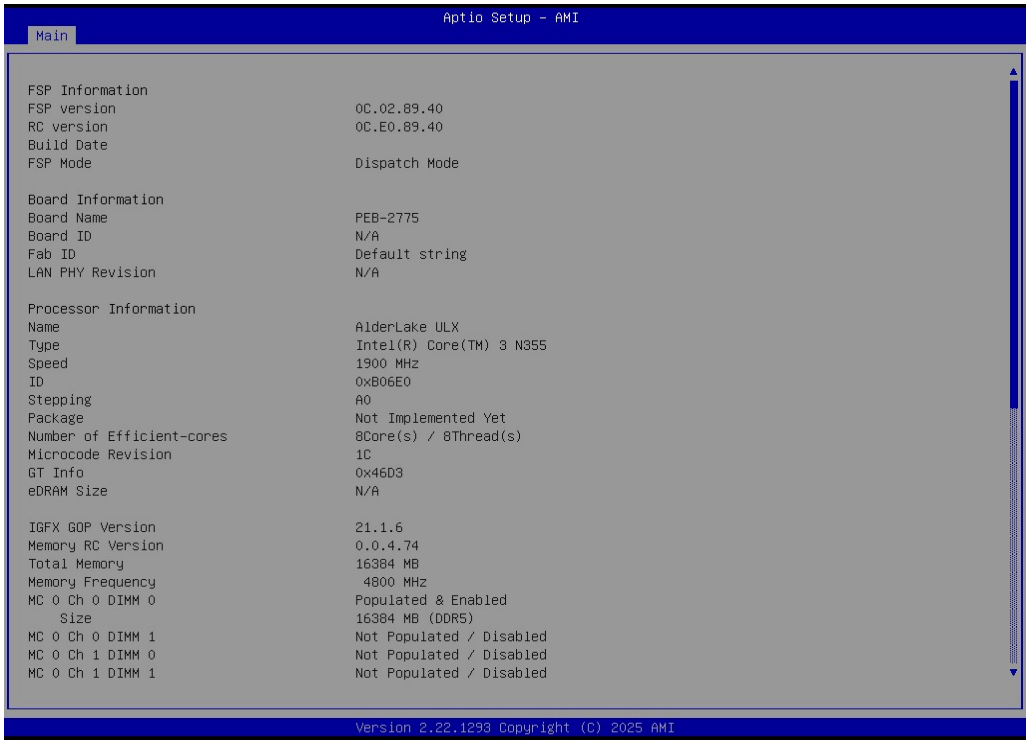
6.2 Main

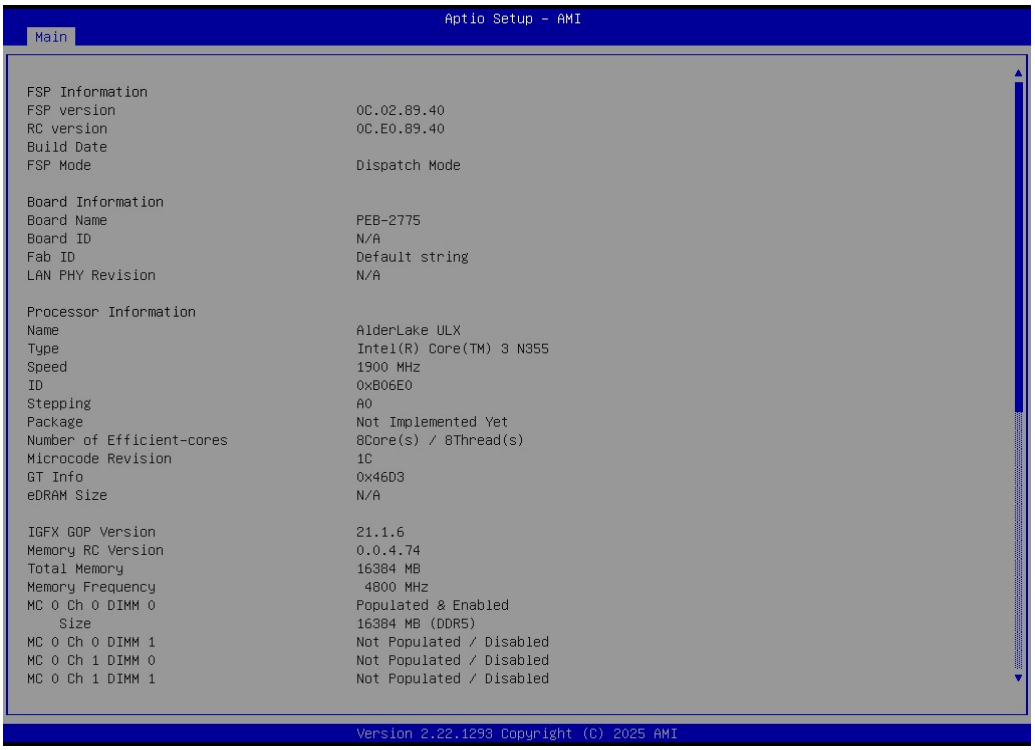
Use this menu for basic system configurations, such as time, date etc.



Feature	Description	Options
System Date	The date format is <Day>, <Month><Date><Year>. Use [+] or [−] to configure system Date.	
System Time	The time format is <Hour><Minute><Second>. Use [+] or [−] to configure system Time.	

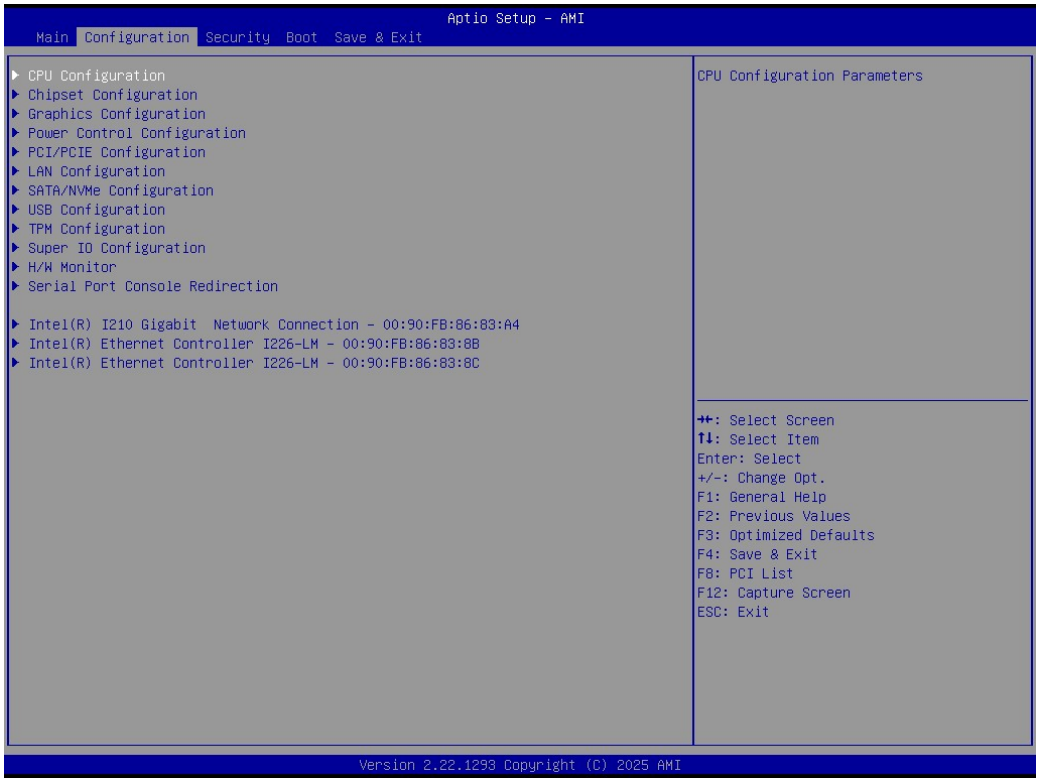
Detailed System Information



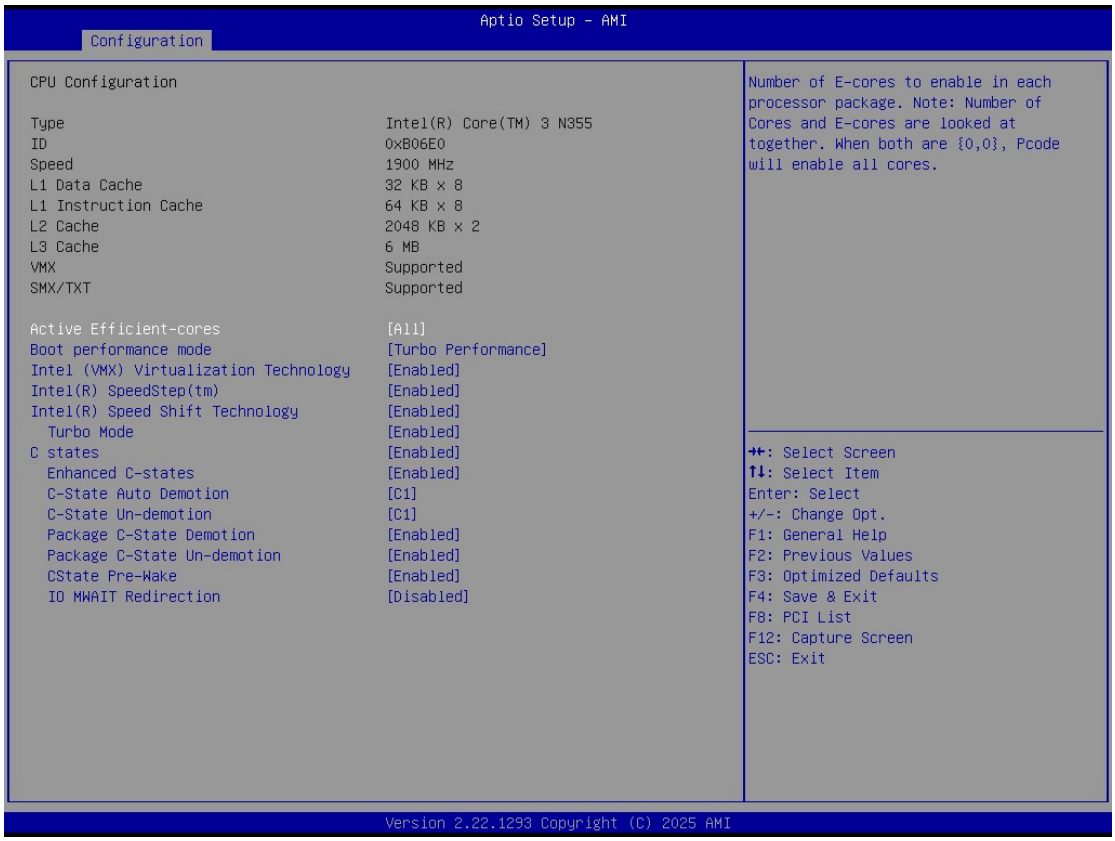


6.3 Configuration

Use this menu to set up the items of special enhanced features



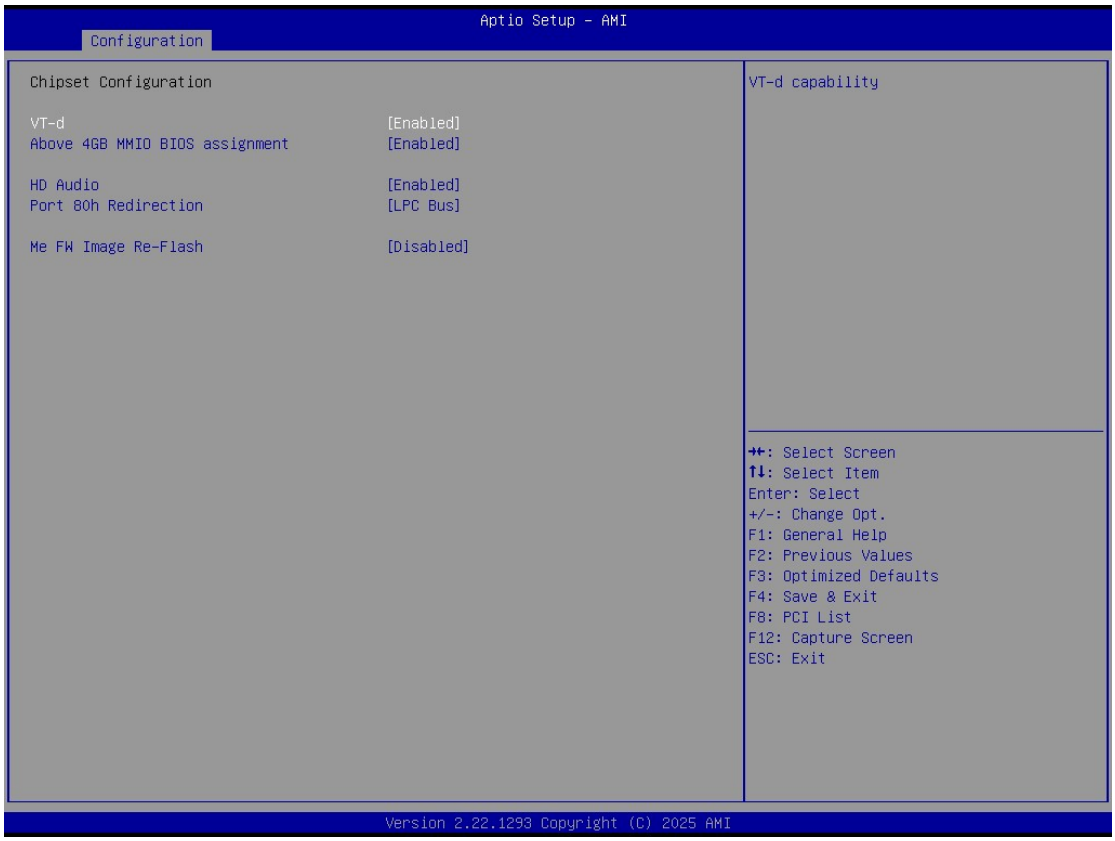
6.3.1 CPU Configuration



Feature	Description	Options
Active Efficient-Cores	Number of E-cores to enable in each processor package. Note: Number of Cores and E-cores are looked at together, When both are {0,0}, Pcode will enable all cores.	★All, 7, 6, 5, 4, 3, 2, 1
Boot performance mode	Select the performance state that the BIOS will set starting from reset vector	Max Non-Turbo Performance, ★Turbo Performance , Max Battery,
Intel (VMX) Virtualization Technology	When enabled, a VMM can utilize the additional hardware capabilities provided by Vander pool Technology.	Disabled, ★Enabled
Intel (R) Speed Step (tm)	Allows more than two frequency ranges to be supported.	Disabled, ★Enabled

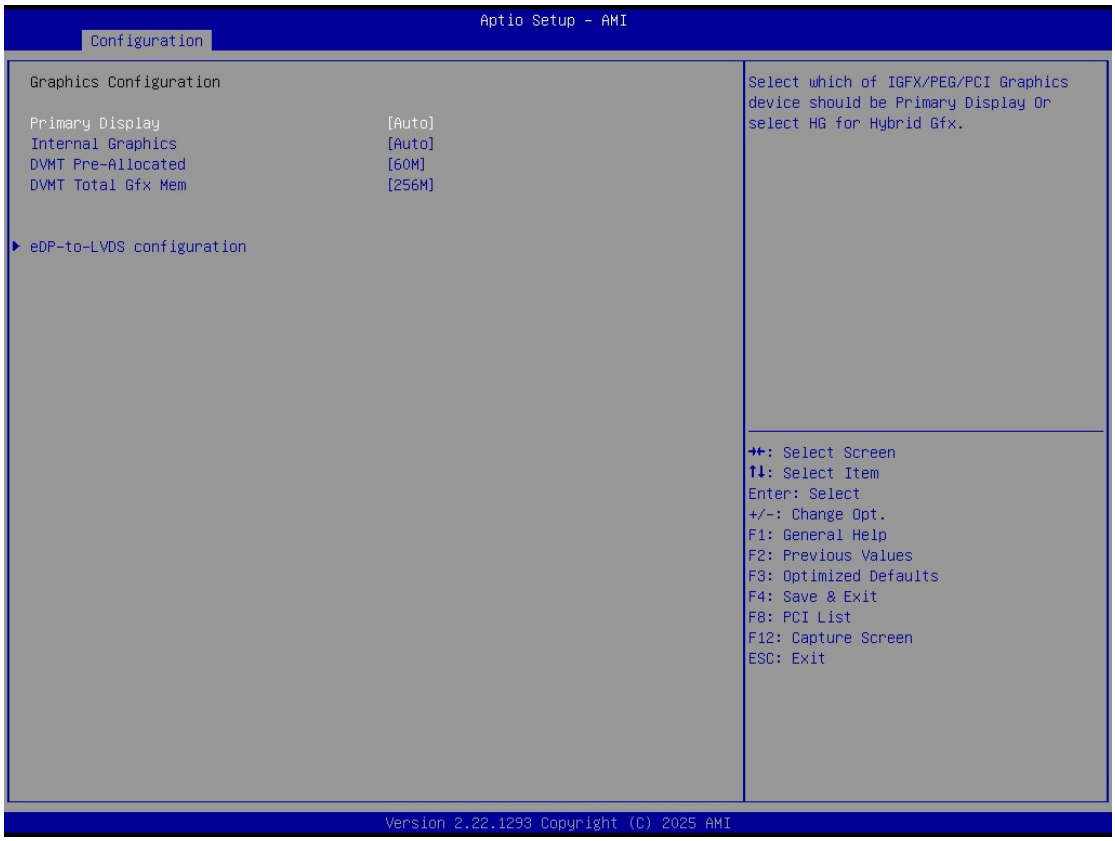
Feature	Description	Options
Intel (R) Speed Shift Technology	Enable/Disable Intel® Speed Shift Technology support. Enabling will expose the CPPC v2 interface to allow for hardware controlled P-states	Disabled, ★Enabled
Turbo Mode	Enable/Disable processor Turbo Mode (requires EMTTM enabled too). AUTO means enabled.	Disabled, ★Enabled
C states	Enable/disable CPU Power Management. Allows CPU to go to C states when it's not 100% utilized	Disabled, ★Enabled
Enhanced C-states	Enable/Disable C1E.When enabled, CPU will switch to minimum speed when all cores enter C-state	Disabled, ★Enabled
C-State Auto Demotion	Configure C-State Auto Demotion	Disabled, ★C1
C-State Un-demotion	Configure C-State Un-demotion	Disabled, ★C1
Package C-State Demotion	Package C-State Demotion	Disabled, ★Enabled
Package C-State Un-demotion	Package C-State Un-demotion	Disabled, ★Enabled
CState Pre-Wake	Disable – Sets bit 30 of POWER_CTL MSR(0x1FC) to 1 to disable the Cstate Pre-Wake	Disabled, ★Enabled
IO MWAIT Redirection	When set, will map IO_read instructions sent to IO registers PMG_IO_BASE_ADDRBASE+offset to MWAIT(offset)	★Disabled, Enabled

6.3.2 Chipset Configuration



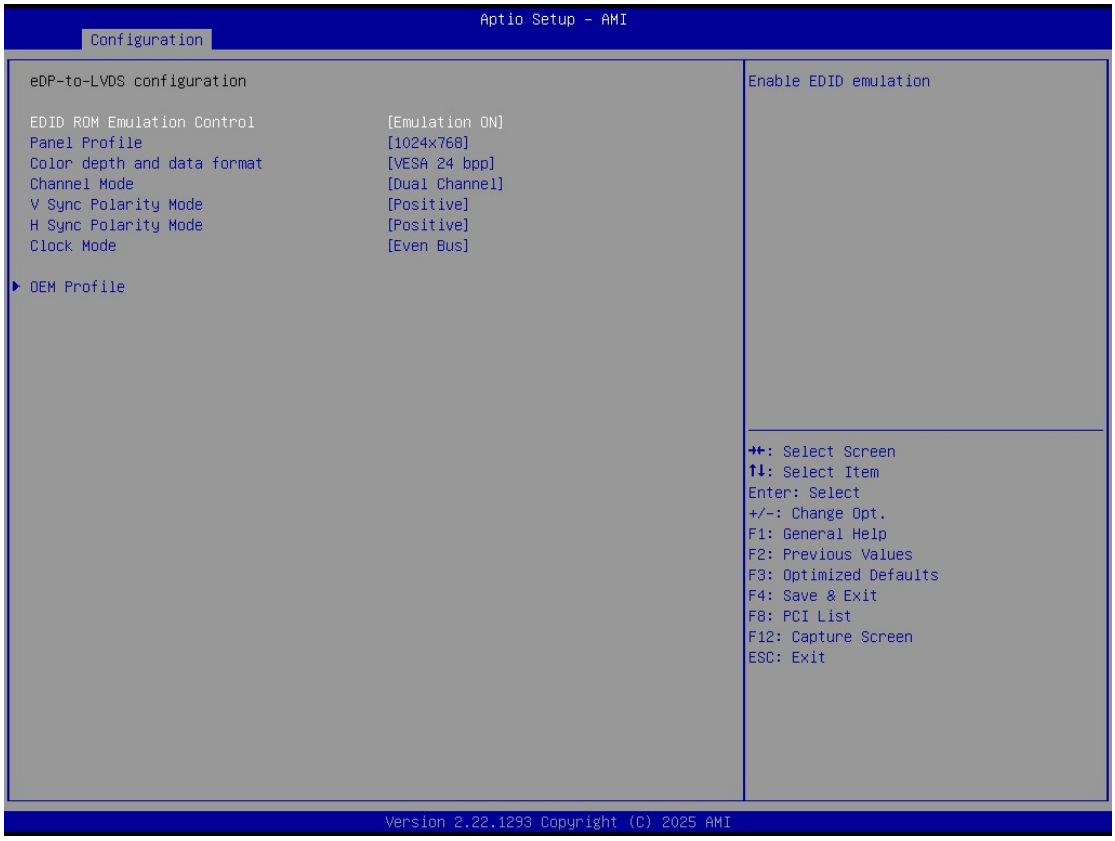
Feature	Description	Options
VT-d	VT-d Capability.	Disabled, ★Enabled
Above 4GB MMIO BIOS assignment	Enable/Disable above 4GB Memory Mapped IO BIOS assignment, This is enabled automatically when Aperture Size is set to 2048MB.	Disabled, ★Enabled
HD Audio	Control Detection of the HD-Audio device. Disabled = HDA will be unconditionally disabled. Enabled = HDA will be unconditionally enabled.	★Disabled, Enabled
Port 80h Redirection	Control where the Port 80h cycles are sent.	★LPC Bus, PCIE Bus
Me FW Image Re-Flash	Enable/Disable Me FW Image Re-Flash function.	★Disabled, Enabled

6.3.3 Graphics Configuration



Feature	Description	Options
Primary Display	Select which of IGFX/PEG/PCI Graphics device should be Primary Display Or Select HG for Hybrid Gfx.	★Auto, IGFX, PEG Slot, PCH PCI
Internal Graphics	Keep IGFX enable based on the setup options.	★Auto, Disabled, Enabled
DVMT Pre-Allocated	Select DVMT 5.0 Pre-Allocated (Fixed) Graphics Memory size used by the Internal Graphics Device.	32M,64M, 96M, 128M, 160M, 12M, 16M,20M, 24M, 28M, 32M/F7,36M,40M,44M,48M, 52M,56M, ★60M
DVMT Total Gfx Mem	Select DVMT5.0 Total Graphic Memory size used by the Internal Graphics Device	★256M, 128M, MAX

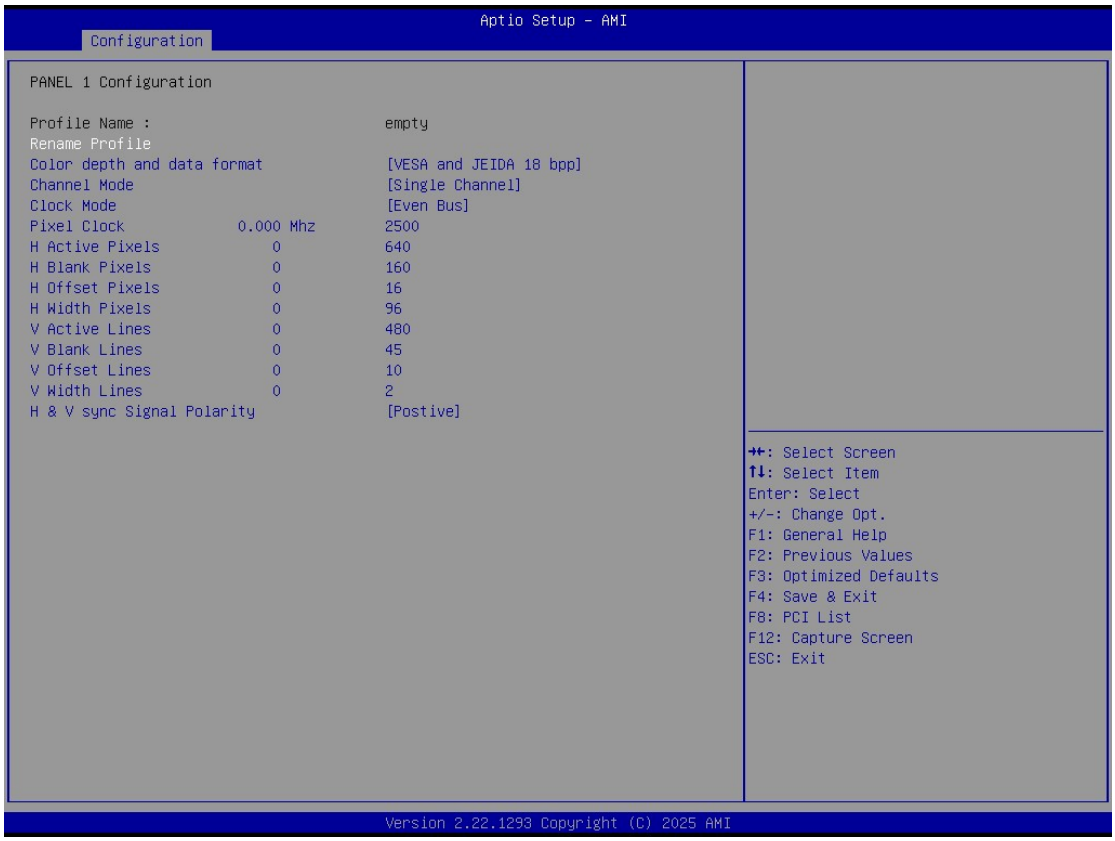
eDP-to-LVDS configuration:



Feature	Description	Options
EDID ROM Emulation Control	Enable EDID emulation	Emulation OFF, ★Emulation ON
Panel Profile	Select Panel Profile for current use	640x480, 800x480, 800x600, ★1024x768, 1280x1024, 1366x768, 1440x900, 1920x1080, OEM Profile
Color depth and data format	Color depth and data format	★VESA 24 bpp, JEIDA 24 bpp, VESA and JEIDA 18 bpp

Feature	Description	Options
Channel Mode	Select LVDS Channel Mode	Single Channel, ★Dual Channel
V Sync Polarity Mode	Select V Sync Polarity Mode	★Positive, Negative
H Sync Polarity Mode	Select H Sync Polarity Mode	★Positive, Negative
Clock Mode	Select clock output for LVDS.	★Even Bus, Odd Bus, Both Buses

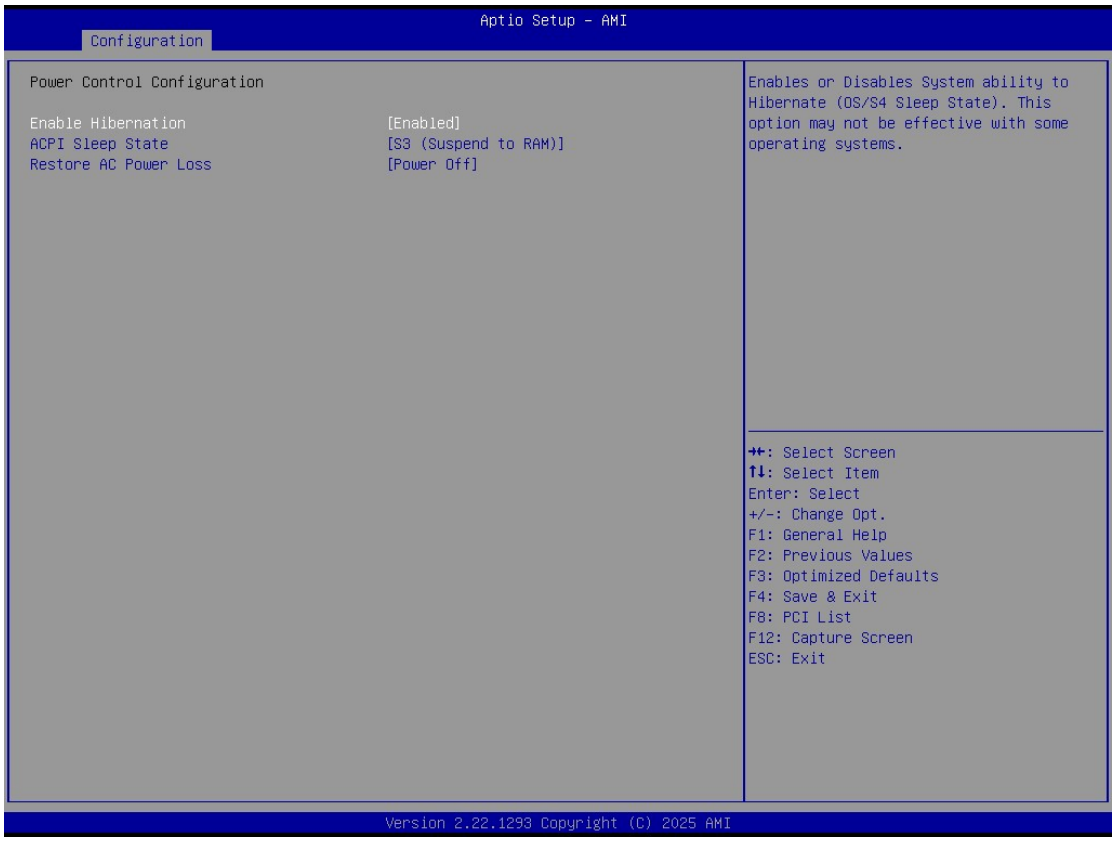
OEM Profile: PANEL 1 Configuration



Feature	Description	Options
Rename Profile	Rename Profile name	
Color depth and data format	Select Color depth and data format.	VESA 24 bpp, JEIDA 24 bpp ★VESA and JEIDA 18 bpp
Channel Mode	Select LVDS Channel Mode.	★Single channel, Dual channel
Clock Mode	Select Clock output for LVDS.	★Even Bus, Odd Bus, Both Buses
Pixel Clock	Pixel Clock (10Khz)	★ 2500
H Active Pixels	H Active Pixels (Pixel)	★ 640
H Blank Pixels	H Blank Pixels (Pixel)	★ 160

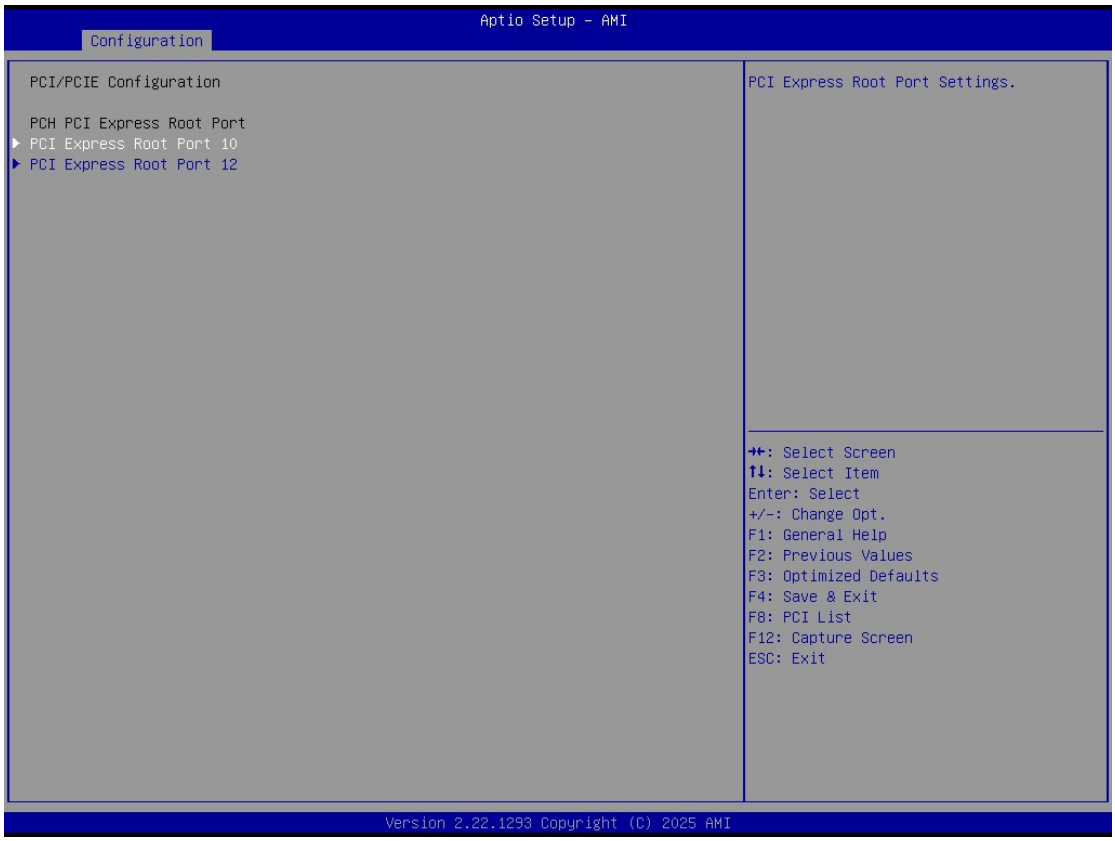
Feature	Description	Options
H Offset Pixels	H Offset Pixels (Pixel)	★ 16
H Width Pixels	H Width Pixels (Pixel)	★ 96
V Active Lines	V Active Lines (Line)	★ 480
V Blank Lines	V Blank Lines (Line)	★ 45
V Offset Lines	V Offset Lines (Line)	★ 10
V Width Lines	V Width Lines (Line)	★ 2
H & V sync Signal Polarity	Flag: 0x1E Signal Polarity is Postive; 0x18 Signal Polarity is Non-Postive	★ Postive, Non-Postive

6.3.4 CPU Power Control Configuration

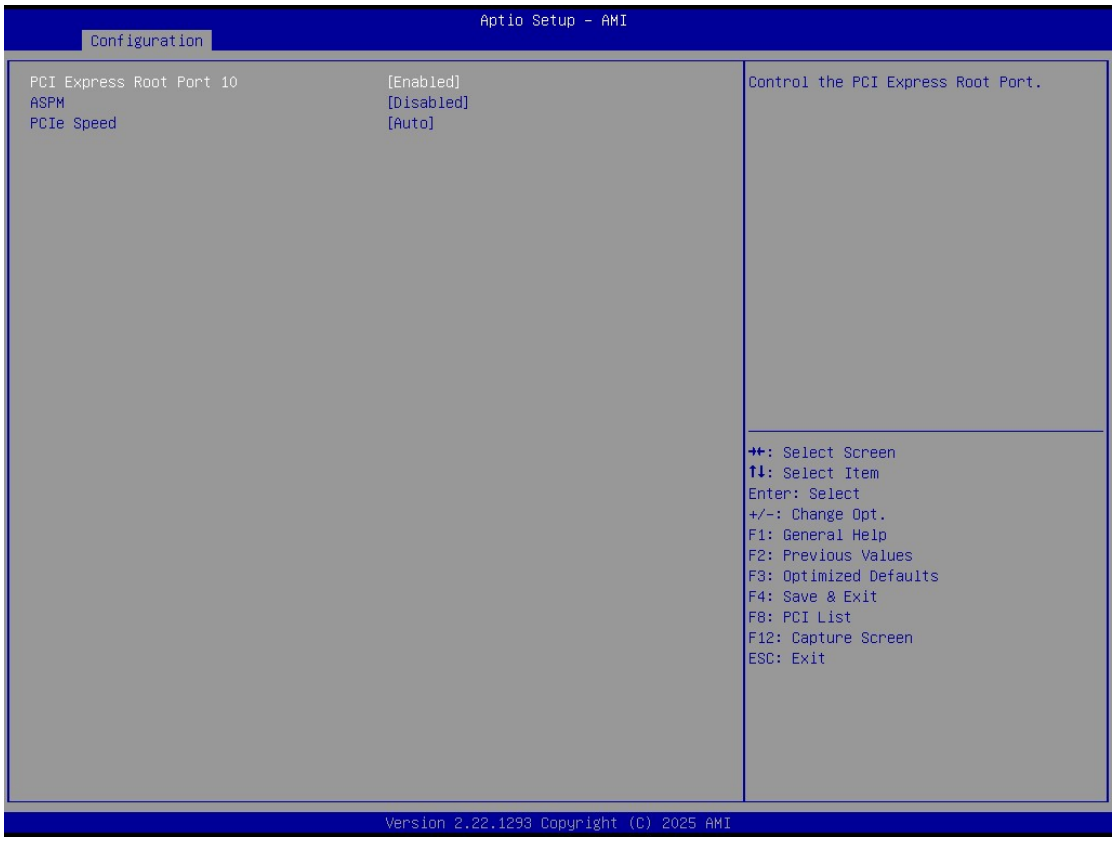


Feature	Description	Options
Enable Hibernation	Enables or Disables System ability to Hibernate (OS/S4 Sleep State). This option may not be effective with some operating systems.	Disabled, ★Enabled
ACPI Sleep State	Select the highest ACPI sleep state the system will enter when the SUSPEND button is pressed.	★S3 (Suspend to RAM), Suspend Disabled
Restore AC Power Loss	Specify what state to go to when power is re-applied after a power failure (G3 state)	★Power Off, Power On, Last State

6.3.5 PCI/PCIE Configuration

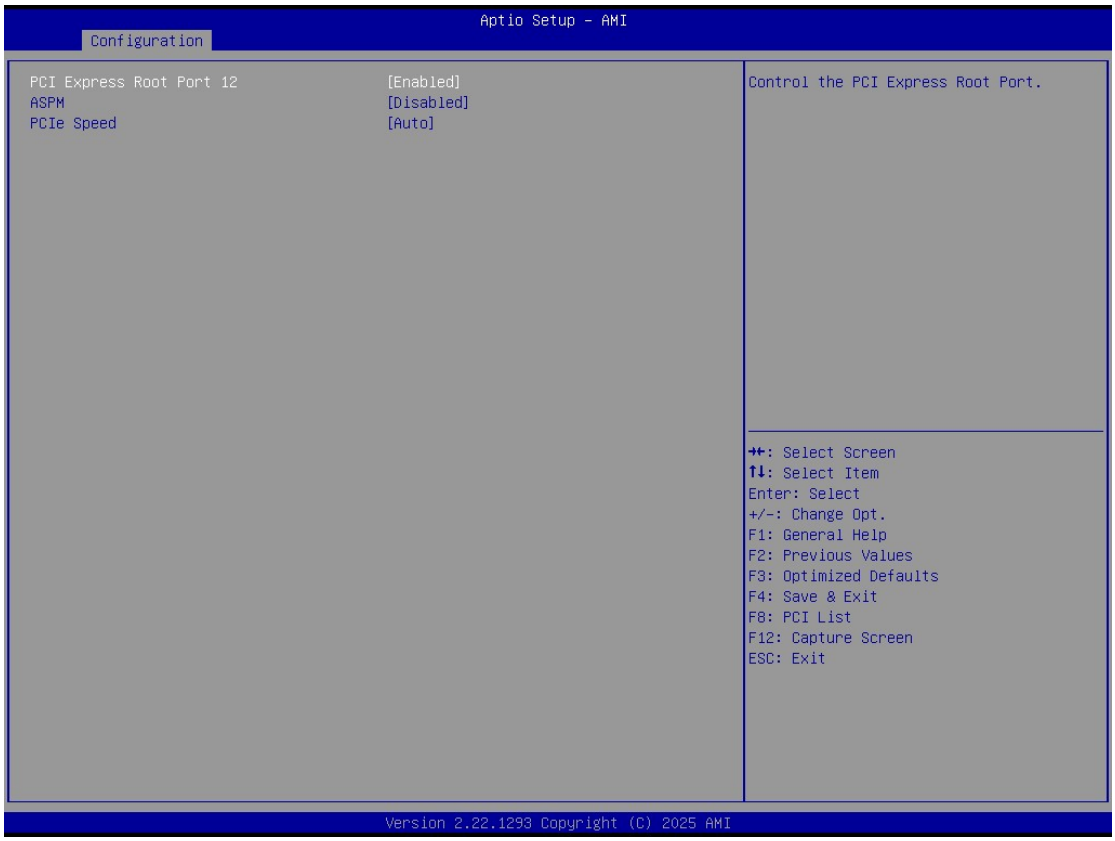


PCI Express Root Port 10



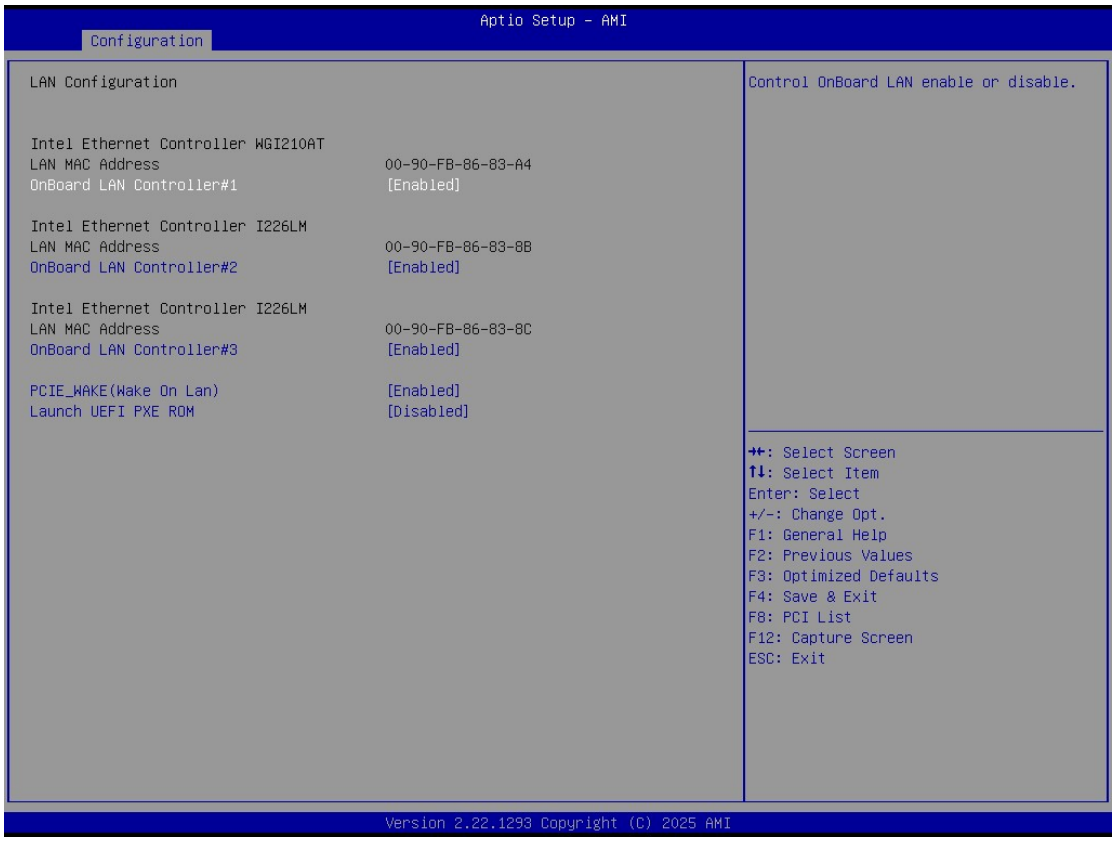
Feature	Description	Options
PCI Express Root Port 10	Control the PCI Express Root Port.	★Enabled, Disabled
ASPM	Set the ASPM Level: Force L0s – Force all links to L0s state; Auto – BIOS AUTO configure ; DISABLE – Disables ASPM	★Disabled, L1, Auto
PCIe Speed	Configure PCIe Speed	★Auto, Gen1, Gen2, Gen3

PCI Express Root Port 12



Feature	Description	Options
PCI Express Root Port 12	Control the PCI Express Root Port.	★Enabled, Disabled
ASPM	Set the ASPM Level: Force L0s – Force all links to L0s state; Auto – BIOS AUTO configure ; DISABLE – Disables ASPM	★Disabled, L1, Auto
PCIe Speed	Configure PCIe Speed	★Auto, Gen1, Gen2, Gen3

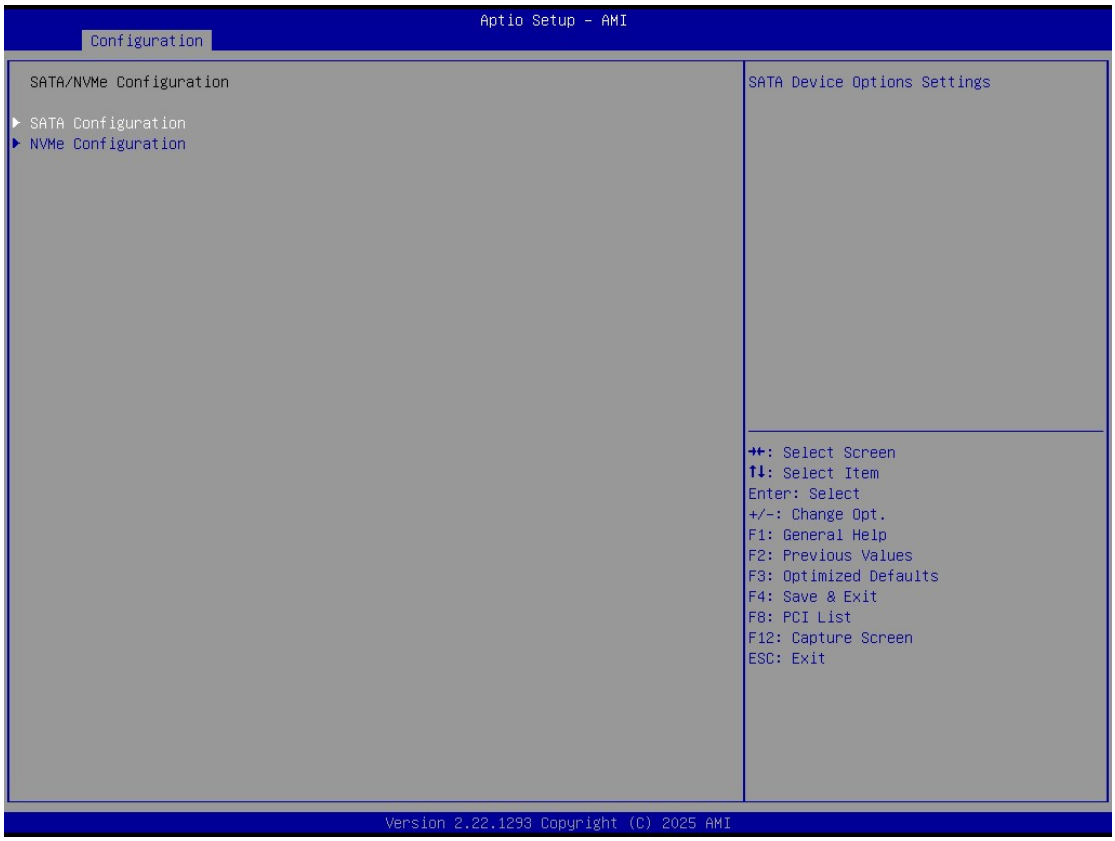
6.3.6 LAN Configuration



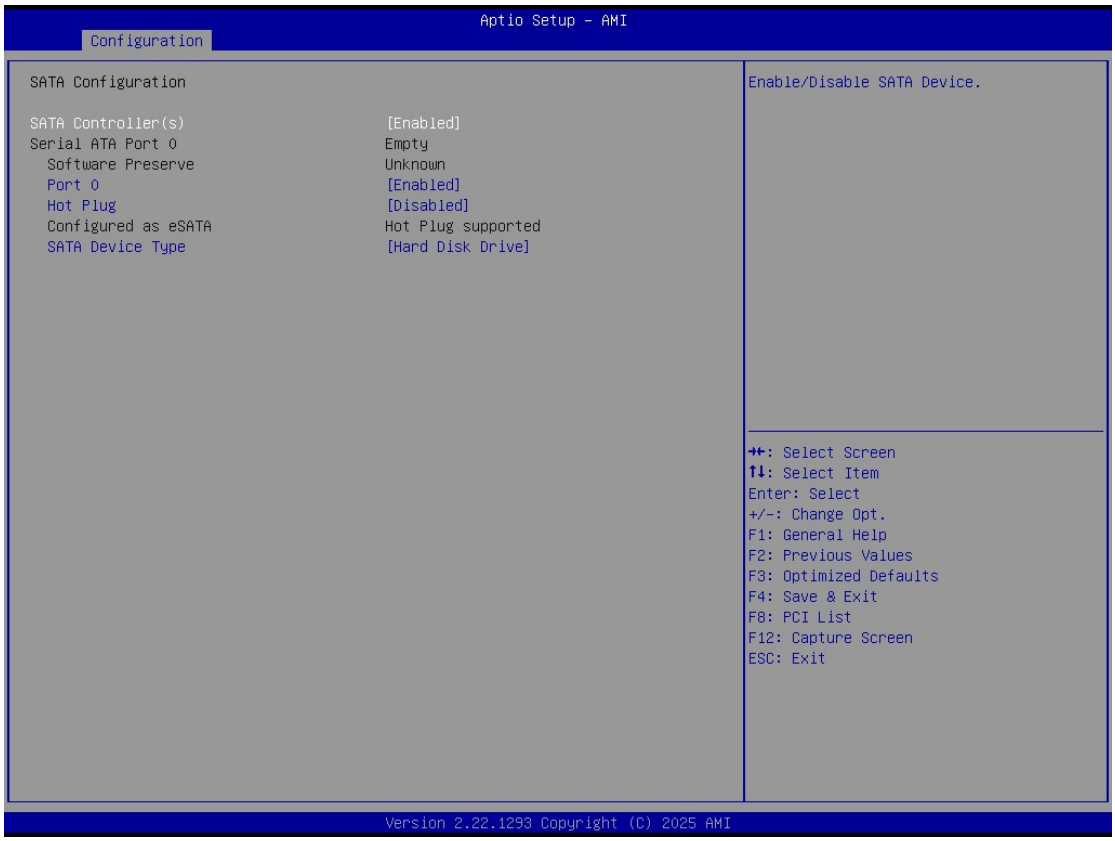
Feature	Description	Options
OnBoard LAN Controller #1	Control OnBoard LAN Enable or Disable.	Disabled, ★Enabled
OnBoard LAN Controller #2	Control OnBoard LAN Enable or Disable.	Disabled, ★Enabled
OnBoard LAN Controller #3	Control OnBoard LAN Enable or Disable.	Disabled, ★Enabled
PCIE_WAKE (Wake On Lan)	Control the PCIE Wake# pin for Wake On Lan function.	Disabled, ★Enabled
Launch UEFI PXE ROM	Enable/Disable UEFI Network Stack	★Disabled, Enabled

Feature	Description	Options
Launch UEFI PXE ROM (Enabled)		
IPv4 PXE Support	Enable/Disable IPv4 PXE boot support. If disabled, IPv4 PXE boot support will not be available.	Disabled, ★Enabled
IPv4 HTTP Support	Enable/Disable IPv4 HTTP boot support. If disabled, IPv4 HTTP boot support will not be available.	Disabled, ★Enabled
IPv6 PXE Support	Enable/Disable IPv6 PXE boot support. If disabled, IPv6 PXE boot support will not be available.	Disabled, ★Enabled
IPv6 HTTP Support	Enable/Disable IPv6 HTTP boot support. If disabled, IPv6 HTTP boot support will not be available.	Disabled, ★Enabled
PXE boot wait time	Wait time in seconds to press ESC key to abort the PXE boot. Use either +/- or numeric keys to set the value.	★0
Media detect count	Number of times the presence of media will be checked. Use either +/- or numeric keys to set the value.	★1

6.3.7 SATA / NVMe Configuration

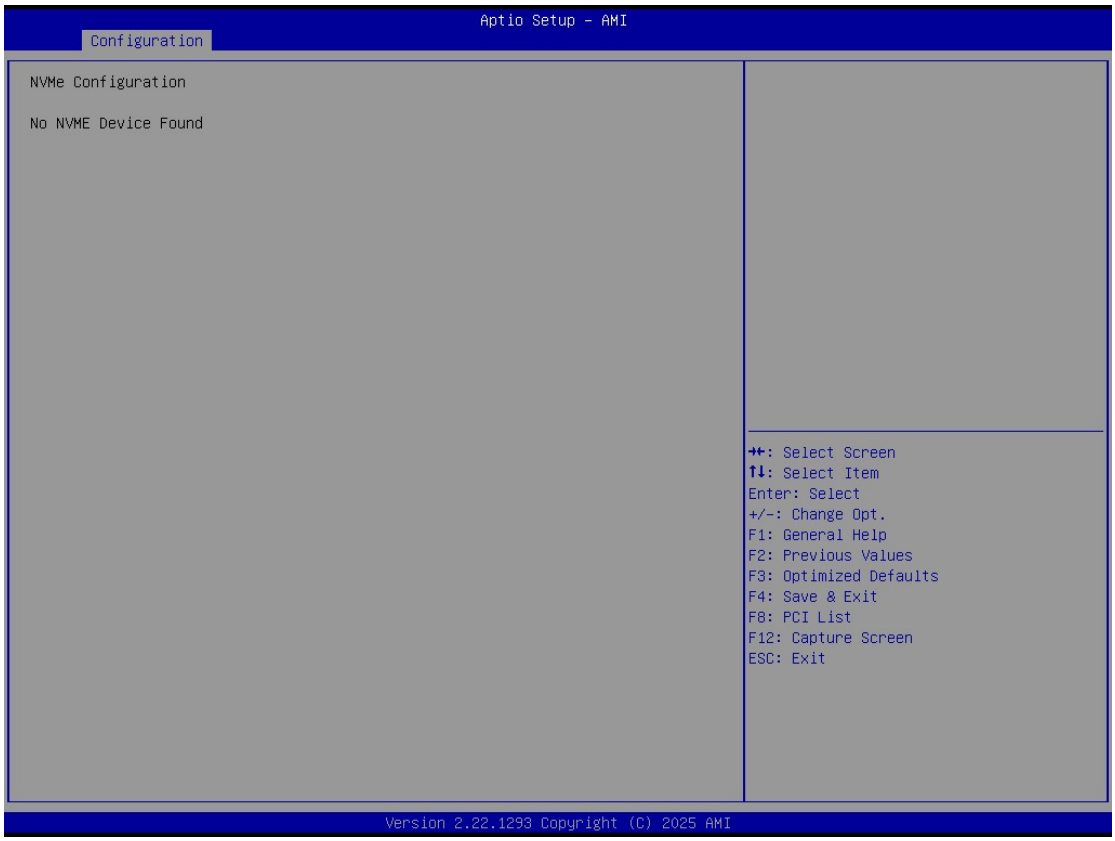


SATA Configuration

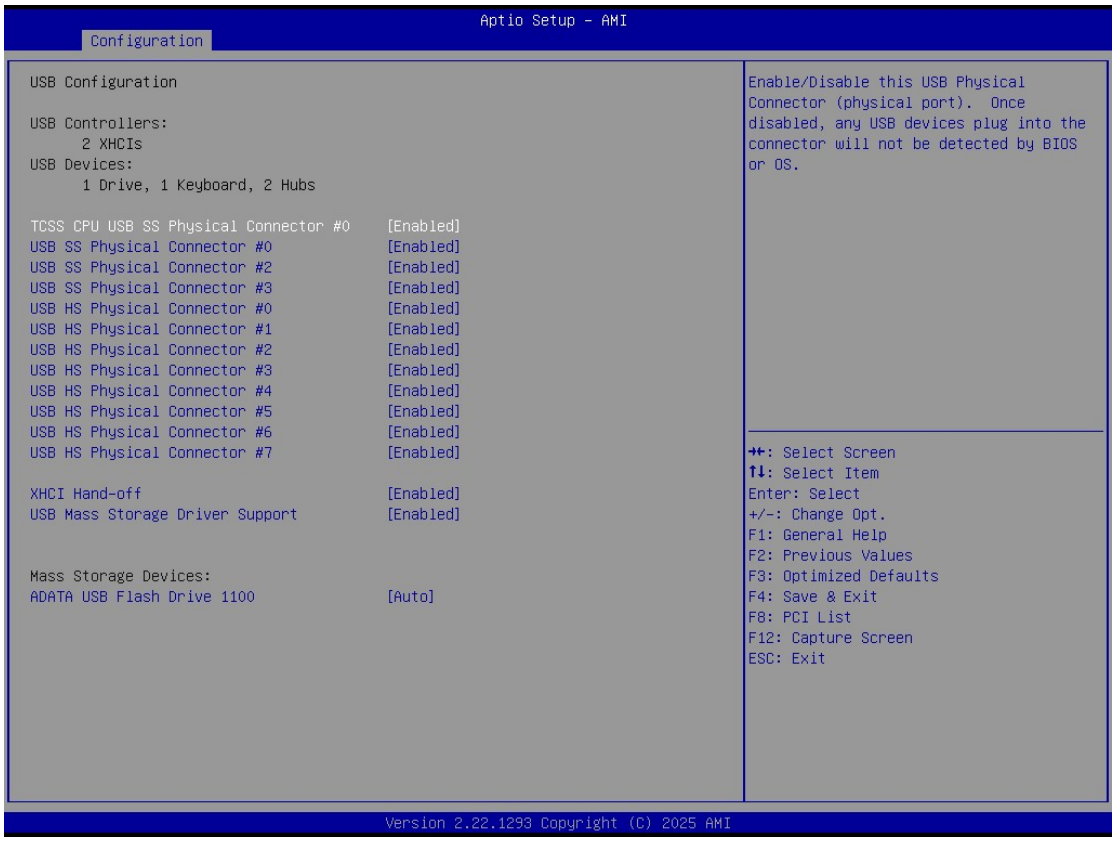


Feature	Description	Options
SATA Controller(s)	Enable/Disable SATA Device	Disabled, ★Enabled
Serial ATA Port 0		
Port 0	Enabled or Disabled SATA Port	Disabled, ★Enabled
Hot plug	Designates this port as Hot pluggable.	★Disabled, Enabled
SATA Device Type	Identify the SATA port is connected to Solid State Drive or Hard Disk Drive.	★Hard Disk Drive, Solid State Drive

NVMe Configuration



6.3.8 USB Configuration

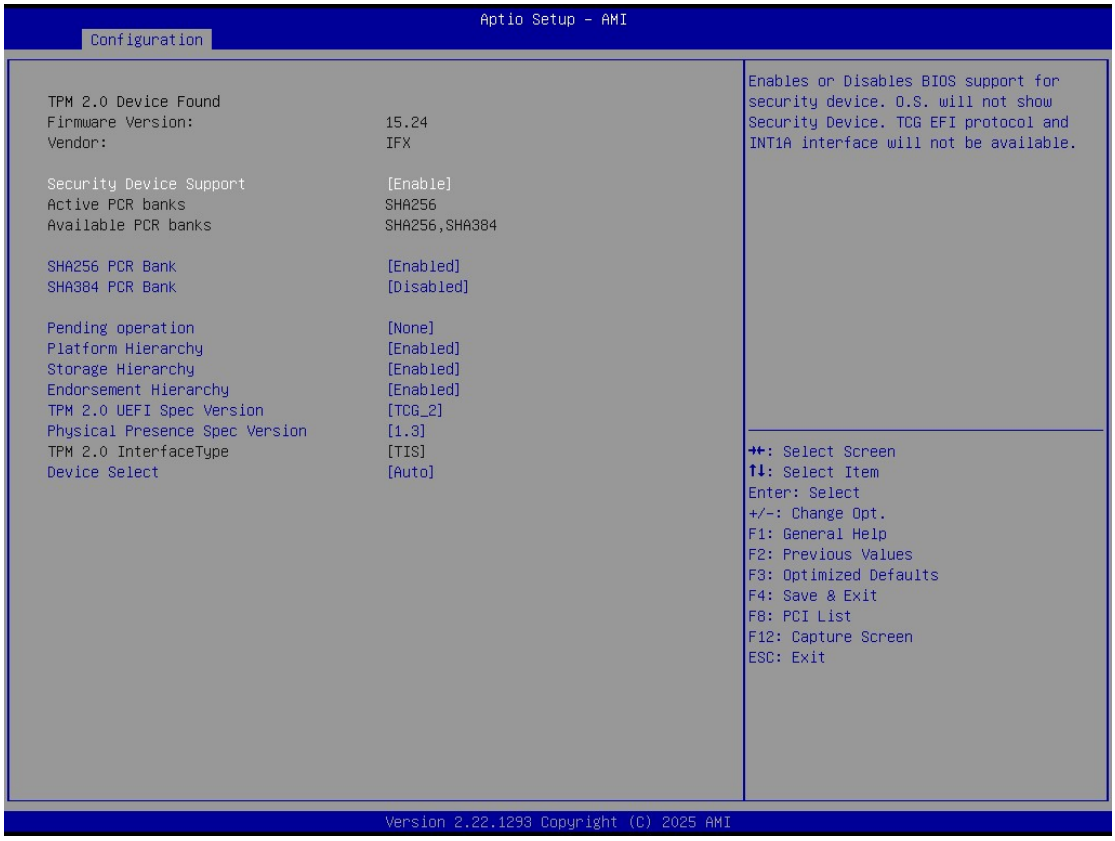


Feature	Description	Options
TCSS CPU USB SS Physical Connector #0	Enabled/Disabled this USB Physical connector (physical port). Once disabled, any USB devices plug into the connector will not be detected by BIOS or OS.	Disabled, ★Enabled
USB SS Physical Connector #0	Enabled/Disabled this USB Physical connector (physical port). Once disabled, any USB devices plug into the connector will not be detected by BIOS or OS.	Disabled, ★Enabled
USB SS Physical Connector #2	Enabled/Disabled this USB Physical connector (physical port). Once disabled, any USB devices plug into the connector will not be detected by BIOS or OS.	Disabled, ★Enabled
USB SS Physical Connector #3	Enabled/Disabled this USB Physical connector (physical port). Once disabled, any USB devices plug into the connector will not be detected by BIOS or OS.	Disabled, ★Enabled

Feature	Description	Options
USB HS Physical Connector #0	Enabled/Disabled this USB Physical connector (physical port). Once disabled, any USB devices plug into the connector will not be detected by BIOS or OS.	Disabled, ★Enabled
USB HS Physical Connector #1	Enabled/Disabled this USB Physical connector (physical port). Once disabled, any USB devices plug into the connector will not be detected by BIOS or OS.	Disabled, ★Enabled
USB HS Physical Connector #2	Enabled/Disabled this USB Physical connector (physical port). Once disabled, any USB devices plug into the connector will not be detected by BIOS or OS.	Disabled, ★Enabled
USB HS Physical Connector #3	Enabled/Disabled this USB Physical connector (physical port). Once disabled, any USB devices plug into the connector will not be detected by BIOS or OS.	Disabled, ★Enabled
USB HS Physical Connector #4	Enabled/Disabled this USB Physical connector (physical port). Once disabled, any USB devices plug into the connector will not be detected by BIOS or OS.	Disabled, ★Enabled
USB HS Physical Connector #5	Enabled/Disabled this USB Physical connector (physical port). Once disabled, any USB devices plug into the connector will not be detected by BIOS or OS.	Disabled, ★Enabled
USB HS Physical Connector #6	Enabled/Disabled this USB Physical connector (physical port). Once disabled, any USB devices plug into the connector will not be detected by BIOS or OS.	Disabled, ★Enabled
USB HS Physical Connector #7	Enabled/Disabled this USB Physical connector (physical port). Once disabled, any USB devices plug into the connector will not be detected by BIOS or OS.	Disabled, ★Enabled
XHCI Hand-off	This is a workaround for OSes without XHCI hand-off support. The XHCI ownership change should be claimed by XHCI driver	Disabled, ★Enabled
USB Mass Storage Driver Support	Enable/Disable USB Mass Storage Driver Support	Disabled, ★Enabled
Mass storage Devices:		
ADATA USB Flash Drive 1100	Mass storage device emulation type. 'AUTO' enumerates devices according to their media format. Optical drives are emulated as 'CDROM'; drives with no media will be emulated according to a drive type.	★Auto, Floppy, Forced FDD, Hard Disk, CD-ROM

6.3.9 TPM Configuration

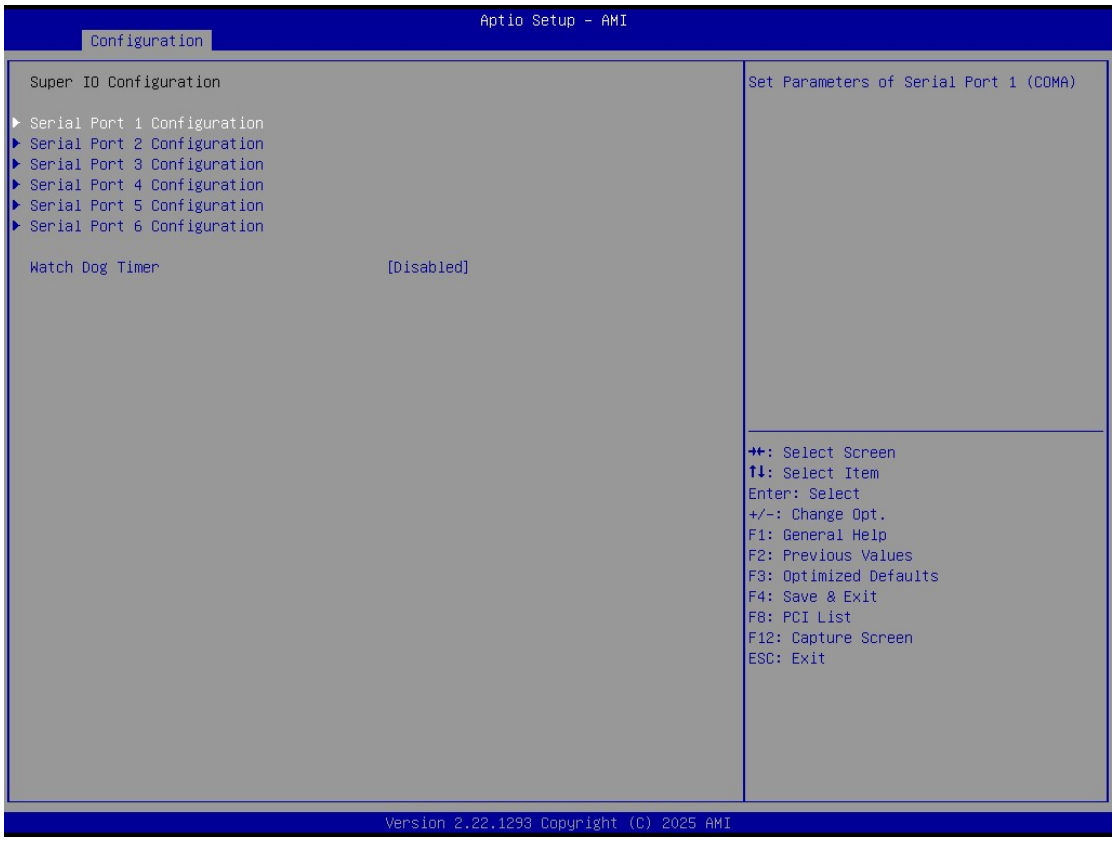
TPM 2.0 Device Found



Feature	Description	Options
Security Device Support	Enables or Disables BIOS support for security device. O.S. will not show Security Device. TCG EFI protocol and INT1A Interface will not be available.	Disabled, ★Enabled
SHA256 PCR Bank	Enables or Disables SHA256 PCR Bank.	Disabled, ★Enabled
SHA384 PCR Bank	Enables or Disables SHA384 PCR Bank.	★Disabled, Enabled
Pending operation	Schedule an Operation for the Security Device. Note: Your Computer will reboot during restart in order to change State of Security Device.	★None, TPM Clear
Platform Hierarchy	Enables or Disables Platform Hierarchy.	Disabled, ★Enabled

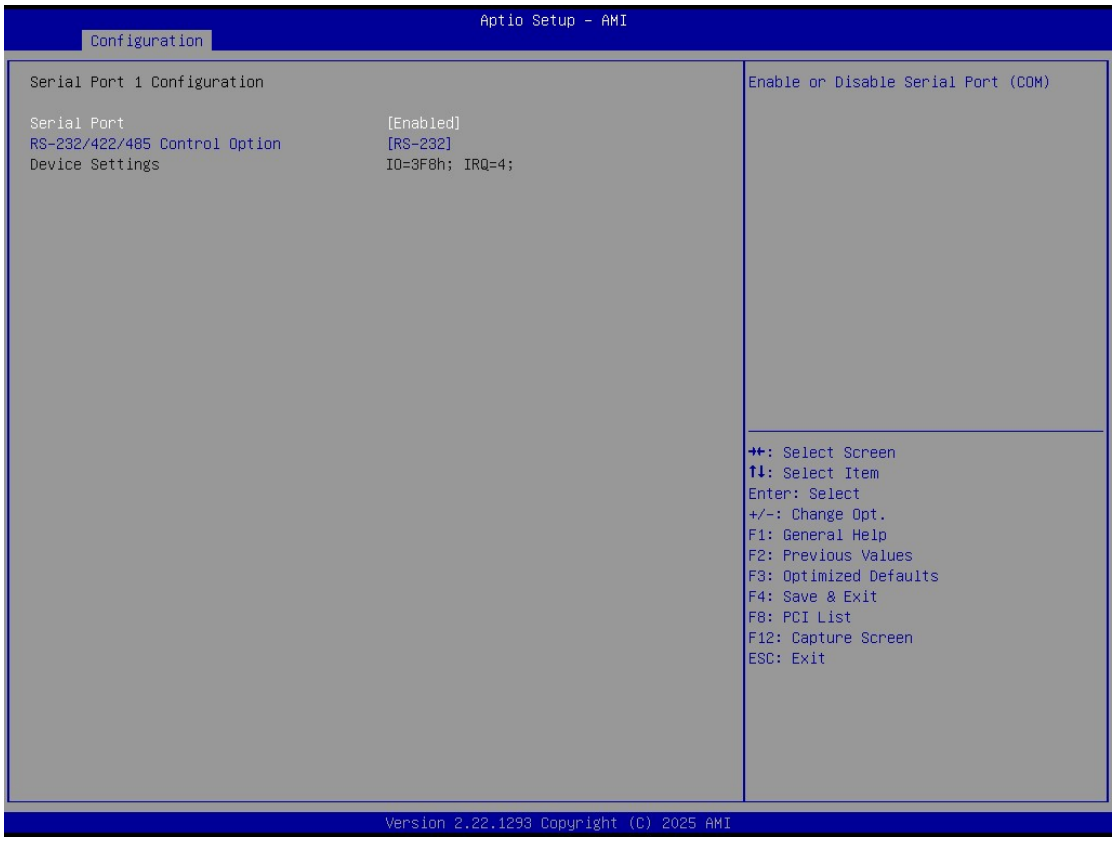
Feature	Description	Options
Storage Hierarchy	Enables or Disables Storage Hierarchy.	Disabled, ★Enabled
Endorsement Hierarchy	Enables or Disables Endorsement Hierarchy.	Disabled, ★Enabled
TPM 2.0 UEFI Spec Version	Select the TCG2 Spec Version Support. CG_1_2: the Compatible mode for Win8/Win10. TCG_2: Support new TCG2 protocol and event format for Win10 or later.	TCG_1_2, ★TCG_2
Physical Presence Spec Version	Select to Tell O.S. to Support PPI Spec Version 1.2 or 1.3. Note some HCK tests might not support 1.3.	1.2, ★1.3
Device Select	TPM 1.2 will restrict support to TPM 1.2 devices, TPM 2.0 will restrict support to TPM 2.0 devices, Auto will support both with the default set to TPM 2.0 devices if not found, TPM 1.2 devices will be enumerated.	★Auto, TPM 1.2, TPM 2.0

6.3.10 Super IO Configuration



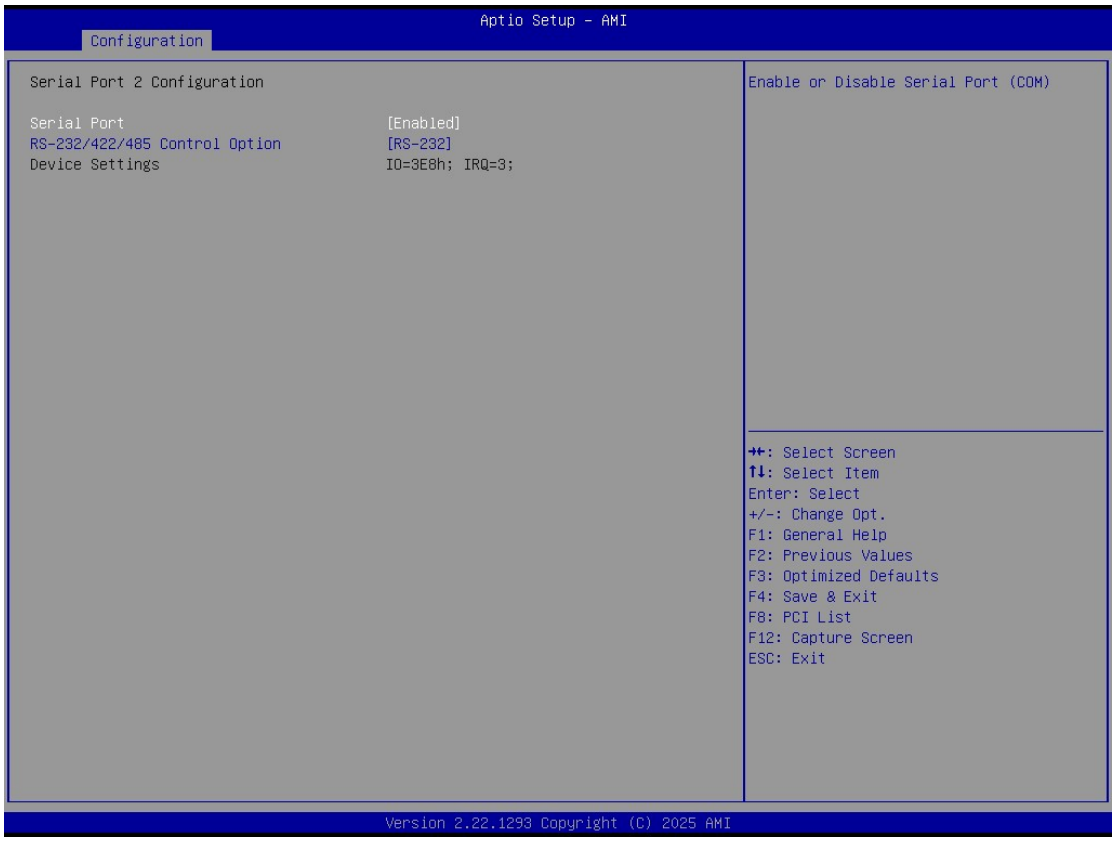
Feature	Description	Options
Watch Dog Timer	Enable/Disable Watch Dog Timer	★Disabled, Enabled
Watch Dog Timer [Enabled]		
Timer Unit	Select Timer count unit of WDT	★Second, Minute
Timer value	Set WDT Timer value seconds / minutes	★20

Serial Port 1 Configuration



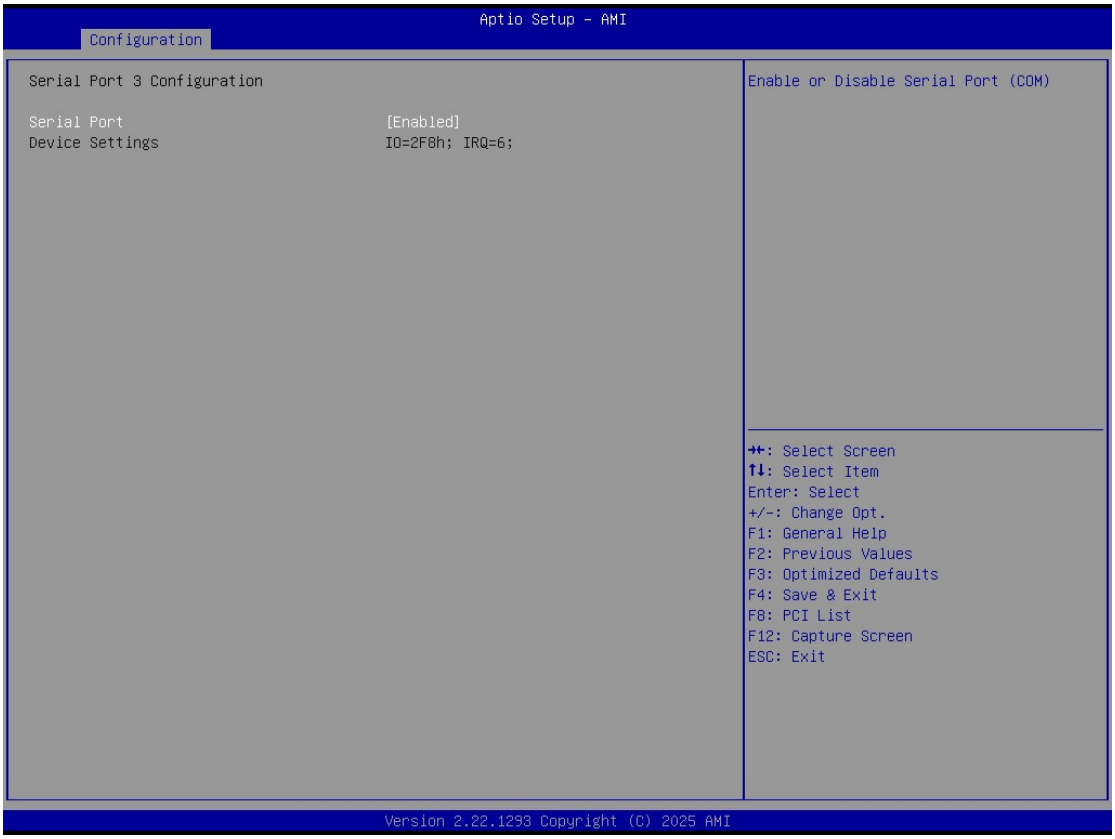
Feature	Description	Options
Serial Port	Enable or Disable Serial Port (COM)	Disabled, ★Enabled
RS-232/422/485 Control Option	Serial Port 1 RS-232/422/485 Control Option	★RS-232, RS-485 HALF DUPLEX, RS-422 FULL DUPLEX,

Serial Port 2 Configuration



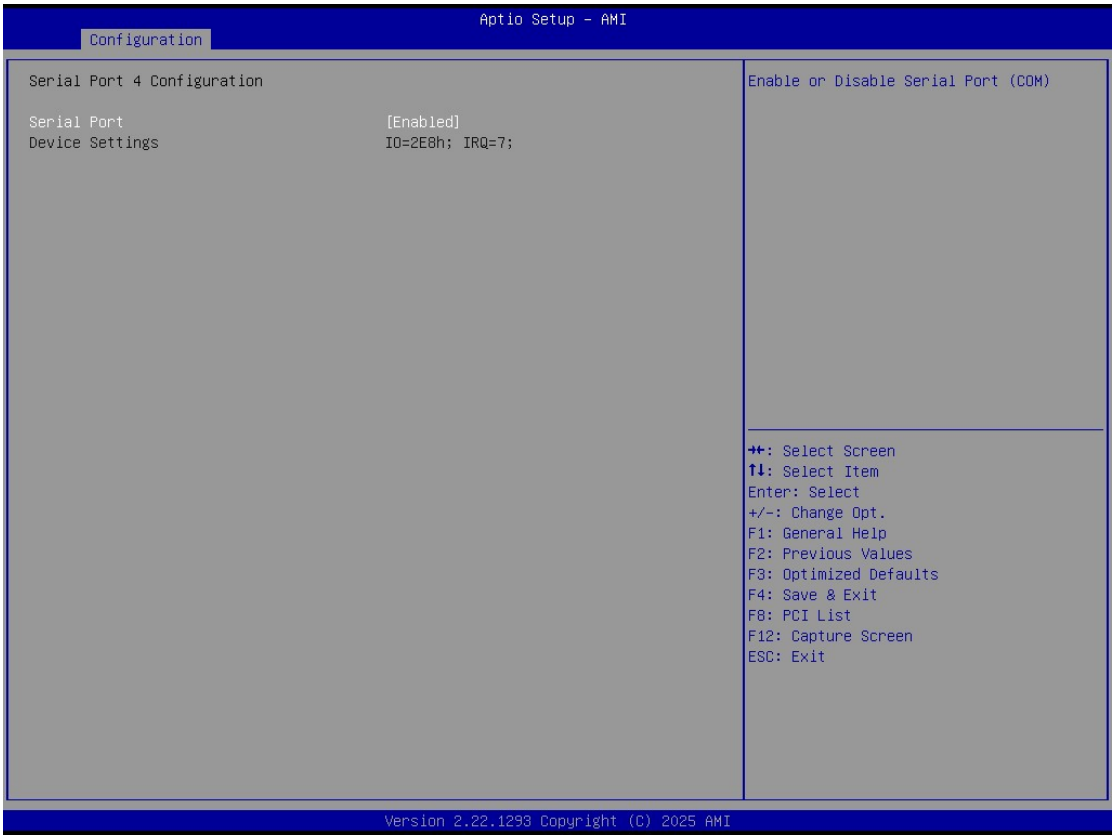
Feature	Description	Options
Serial Port	Enable or Disable Serial Port (COM)	Disabled, ★Enabled
RS-232/422/485 Control Option	Serial Port 2 RS-232/422/485 Control Option	★RS-232, RS-485 HALF DUPLEX, RS-422 FULL DUPLEX,

Serial Port 3 Configuration



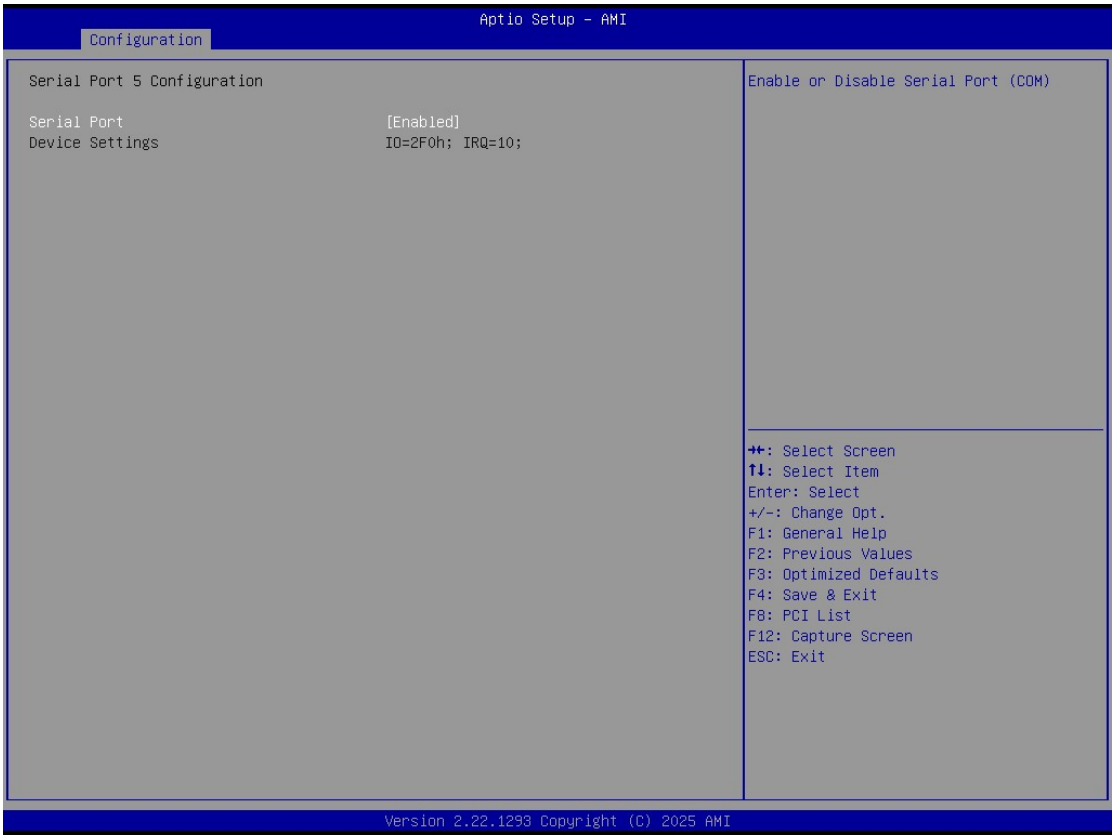
Feature	Description	Options
Serial Port	Enable or Disable Serial Port (COM)	Disabled, ★Enabled

Serial Port 4 Configuration



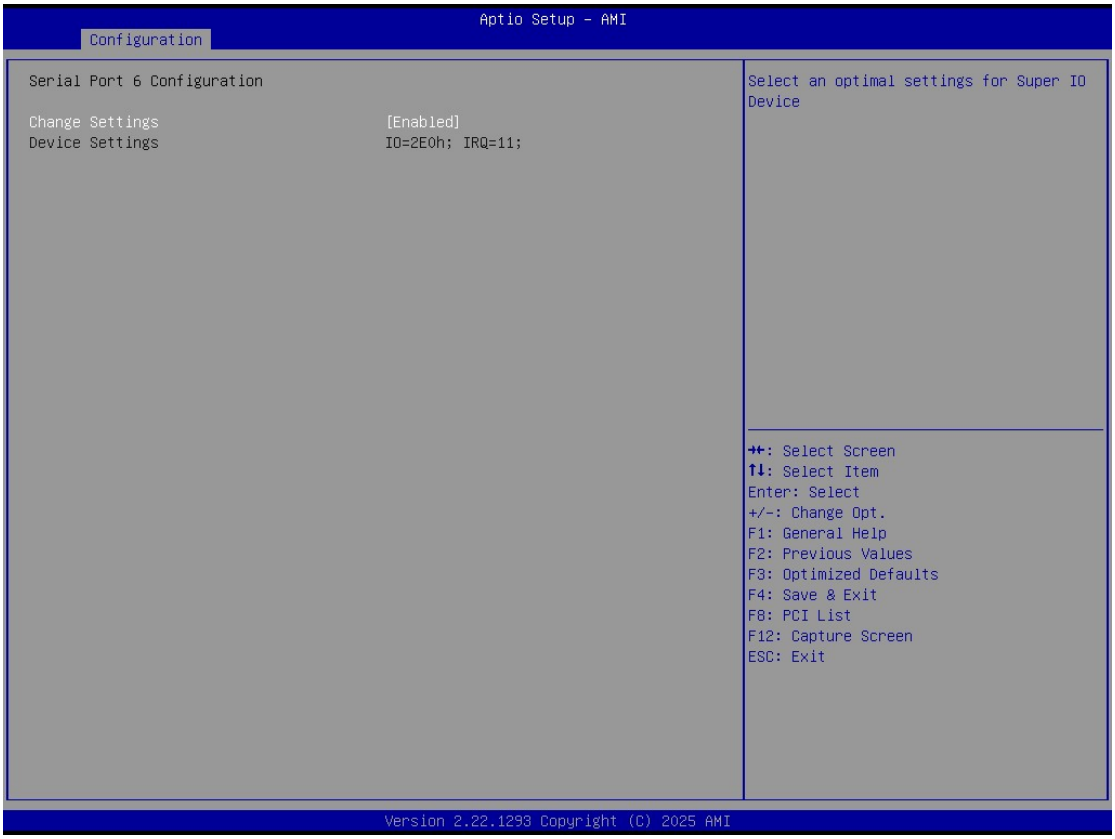
Feature	Description	Options
Serial Port	Enable or Disable Serial Port (COM)	Disabled, ★Enabled

Serial Port 5 Configuration



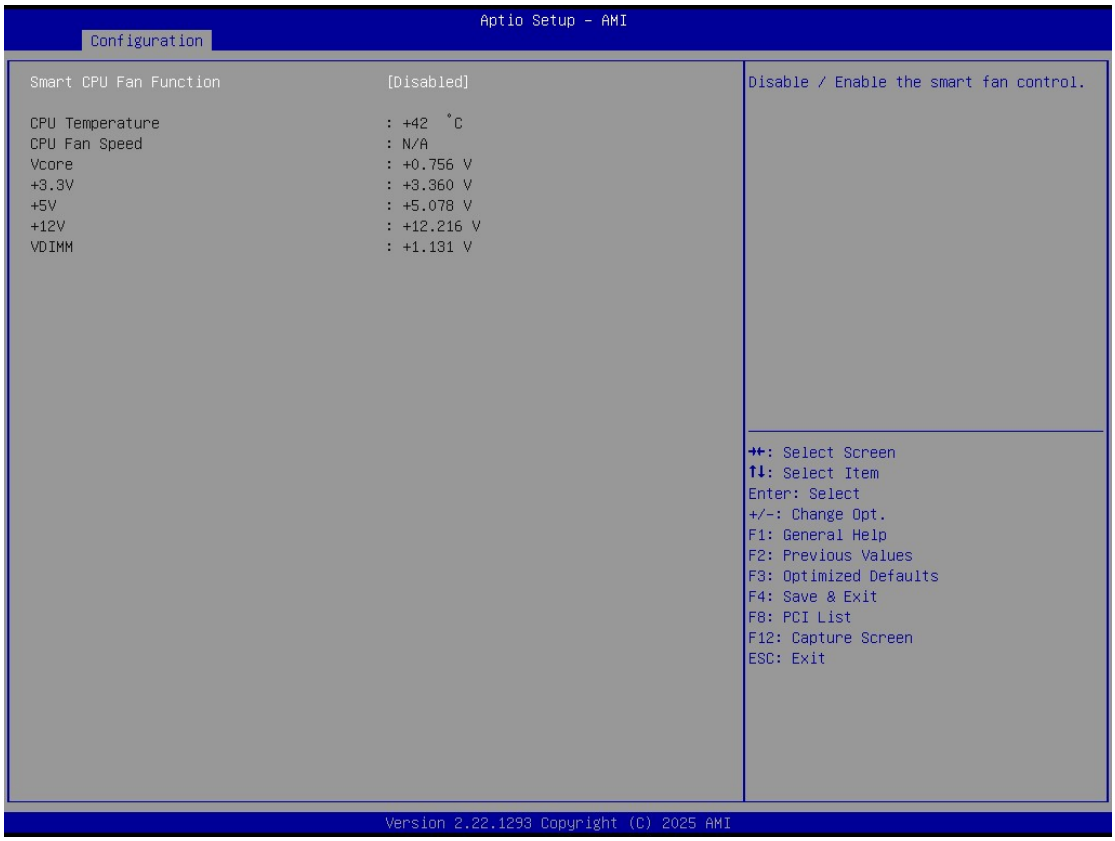
Feature	Description	Options
Serial Port	Enable or Disable Serial Port (COM)	Disabled, ★Enabled

Serial Port 6 Configuration



Feature	Description	Options
Serial Port	Enable or Disable Serial Port (COM)	Disabled, ★Enabled

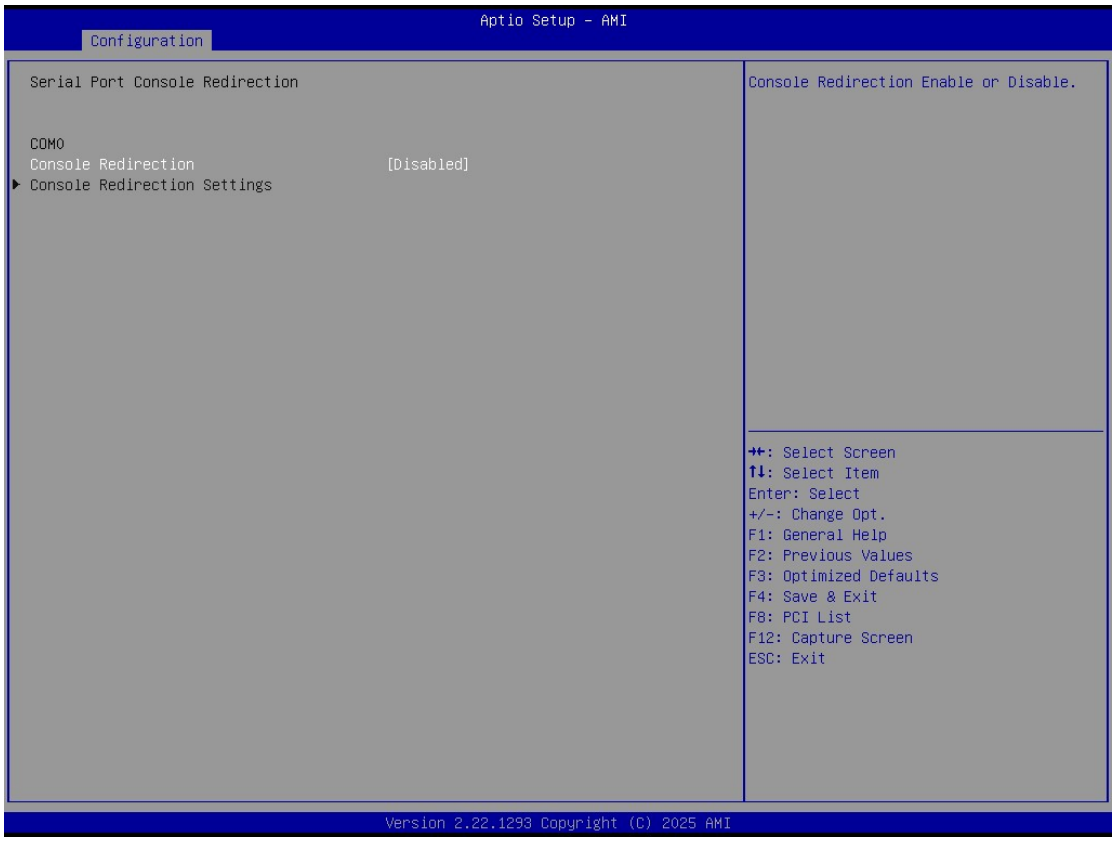
6.3.11 HW Monitor



Feature	Description	Options
Smart CPU Fan Function	Disable / Enable the smart fan control.	★Disabled, Enabled
Smart CPU Fan Function [Enabled]		
Smart Fan 1 Control Mode	Select Smart Fan Control Mode.	★Thermal Cruise Mode Fan Control Mode
Smart Fan 1 Control Mode [Thermal Cruise Mode]		
Smart Fan 1 Tolerance Temp	In Thermal Cruise Mode: tolerance of target temperature.	★5
Smart Fan 1 Start Target Temp	In Thermal Cruise Mode: Start temperature.	★40

Feature	Description	Options
Smart Fan 1 Full Target Temp	In Thermal Cruise Mode: Full speed temperature.	★60
Smart Fan 1 Low End	In Thermal Cruise Mode: low end of fan speed (0-100%)	★5
Smart Fan 1 Control Mode [Fan Control Mode]		
Smart Fan 1 Speed (%)	Set Smart speed 0-100%.	★100

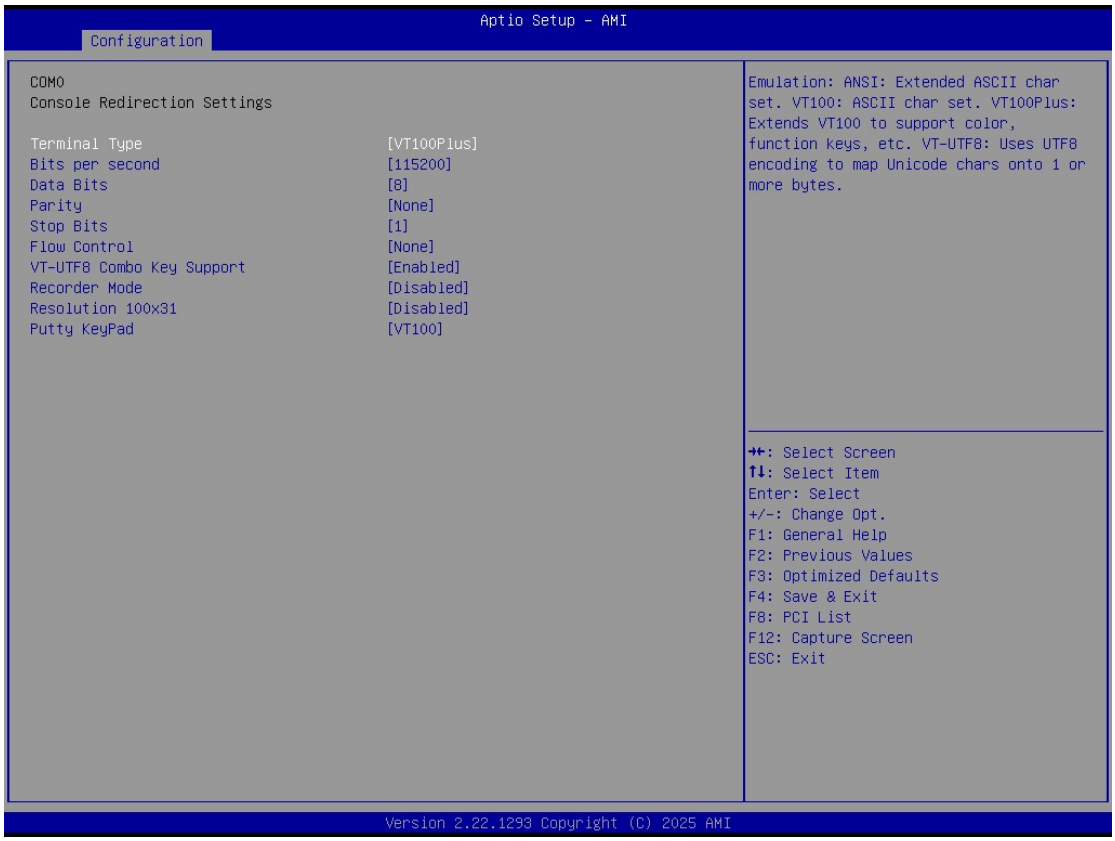
6.3.12 Serial Port Console Redirection



Feature	Description	Options
Console Redirection	Console Redirection Enable or Disable	★Disabled, Enabled

COM0 Console Redirection Settings:

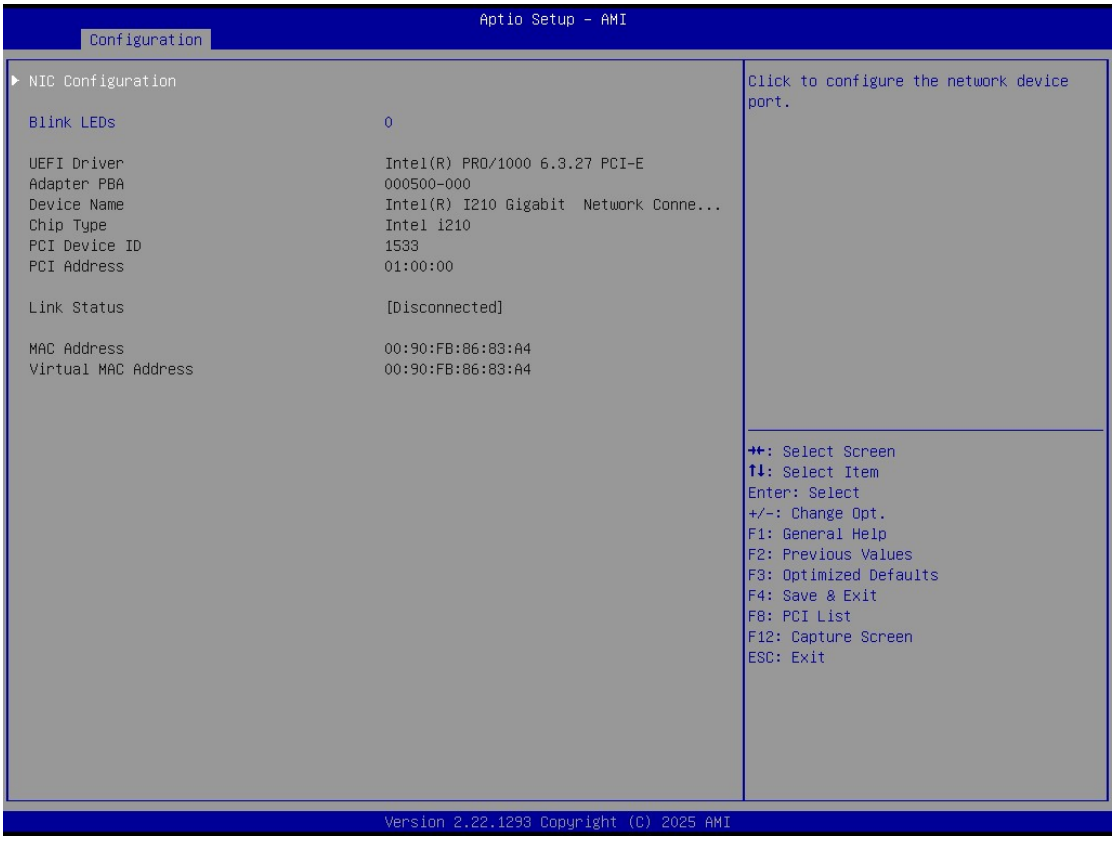
The settings specify how the host computer and the remote computer (which the user is using) will exchange data. Both computers should have the same or compatible settings.



Feature	Description	Options
Terminal Type	Emulation: ANSI: Extended ASCII char set. VT100: ASCII char set. VT100Plus: Extends VT100 to support color, function keys, etc. VT-UTF8: Uses UTF8 encoding to map Unicode chars onto 1 or more bytes.	★VT100Plus, ANSI, VT100, VT-UTF8
Bits per second	Select Serial port transmission speed. The speed must be matched on other side. Long or noisy lines may require lower speeds.	★115200, 9600, 19200, 38400, 57600
Data bits	Data bits	★8, 7

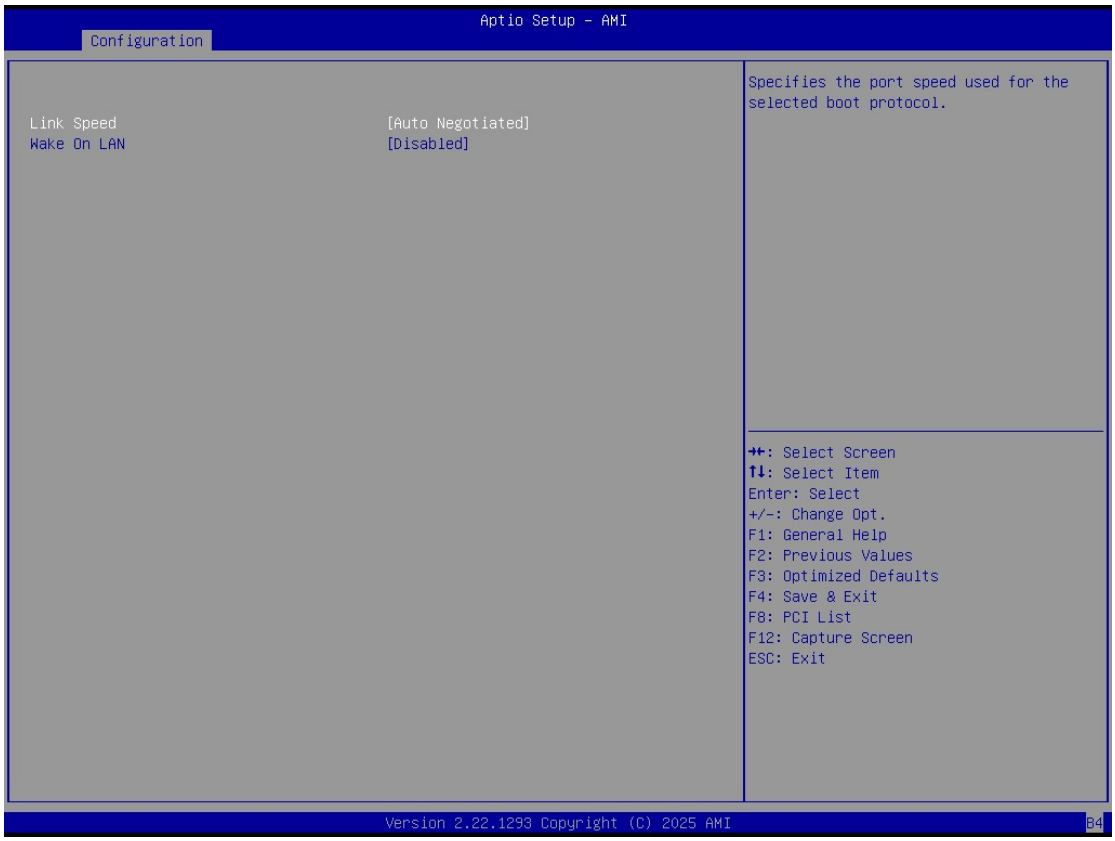
Feature	Description	Options
Parity	A parity bit can be sent with the data bits to detect some transmission errors. Even: parity bit is 0 if the num of 1's in the data bits is even. Odd: parity bit is 0 if num of 1's in the data bits is odd. Mark: parity bit is always 1. Space parity bit is always 0. Mark and Space Parity do not allow for error detection. They can be used as an additional data bit.	★None, Even, Odd, Mark, Space
Stop Bits	Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may require more than 1 stop bit.	★1,2
Flow Control	Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signals.	★None, Hardware RTS/CTS
VT-UTF8 Combo Key Support	Enable VT-UTF8 Combination Key Support for ANSI/VT100 terminals	Disabled, ★Enabled
Recorder Mode	With this mode enabled only text will be sent. This is to capture Terminal data.	★Disabled, Enabled
Resolution 100x31	Enables or disables extended terminal resolution	★Disabled, Enabled
Putty KeyPad	Select FunctionKey and KeyPad on Putty	★VT100, LINUX, XTERMR6, SCO, ESCN, VT400

6.3.13 6.3.13 Intel (R) I210 Gigabit Network Controller – 00:90:FB:86:83:A4



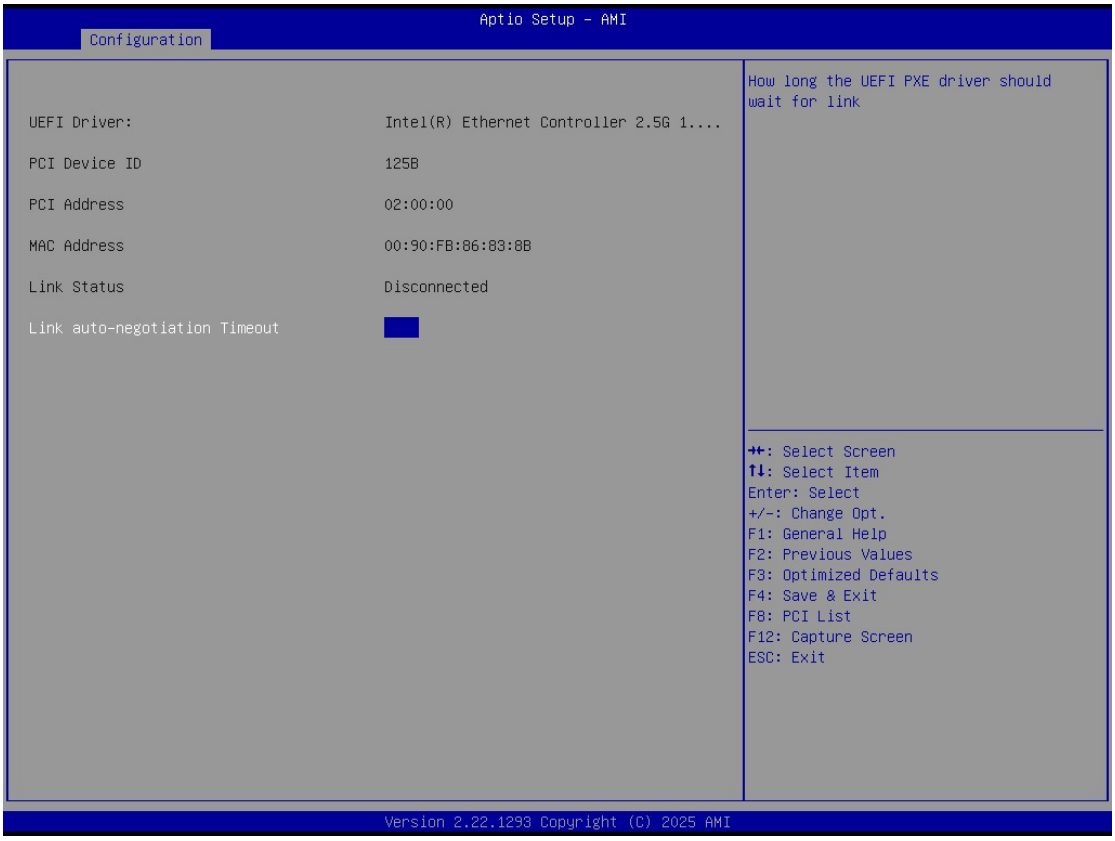
Feature	Description	Options
Blink LEDs	Identify the physical network port by blinking the associated LED.	★0

NIC Configuration



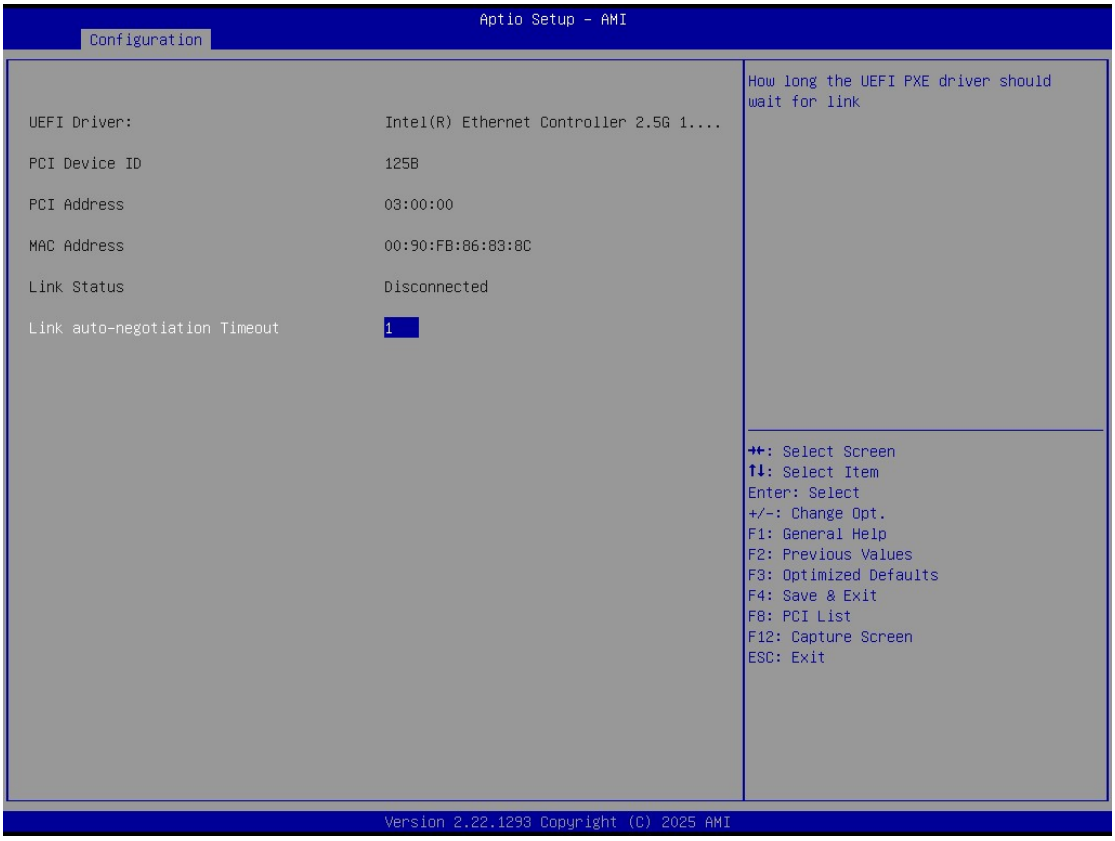
Feature	Description	Options
Link Speed	Specifies the port speed used for the selected boot protocol.	★Auto Negotiated, 10 Mbps Half 10 Mbps Full 100 Mbps Half 100 Mbps Full
Wake On LAN	Enables the server to be powered on using an in-band magic packet.	★Disabled, Enabled

6.3.14 6.3.14 Intel (R) Ethernet Controller I226-LM -- 00:90:FB:86:83:8B



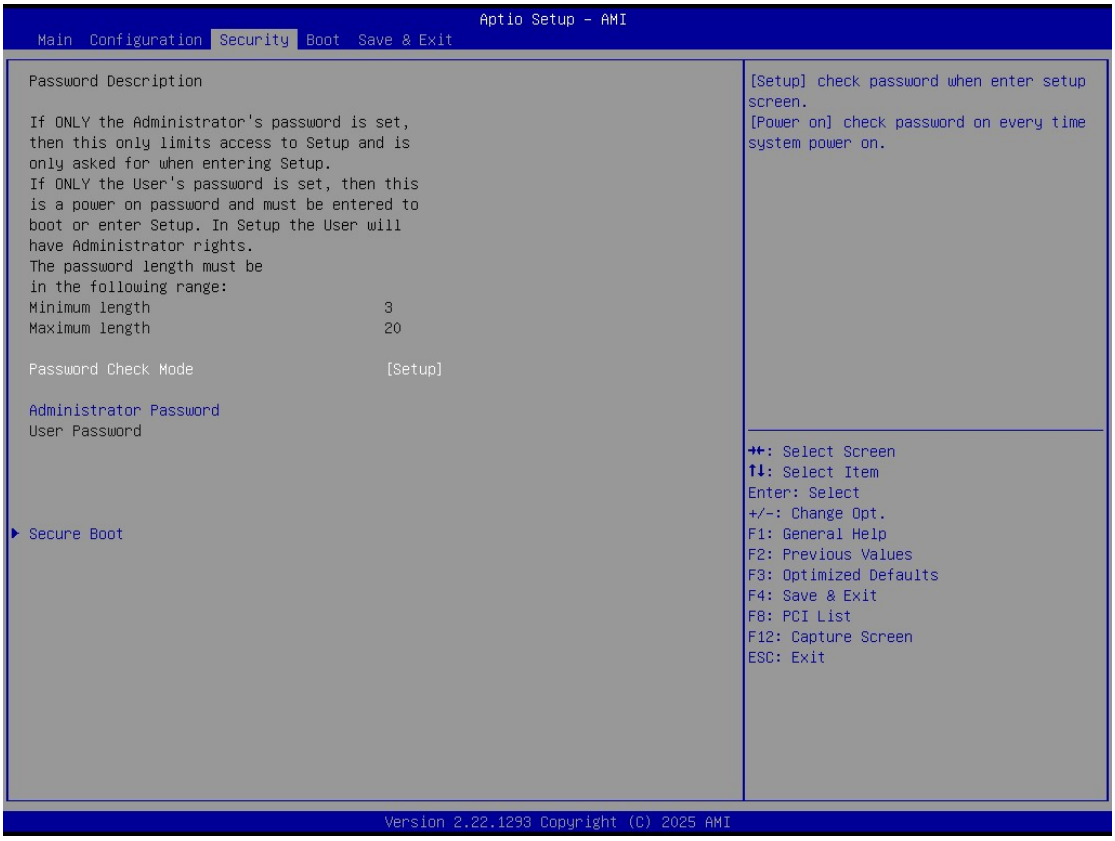
Feature	Description	Options
Link auto-negotiation Timeout	How long the UEFI PXE driver should wait for link.	★8

6.3.15 6.3.15 Intel (R) Ethernet Controller I226-LM -- 00:90:FB:86:83:8C



Feature	Description	Options
Link auto-negotiation Timeout	How long the UEFI PXE driver should wait for link.	★8

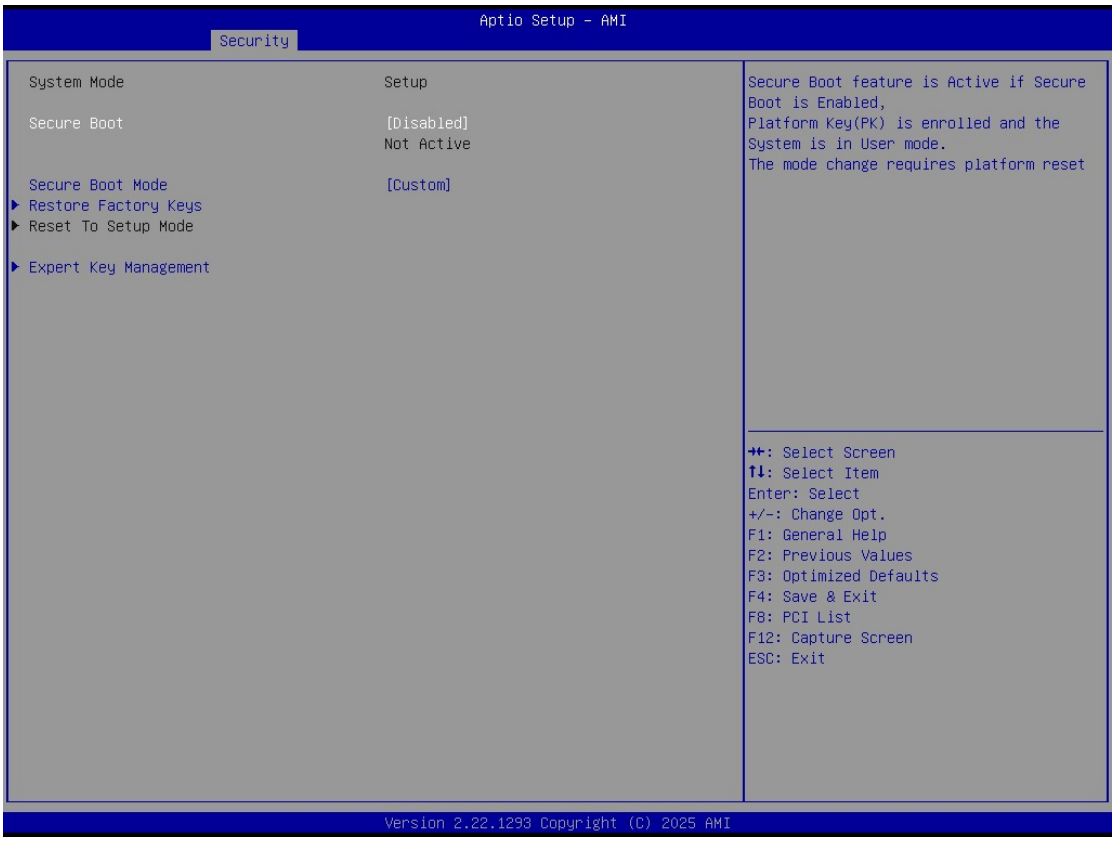
6.4 Security



Feature	Description	Options
Password Check Mode	[Setup] check password when enter setup screen. [Power on] check password on every time system power on.	★Setup, Power On
Administrator Password	Set Administrator Password	
Secure Boot	Secure Boot configuration	

Secure Boot

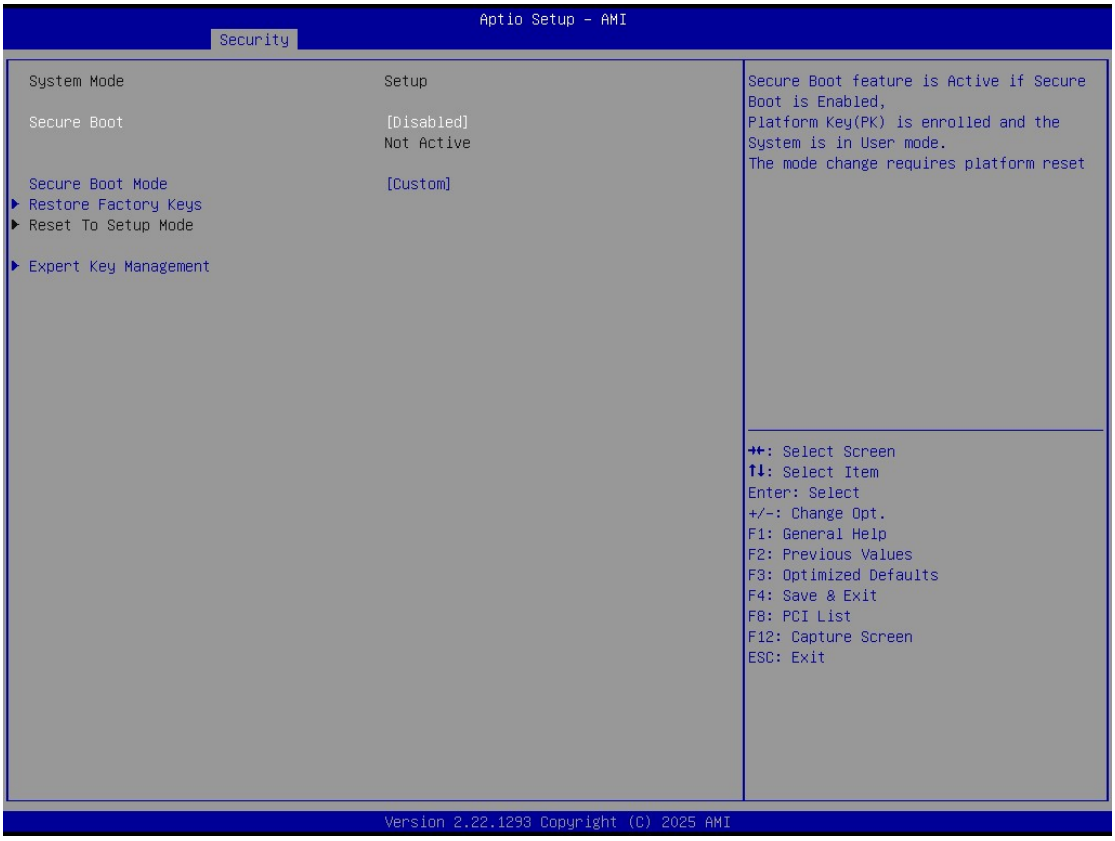
Secure Boot configuration



Feature	Description	Options
Secure Boot	Secure Boot feature is Active if Secure Boot is Enabled, Platform Key (PK) is enrolled and the System is in User mode. The mode change requires platform reset.	★Disabled, Enabled
Secure Boot Mode	Secure Boot Mode options: Standard or Custom. In Custom mode, Secure Boot Policy variables can be configured by a physically present user without full authentication	★Custom, Standard
Restore Factory keys	Force System to User Mode. Install factory default Secure Boot key databases	Yes, No
Key Management	Enables expert users to modify Secure Boot Policy variables without variable authentication	

Key Management

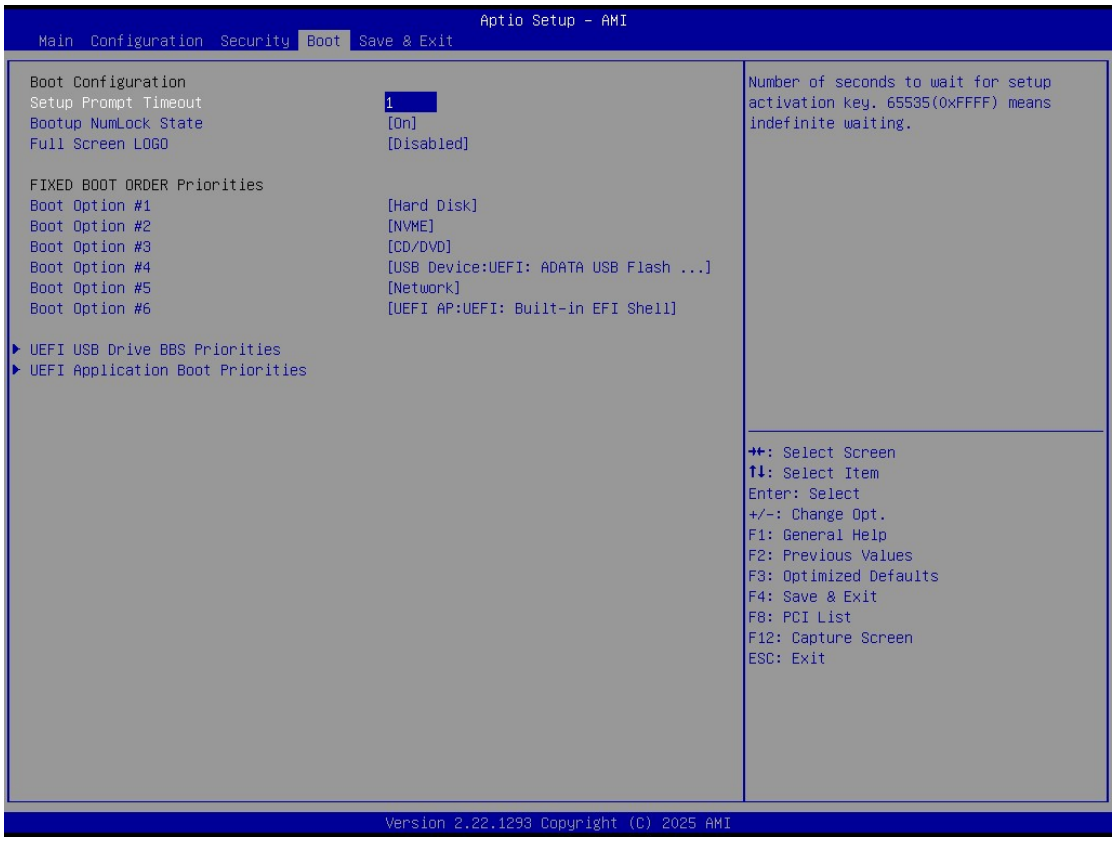
Enables expert users to modify Secure Boot Policy variables without variable authentication



Feature	Description	Options
Factory keys Provision	Install factory default Secure Boot key after the platform reset and while the System is in Setup mode.	★Disabled, Enabled
Restore Factory keys	Force System to User Mode. Install factory default Secure Boot key databases	Yes, No
Enroll Efi Image	Allow Efi image to run in Secure Boot mode. Enroll SHA256 Hash certificate of a PE image into Authorized Signature Database (db)	

Feature	Description	Options
Platform Key(PK)	Enroll Factory Defaults or load certificates from a file: 1.Public Key Certificate: a)EFI_SIGNATURE_LIST b) EFI_CERT_X509 (DER) c) EFI_CERT_RSA2048 (bin) d)EFI_CERT_SHAXXX 2.Authenticated UEFI Variable 3.EFI PE/COFF Image(SHA256) Key Source: Factory, Modified, Mixed	Update
Key Exchange Keys(KEK)		Update, Append
Authorized Signatures (db)		Update, Append
Forbidden Signatures (dbx)		Update, Append
Authorized TimeStamps (dbt)		Update, Append
OsRecovery Signatures (dbr)		Update, Append

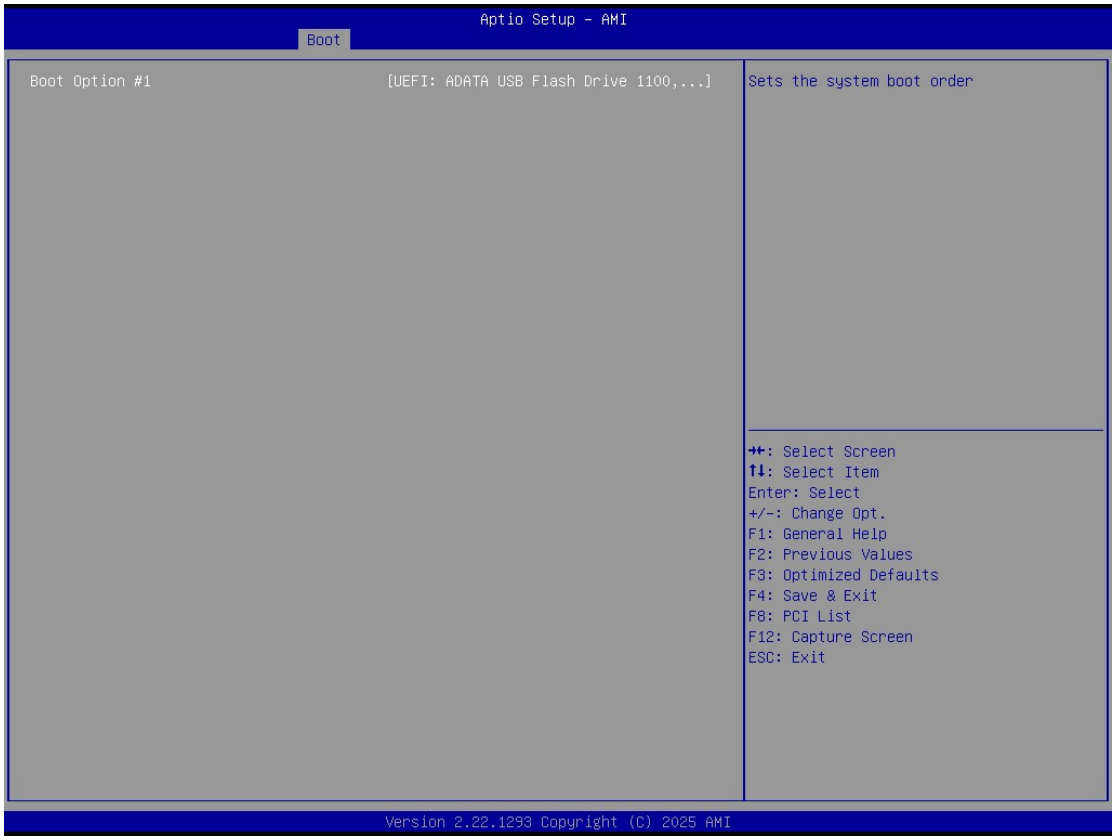
6.5 Boot



Feature	Description	Options
Setup Prompt Timeout	Number of seconds to wait for setup activation key. 65535(0xFFFF) means indefinite waiting.	★1
Bootup NumLock State	Select the keyboard NumLock state.	★On, Off
Full Screen LOGO	Enables or disables Quiet Boot option and Full screen Logo.	★Disabled, Enabled
Boot Option #1 ~ #6	Sets the system boot order	Hard Disk, NVME, CD/DVD, USB Device, Network, UEFI AP: UEFI: Built-in EFI Shell, Disabled
UEFI USB Drive BBS Priorities	Specifies the Boot Device Priority sequence from available UEFI USB Drive	
UEFI Application Boot Priorities	Specifies the Boot Device Priority sequence from available UEFI Application	

UEFI USB Drive BBS Priorities:

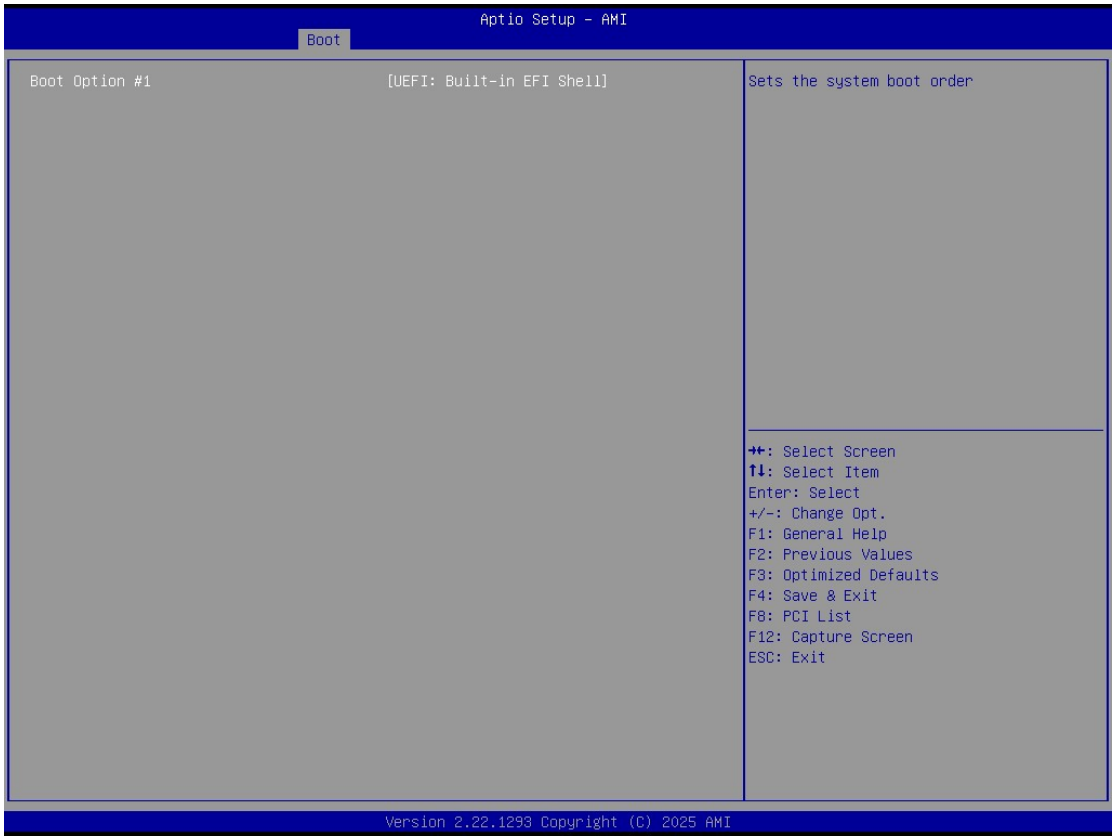
Specifies the Boot Device Priority sequence from available UEFI Hard Drive Application.



Feature	Description	Options
Boot Option #1	Sets the system boot order.	

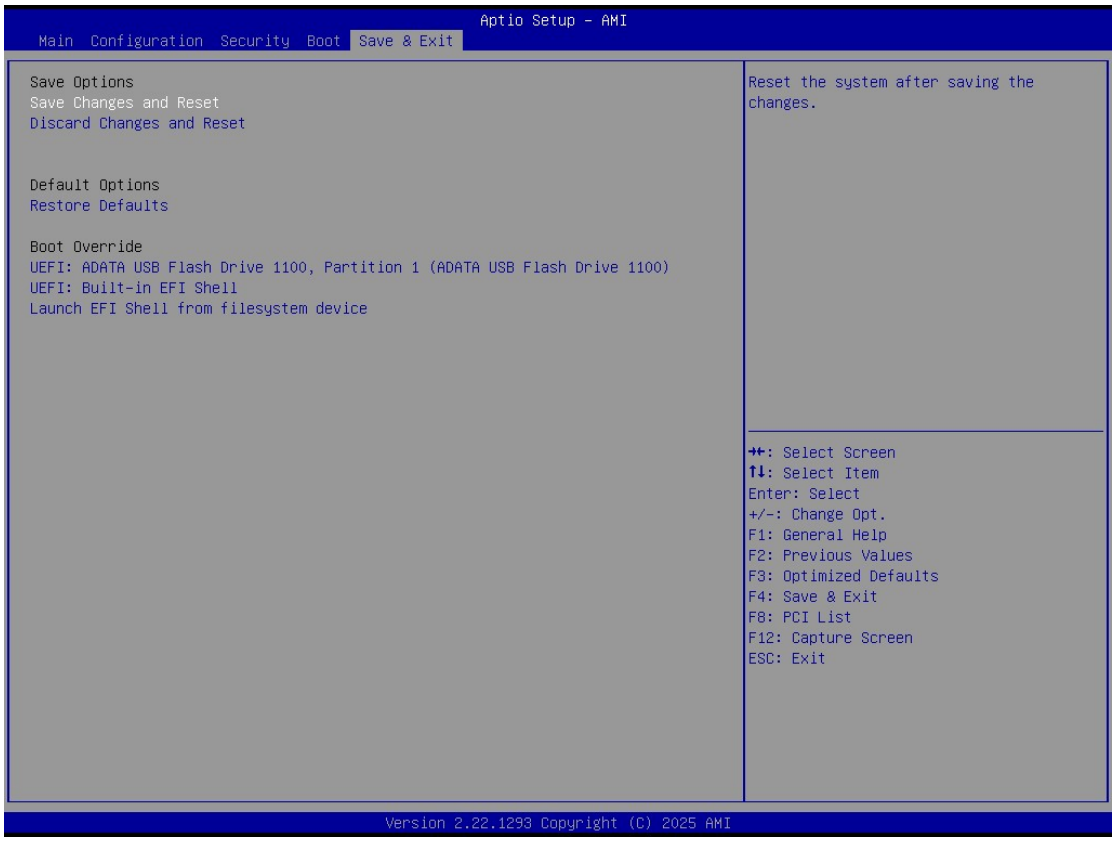
UEFI Application Boot Priorities:

Specifies the Boot Device Priority sequence from available UEFI Application.



Feature	Description	Options
Boot Option #1	Sets the system boot order.	

6.6 Save& Exit



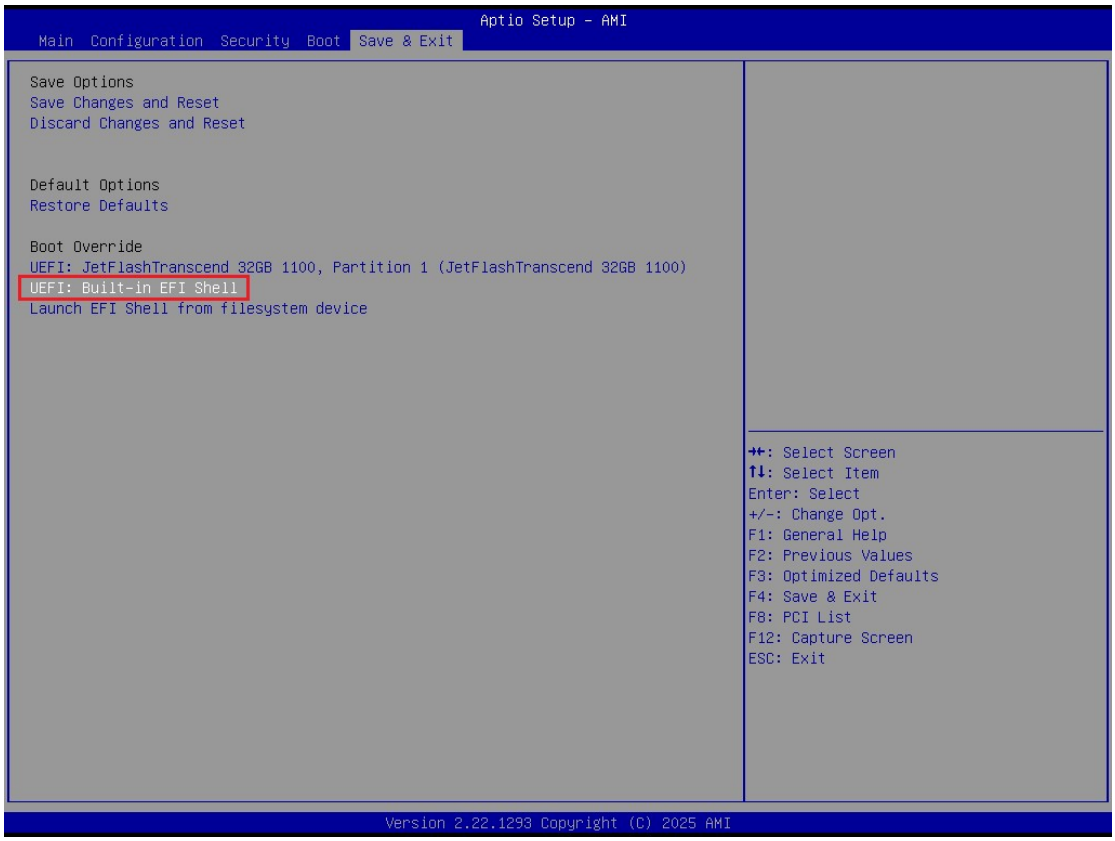
Feature	Description	Options
Save Changes and Reset	Reset the system after saving the changes.	
Discard Changes and Reset	Reset system setup without saving any changes.	
Restore Defaults	Restore/Load Default values for all the setup options.	
UEFI: Built-in EFI Shell		
Launch EFI Shell from filesystem device	Attempts to Launch EFI Shell application (Shell.efi) from one of the available filesystem devices.	

PEB-2775 BIOS/EC UEFI Update SOP process under UEFI Shell

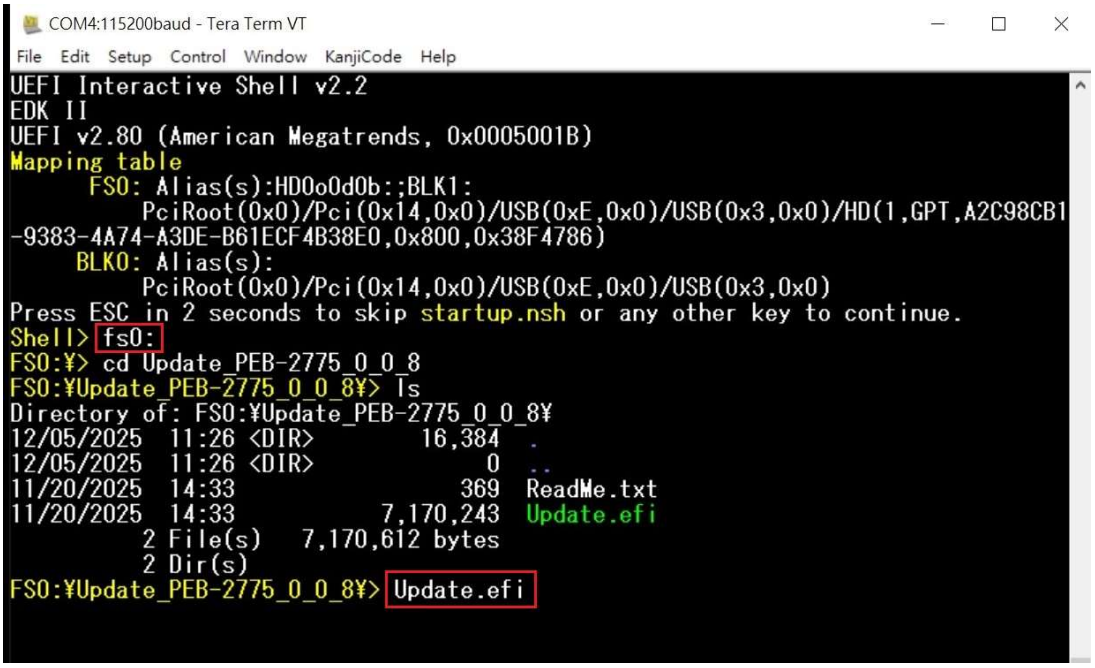
Step1. Prepare a USB DOK.

Step2. Unzip BIOS update file to the USB DOK.

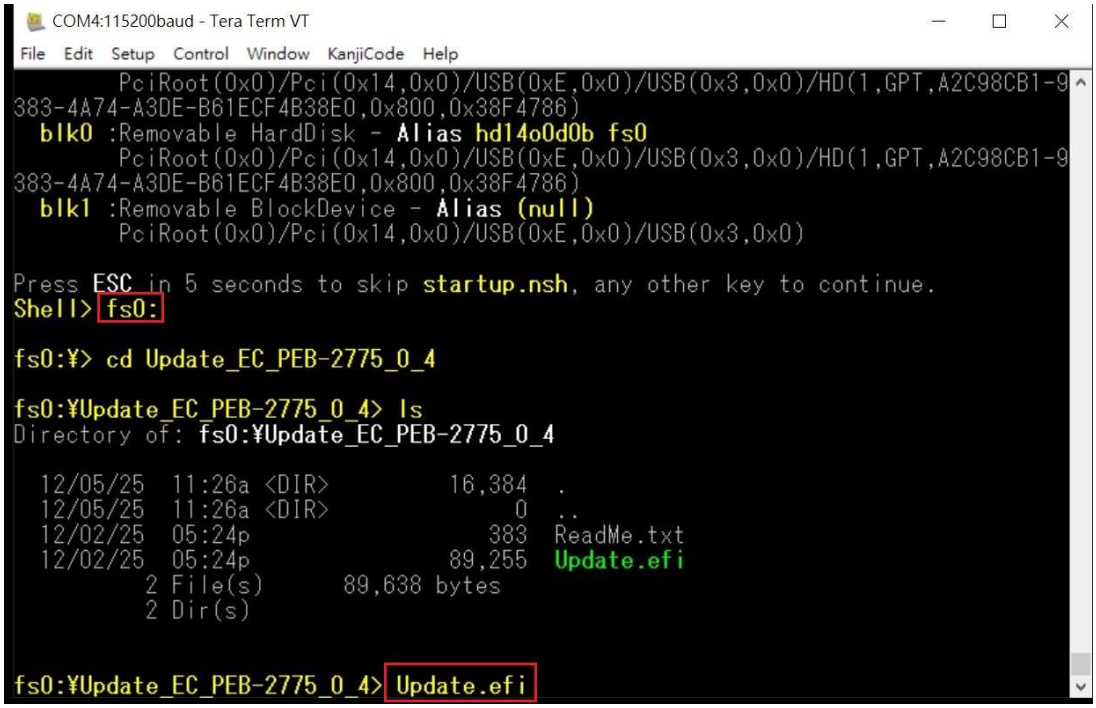
Step3. Plug the USB DOK into the target system and then boot in UEFI Shell By selecting UEFI: Built-In EFI shell in the BIOS save & Exit page.



Step 4. Under the UEFI shell, direct to your USB DOK, below picture is an example using fs0. Then direct to the folder with BIOS updated file and then enter command: "Update.efi" to start updating BIOS or EC.



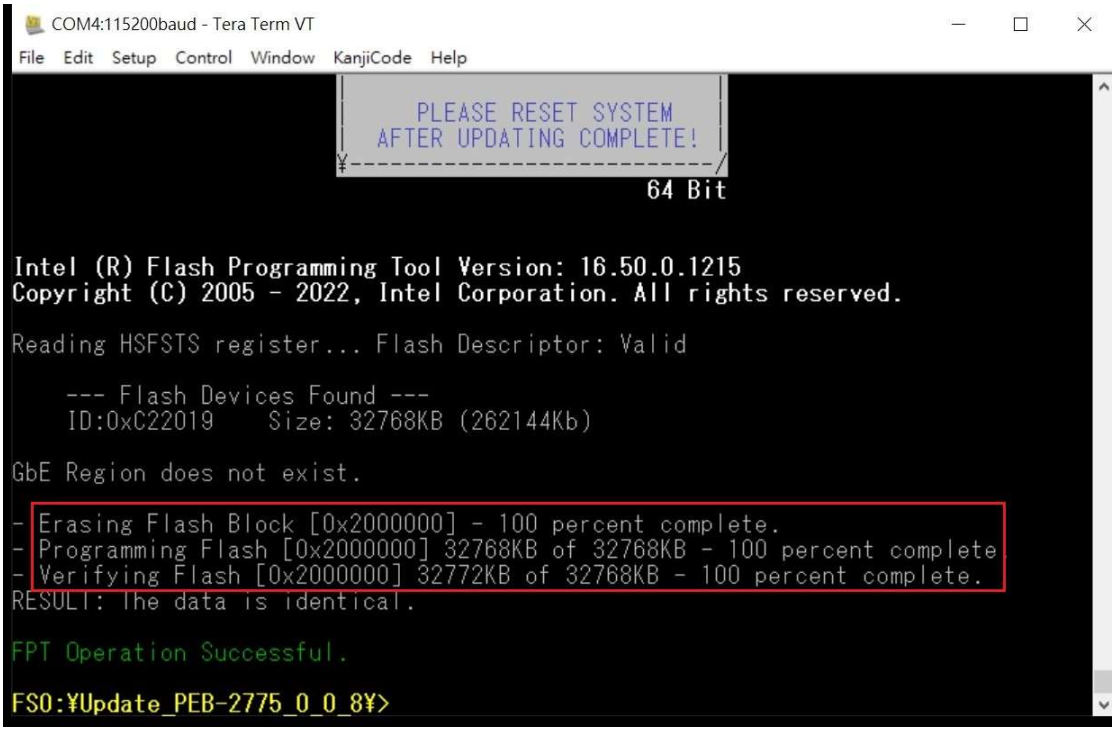
(BIOS File Update)



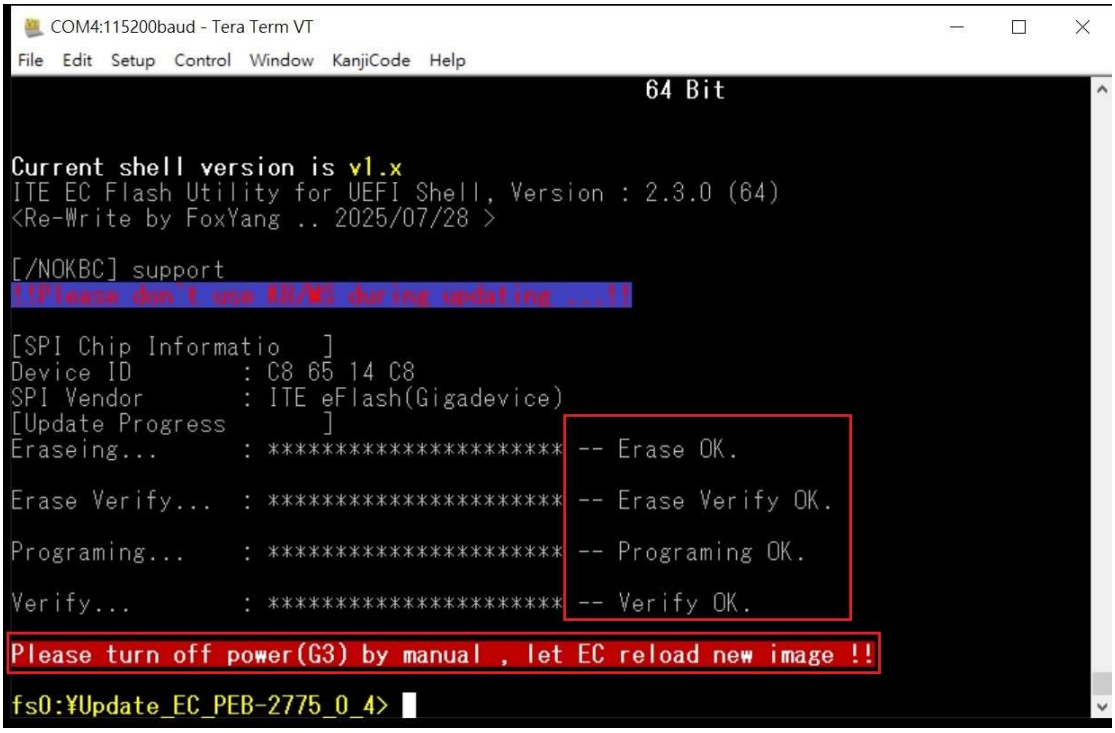
(EC File Update)

Step 5. The updating process will start and you can see the updating progress. When you see the following pictures, which means the BIOS / EC update processes finished.

Please cut the AC power off and wait for 10 seconds before powering on.



(BIOS update finished)



(EC update finished)

Chapter 7

System Overview

7 System Resources
7.1 Intel Twin Lake SoC
7.2 Main Memory
7.3 Installing the Single Board Computer

7. System Resources

7.1 Intel® Twin Lake & Amston Lake Soc

Intel® Processor N150 (4C, 0.8GHz, 6W)

Intel® Processor N355 (8C, 1.8GHz, 9/15W)

Intel® Atom x7433RE (4C, 1.5GHz, 9W)

7.2 Main Memory

PEB-2775 provides 1x 262-pin SO-DIMM sockets which supports DDR5 non-ECC memory. The maximum memory can be up to 16GB. Memory clock and related settings can be detected by BIOS via SPD interface.

7.3 Installing the Single Board Computer

To install your PEB-2775 into standard chassis or proprietary environment, please perform the following:

Step 1 : Check all jumpers setting on proper position

Step 2 : Install and configure memory module on right position

Step 3 : Place PEB-2775 into the dedicated position in the system

Step 4 : Attach cables to existing peripheral devices and secure it

WARNING

Please ensure that motherboard is properly inserted and fixed by mechanism.

Chapter 8

System Overview

8 Troubleshooting
8.1 Hardware Quick Installation
8.2 BIOS Setting
8.3 FAQ

8. Troubleshooting

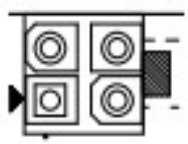
This chapter provides a few useful tips to quickly get PEB-2775 running with success.

8.1 Hardware Quick Installation

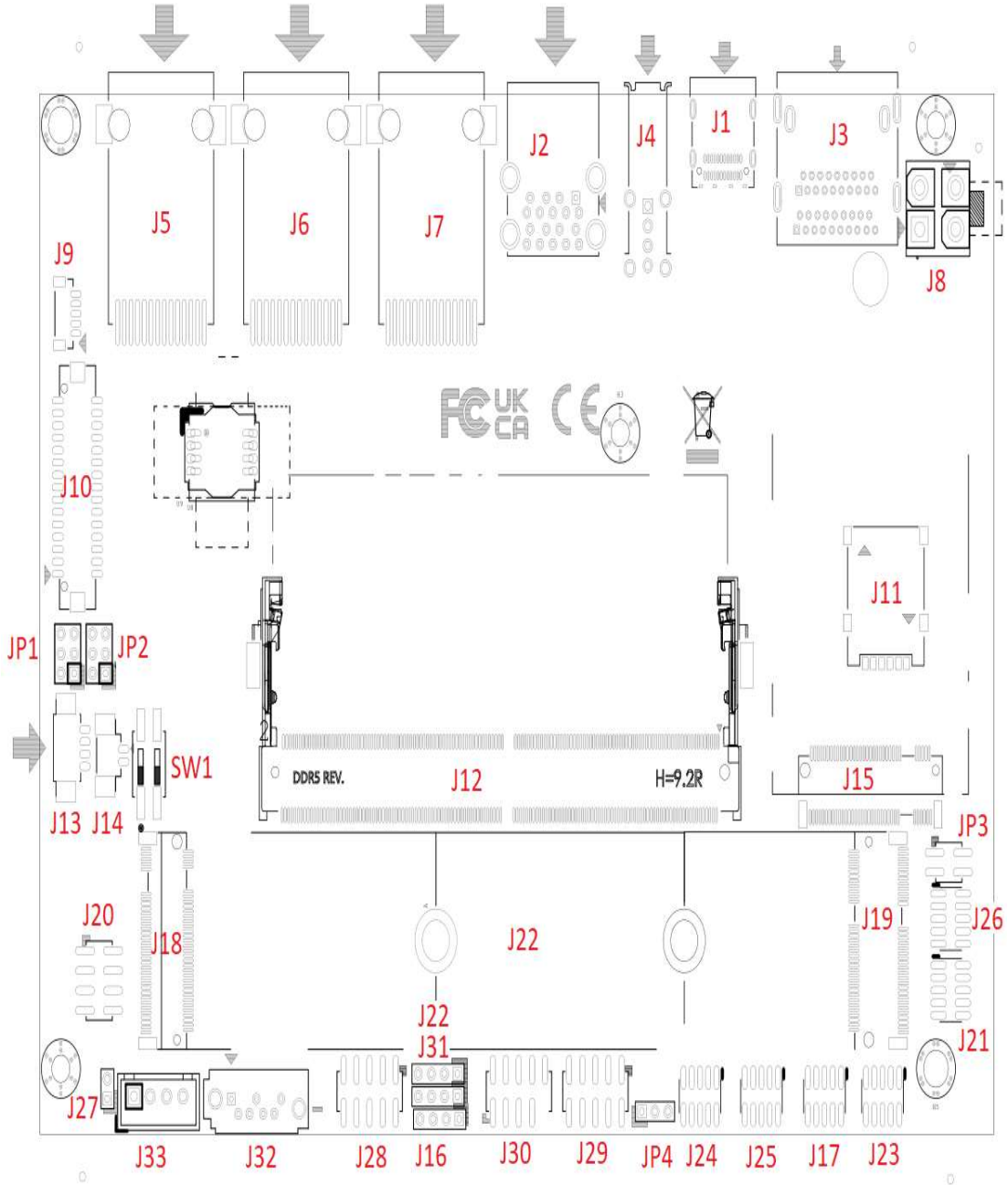
DC Jack Power

PEB-2775 is powered via a ATX 4pin connector, supporting a wide input voltage range from 9V to 36V.

J8 : 4-PIN ATX Power(Support DC 9~36V)

PCB Footprint	Pin No.	Signal Description
	1	GND
	2	GND
	3	DC-IN(9~36V)
	4	DC-IN(9~36V)

Connector


J1
J2
J3
J4
J5
J6
J7
J8
J9
J10
J11
J12
J13
J14
J15
J16
J18
J19
J20
J21
J22
J23
J24
J25
J26
J27
J28
J29
J30
J31
J32
J33
JP1
JP2
JP3
JP4
SW1
DDR5 REV.
H=9.2R

8.2 BIOS Setting

It is assumed that users have correctly adopted modules and connected all the devices cables required before turning on DC power.

262-pin DDR5 4800MT/s SO-DIMM Memory, keyboard, mouse, M.2 M-key storage, HDMI connector, device power cables, DC jack accessories are good examples that deserve attention. With no assurance of properly and correctly accommodating these modules and devices, it is very possible to encounter system failures that result in malfunction of any device.

To make sure that you have a successful start with PEB-2775, it is recommended, when going with the boot-up sequence, to hit “DEL” and ”ESC” key and enter the BIOS

setup menu to tune up a stable BIOS configuration so that you can wake up your system far well.

Loading the default optimal setting

When prompted with the main setup menu, please scroll down to “RestoreDefaults”, press “Enter” and select “Yes” to load default optimal BIOS setup.

This will force your BIOS setting back to the initial factory configurations. It is recommended to do this so you can be sure the system is running with the BIOS setting that Portwell has highly endorsed. As a matter of fact, users can load the default BIOS setting at any time when system appears to be unstable in boot up sequence.

8.3 FAQ

Information & Support

● Question: I forgot my password for system BIOS, what am I supposed to do?

Answer: You can switch off your power supply then find the RTC Battery on PEB-2775. Then remove the RTC battery and wait 5 seconds to clean your password then to switch on your power supply.

● Question: How to update the BIOS file of PEB-2775?

Answer:

1. Please visit the web site of Portwell download center as below hyperlink https://download.portwell.tw/
2. Select “Search download” and type the keyword “PEB-2775”.
3. Find the “BIOS “page and download the ROM file and flash utility.
4. Unzip file to bootable USB flash drive which can boot to shell mode. Then execute the “update.efi”. It will start to update BIOS.
5. When you see the “FPT Operation Passed” message, which means the BIOS update processes finished. Please cut the AC power off and wait for 10 seconds before powering on.
6. If you have other additional technical information or requests which are not covered in this manual, please fill in the technical request form as below hyperlink. https://www.portwell.com.tw/support-center/service-request/
We will do our best to provide a suggestion or solution for you.

Chapter 9

System Overview

9 Portwell Software Service

9. Portwell Software Service

1. If you have customized requirements of BIOS, you can contact people from our company or branch.
2. If you have requirements of WDT、GPIO APP、OOB GUI, you can contact our headquarter or branch, and we can render your assistance on developing.
https://www.portwell.com.tw/portwell-worldwide/

Portwell

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