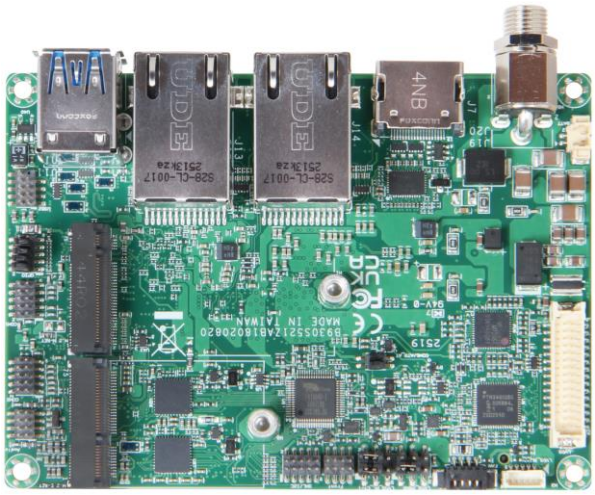
Portwell



PICO-8020 Series

PICO-ITX Embedded Board

User Manual

Version R 1.2

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Revision History

R 1.0	Official Release Rev. 1.0
R 1.1	Updated JP3 information in Section 4.2 (Jumper Setting List)
R1.2	1. Add a warning regarding thermal kit usage in Section 2 (Specifications) and Section 2.4 (Environmental Specifications) 2. Modify the motherboard installation steps and recommend using a thermal kit in Section 7.3 (Installing the Single Board Computer)

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Chapter 1

System Overview

1 Introduction

1. Introduction

The PICO-8020 is a high-performance, ultra-compact fanless SBC based on the PICO-ITX form factor, featuring Intel® Twin Lake and Amston Lake processors-including Intel® Processor N150 and Atom® x7433RE/x7211RE. It delivers exceptional computing and graphics capabilities while maintaining low power consumption, making it ideal for space-constrained edge applications.

Designed with versatility in mind, the PICO-8020 supports one DDR5 SO-DIMM socket (up to 16GB), one M.2 E-Key (2230) for wireless modules, and one M.2 M-Key (2242) for PCIe/SATA storage. It features Intel® Gen12 UHD Graphics with up to 32 EUs, supporting dual independent displays via HDMI 2.0 and LVDS.

I/O-rich and robust, the board offers dual Intel® GbE LAN, dual USB 3.2 Gen2 ports, dual USB 2.0 headers, dual RS-232/422/485, audio I/O, GPIO, I2C, SMBus, and onboard TPM 2.0. Its wide operating temperature range (up to -40° C to 85° C for industrial SKUs) and 12~24V DC input ensure reliability in harsh environments.

Whether used in industrial automation (e.g. vision systems, HMI panels), medical equipment (e.g. diagnostic imaging, patient monitoring), or IoT gateway applications, the PICO-8020 empowers developers to build reliable, intelligent, and connected systems.

Chapter 2

System Overview

2 Specifications
2.1 Supported Operating Systems
2.2 Mechanical Dimensions
2.3 Power Consumption
2.4 Environmental Specifications

2. Specifications

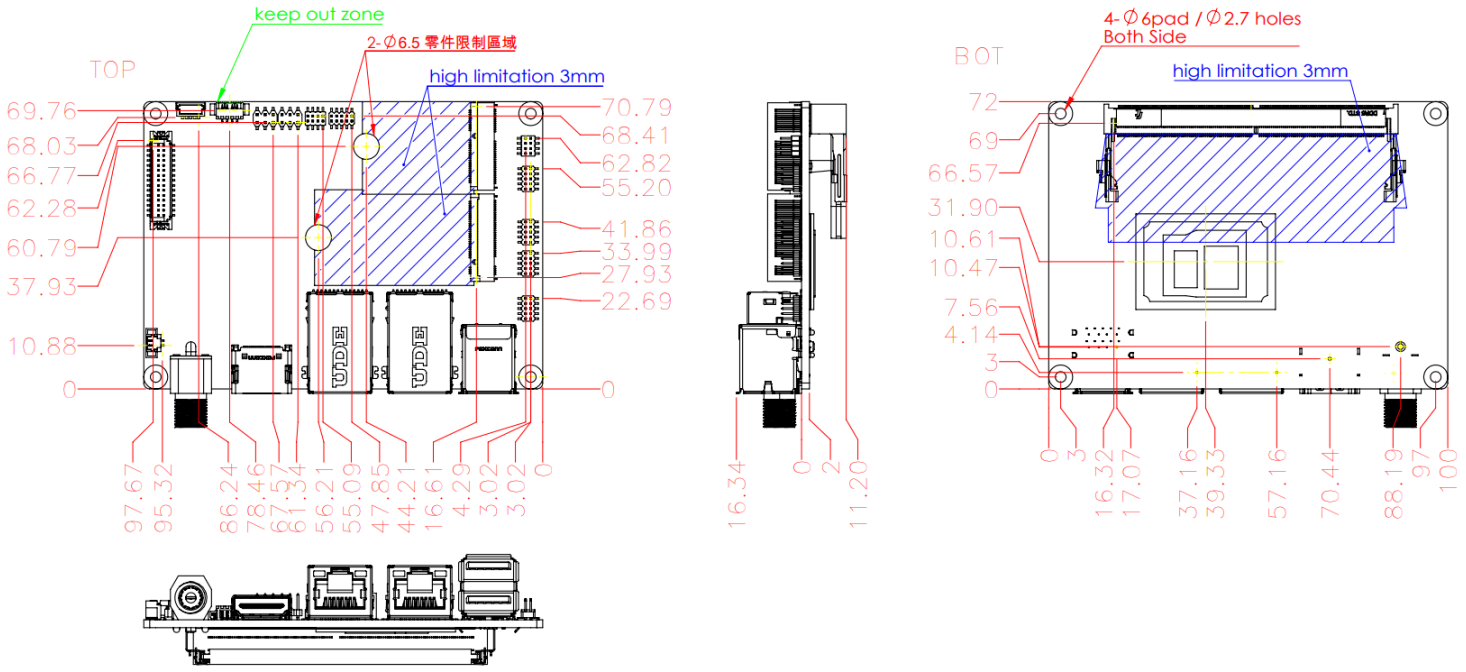
Main Processor	Intel® Processor N150 Intel® Atom x7433RE Intel® Atom x7211RE
System BIOS	AMI UEFI BIOS
Main Memory	1x non-ECC DDR5 4800MT/s SO-DIMM up to 16GB 1DPC, 1-channel
Graphics	Intel® Graphics Gen12 with up to 24 EUs HDMI: 1x HDMI port on rear I/O (HDMI 2.0, 3840x2160 @ 60Hz) LVDS: 1x LVDS on board connector (Dual channel, 24bit, 1920x1200 @60Hz)
Expansion Interface	1x M.2 E key 2230
Storage Interface	1x M.2 M key 2242
Input/Output	Serial Port: 2x RS-232/422/485 port 2x USB 3.2 Gen2 on rear I/O, 2x USB 2.0 on board pin header Audio Interface: line-in, line-out, mic-in on board pin header 1x SMbus & 1x I2C on board pin heade 1x 4-pin smart fan header
Ethernet	2x Intel® GbE Controller(I210) 2x RJ45 connectors on rear I/O
High Drive GPIO	1x pin-header for GPIO(8bit)
Mechanical and environmental specifications	Operating temperature: 0 ~ 60° C (Twin Lake)/ -40 to +85° C (Asmton Lake) Storage temperature: -40 ~ 85° C Humidity: 5 ~ 95% non-condensing Power supply voltage: 12 ~24V DC jack on rear I/O (Colay 2-pin terminal blocks) Board size: 100mm x 72 mm (3.94" x 2.83") **※Please be sure to use active or passive heat dissipation equipment**
Certification	CE/FCC

2.1 Supported Operating Systems

The PICO-8020 supports the following operating systems.

	Windows IoT Enterprise	Ubuntu
Twin Lake	Windows 11 LTSC (24H2)	24.04
Amston Lake	Windows 10 LTSC (21H2) Windows 11 LTSC (24H2)	22.04/24.04

2.2 Mechanical Dimensions



2.3 Power Consumption

Test Configuration	
CPU Type	Intel® Atom™ x7433RE 1.5GHz,L3:6M
SBC BIOS	Portwell BIOS Version : 0.0.6
Memory	Innodisk DDR5 4800 SODIMM 16GB
Graphic Card	Intel® UHD Graphics
Graphic Driver	Intel® UHD Graphics,Driver Version:32.0.101.6737
LAN Card #1	Intel® I210 Gigabit Network Connection
LAN Driver #1	Intel® I210 Gigabit Network Connection,Driver Version:12.18.11.1

LAN Card #2	Intel® I210 Gigabit Network Connection#2
LAN Driver #2	Intel® I210 Gigabit Network Connection#2,Driver Version:12.18.11.1
Audio Card	High Definition Audio Device
Audio Driver	High Definition Audio Device,Driver Version:10.0.26100.3624
Chip Driver	Intel® Chipset Device Software,Version:10.1.19899.8597
USB 2.0 Driver	USB Composite Device,Driver Version:10.0.26100.3912
USB 3.0 Driver	Intel® USB 3.10 eXtensible Host Controller – 1.20 (Micrsoft),Driver Version:10.0.26100.4202
OS Edition	Win11 24H2
Hard Drive	WARIS M.2 256GB
Power Supply	FSP060-DBAB1
Boot Mode Select	UEFI

Power consumption(12V)

Item	*Power ON*	*Full Loading 10mins*
DC in (+12V)	1.55A	1.666A

USB Port and the Spec.	*Result*
USB 3.2 Gen1 Port J11	4.86 V/ 1.04 A
USB 3.2 Gen1 Port J11	4.86 V/ 1.1 A
USB 2.0 Port J12	4.86 V/ 0.49 A
USB 2.0 Port J12	4.86 V/ 0.51 A
Full USB port Loading Test (x4)	USB 3.2 Gen2 Port J11 ： 4.84 V/ 0.99 A USB 2.0 Port J12 ： 4.77 V/ 0.46 A

Item	*S0*	*S3*	*S4*	*S5*
DC in (+12V)	0.86A	0.37A	0.349A	0.349A

2.4 Environmental Specifications

Storage Temperature : 0 ~ 60° C (Twin Lake)/ -40 to +85° C (Asmton Lake)

Operation Temperature : 0~60° C

Storage Humidity : 5~95%, non-condensing

Operation Humidity: 5~95%, non-condensing

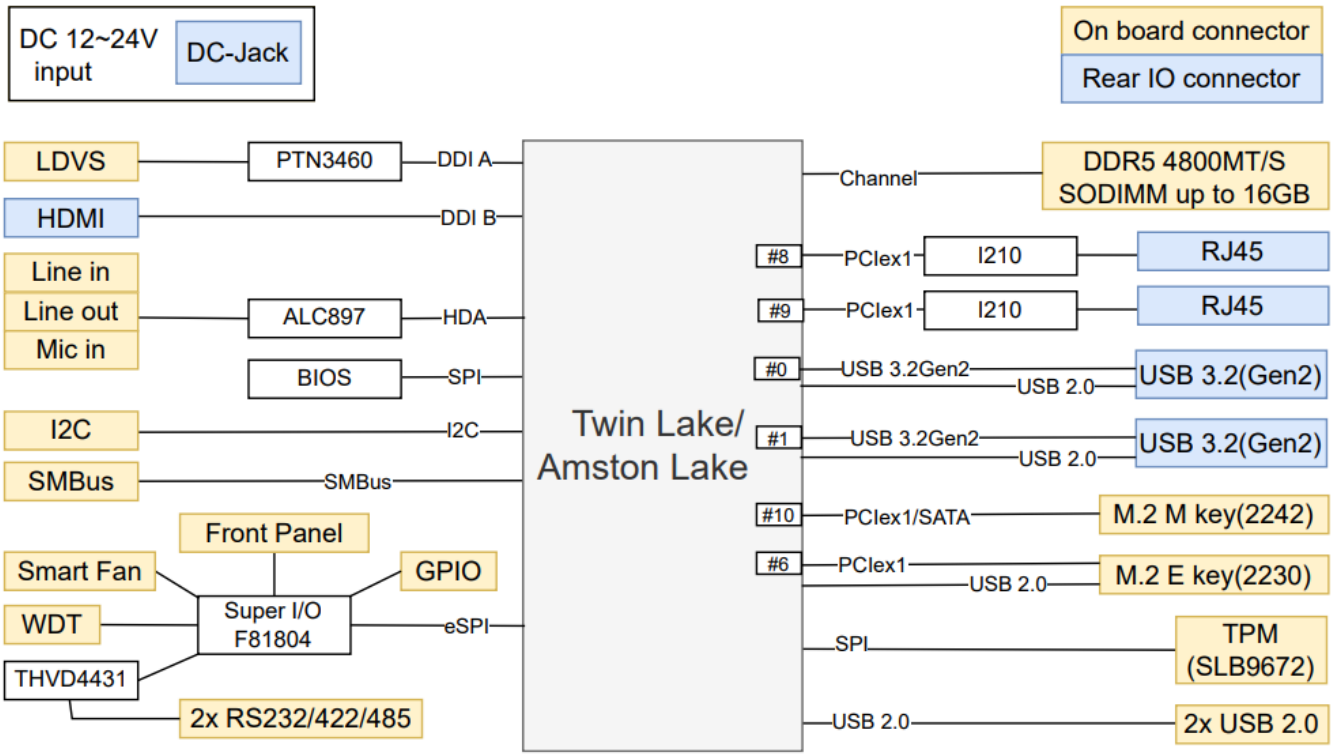
※Please be sure to use active or passive heat dissipation equipment

Chapter 3

System Overview

3 Block Diagram

3. Block Diagram



Chapter 4

System Overview

4 Hardware Configuration
4.1 Drawing Overview
4.2 Jumper Setting List
4.3 Connector Function List

4. Hardware Configuration

This chapter indicates jumpers、headers, and connectors' locations. Users may find useful information related to hardware settings in this chapter.

4.1 Drawing Overview

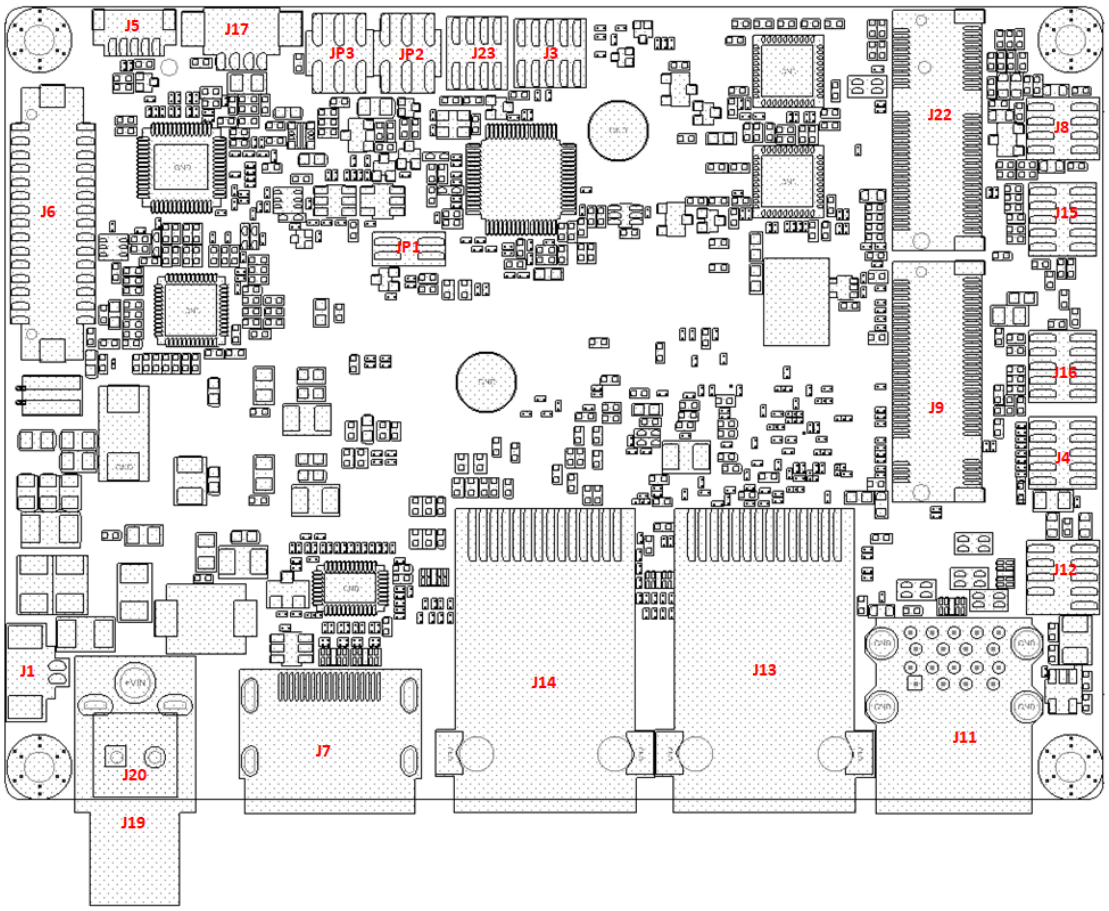


Figure1. PICO-8020 Top View

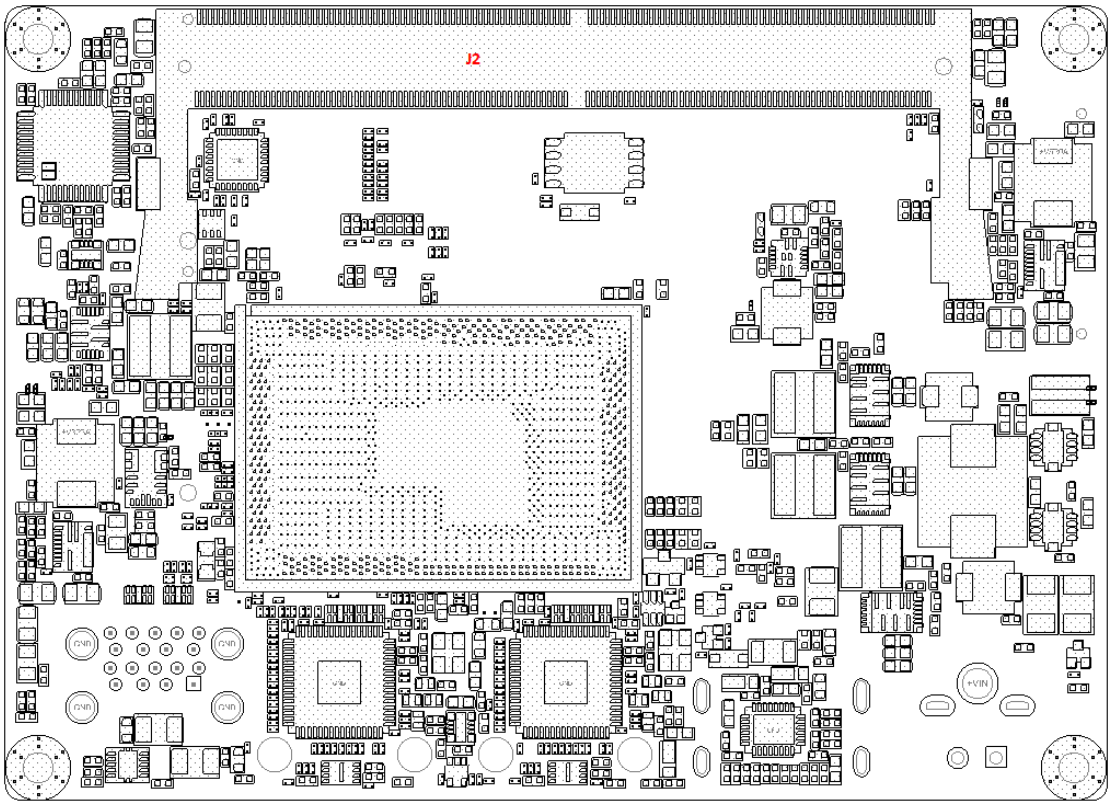


Figure1. PICO-8020 Bot View

4.2 Jumper Setting List

For users to customize PICO-8020 features. In the following sections, Short means covering a jumper cap over jumper pins; Open or N/C (Not Connected) means removing a jumper cap from jumper pins. Users can refer to Figure 1 for the Jumper allocations.

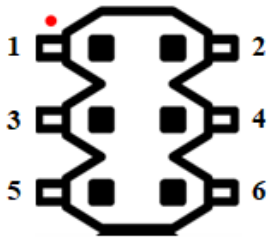
Jump Function List:

Location	Connector	Function
JP1	Pin Header 2Px2 P=1.27mm 180D	Clear CMOS Jumper & AT & ATX mode
JP2	Pin Header 3Px2 P=2.0mm 180D	LVDS backlight Enable setting Jumper
JP3	Pin Header 3Px2 P=2.0mm 180D	LVDS VCC Selection Jumper(3.3V,5V,12V)

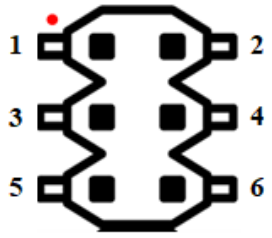
JP1: Clear CMOS Jumper & AT & ATX mode

PCB Footprint	Jumper Setting	Function Description
	Short 1-2	**Save CMOS (Default)**
	Short 2-3	Clear CMOS
	Open 3-4	ATX MODE
	Short 3-4	**AT MODE (Default)**

JP2: LVDS backlight Enable setting Jumper

PCB Footprint	Jumper Setting	Function Description
	**Short 1-3, 2-4**	**5V, Active High (Default)**
	Short 1-3, 4-6	12V, Active High
	Short 3-5, 2-4	5V, Active Low
	Short 3-5, 4-6	12V, Active Low

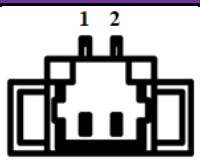
JP3: LVDS VCC Selection Jumper(3.3V,5V,12V)

PCB Footprint	Jumper Setting	Function Description
	**Short 1-3**	**3.3V (Default)**
	Short 5-3	5V
	Short 4-3	12V

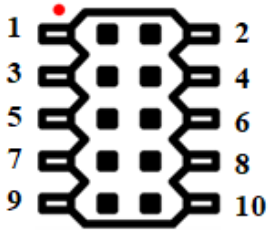
4.3 Connector Function List

Location	Connector	Function
J1	Wafer 2Px1 P=1.25mm	BATT Socket
J2	DDR5 SODIMM Socket262P	DDR5 SO-DIMM Socket
J3	Pin Header 5Px2 P=1.27mm 180D	SMBus/I2C
J4	Pin Header 5Px2 P=1.27mm 180D	GPIO*8
J5	Wafer 5Px1 P=1.0mm 180D	LVDS backlight Inverter
J6	Wafer 15Px2 P=1.25mm 180D	LVDS
J7	Wafer 4Px1/1.25mm/90D	HDMI
J8	Pin Header 4Px2 P=1.27mm 180D	Audio
J9	NGFF M.2 Key-M H=8.5mm	M.2 SSD_2242 for PCIEx1 or SATA
J11	USB3 x2 A-Type 90D	USB3 x 2
J12	Pin Header 5Px2(-9) P=1.27mm 180D	USB2 x 2
J13	RJ45	RJ45(1G)
J14	RJ45	RJ45(1G)
J15	Pin Header 5Px2 P=1.27mm 180D	COM2 RS232/RS422/RS485
J16	Pin Header 5Px2 P=1.27mm 180D	COM1 RS232/RS422/RS485
J17	Wafer 4Px1 P=1.25mm 90D	FAN
J20	Terminal Blocks. 2Px1 P=3.5mm	DC IN
J22	NGFF M2 KEY-E H=8.5mm	WiFi_2230
J23	Pin Header 4Px2 P=1.27mm 180D	Front Panel

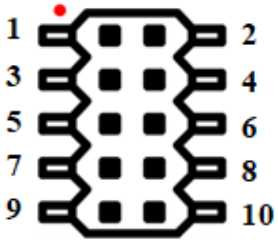
J1 : BATT Socket

PCB Footprint	Pin No.	Signal Description	Pin No.	Signal Description
	1	VBAT		
	2	GND		

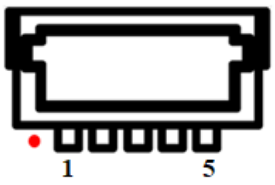
J3 : SMBus/I2C

PCB Footprint	Pin No.	Signal Description	Pin No.	Signal Description
	1	SMB_CLK	2	3.3V
	3	SMB_ALERT#	4	NC
	5	GND	6	I2C_CLK
	7	SMB_DATA	8	I2C _DATA
	9	3.3V	10	GND

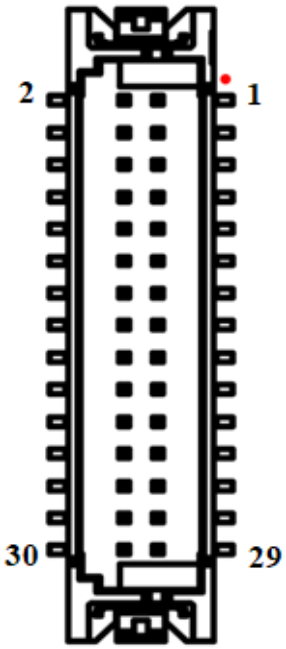
J4 : GPIO*8

PCB Footprint	Pin No.	Signal Description	Pin No.	Signal Description
	1	GPI0	2	GPO0
	3	GPI1	4	GPO1
	5	GPI2	6	GPO2
	7	GPI3	8	GPO3
	9	GND	10	3.3V

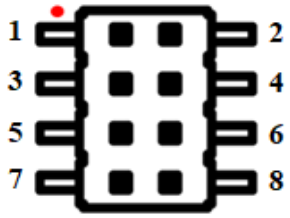
J5 : LVDS backlight Inverter

PCB Footprint	Pin No.	Signal Description	Pin No.	Signal Description
	1	5V	4	GND
	2	BKLT_CTRL	5	BKLT_EN
	3	12V		

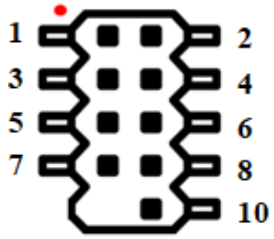
J6 : LVDS

PCB Footprint	Pin No.	Signal Description	Pin No.	Signal Description
	2	VDD	1	VDD
	4	LVDS0_CHA_TXN0	3	LVDS0_CHA_TXP0
	6	LVDS0_CHA_TXN1	5	LVDS0_CHA_TXP1
	8	LVDS0_CHA_TXN2	7	LVDS0_CHA_TXP2
	10	LVDS0_CHA_TXN3	9	LVDS0_CHA_TXP3
	12	LVDS0_CHA_CLKN	11	LVDS0_CHA_CLKP
	14	LVDS0_DDC_DATA	13	LVDS0_DDC_CLK
	16	GND	15	
	18	LVDS0_CHB_TXN0	17	LVDS0_CHB_TXP0
	20	LVDS0_CHB_TXN1	19	LVDS0_CHB_TXP1
	22	LVDS0_CHB_TXN2	21	LVDS0_CHB_TXP2
	24	LVDS0_CHB_TXN3	23	LVDS0_CHB_TXP3
	26	LVDS0_CHB_CLKN	25	LVDS0_CHB_CLKP
	28	NC	27	NC
	30	GND	29	GND

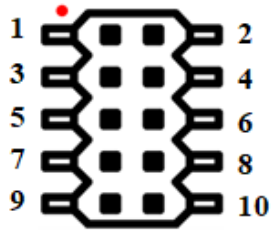
J8 : Audio

PCB Footprint	Pin No.	Signal Description	Pin No.	Signal Description
	1	MIC1L	2	LINE_IN_L
	3	AUD_GND	4	LINE_IN_R
	5	LINE_OUT_L	6	AUD_GND
	7	LINE_OUT_R	8	MIC1R

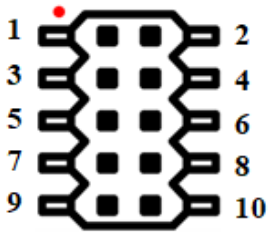
J12 : USB2 x 2 Header

PCB Footprint	Pin No.	Signal Description	Pin No.	Signal Description
	1	VUSB	2	VUSB
	3	USB2_N	4	USB3_N
	5	USB2_P	6	USB3_P
	7	GND	8	GND
			10	NC

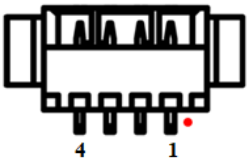
J15 : COM2 RS232/RS422/RS485

PCB Footprint	Pin No.	Signal Description	Pin No.	Signal Description
	1	DCD#2	2	RXD#2
	3	TXD#2	4	DTR#2
	5	GND	6	DSR#2
	7	RTS#2	8	CTS#2
	9	RI#2	10	NC

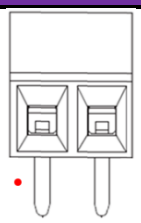
J16: COM1 RS232/RS422/RS485

PCB Footprint	Pin No.	Signal Description	Pin No.	Signal Description
	1	DCD#1	2	RXD#1
	3	TXD#1	4	DTR#1
	5	GND	6	DSR#1
	7	RTS#1	8	CTS#1
	9	RI#1	10	NC

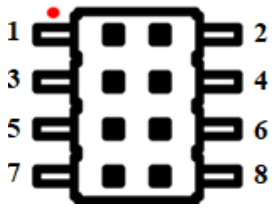
J17 : FAN

PCB Footprint	Pin No.	Signal Description	Pin No.	Signal Description
	1	GND	3	CPU_FANIN
	2	12V	4	CPU_FANOUT

J20 : DC IN (DNI)

PCB Footprint	Pin No.	Signal Description	Pin No.	Signal Description
	1	Vin		
	2	GND		

J23 : Front Panel

PCB Footprint	Pin No.	Signal Description	Pin No.	Signal Description
	1	P_LED+	2	P_LED-
	3	SATA_LED+	4	SATA _LED-
	5	RESET#	6	GND
	7	GND	8	PWRBTN#

Chapter 5

System Overview

5 Sample Code
5.1 Watch Dog Timer
5.2 GPIO Signal

5. Sample Code

5.1 Watch Dog Timer

```
//F81804 WDT Sample Code
#Define SIO_Port_Index          0x2E
#Define SIO_Port_Data           0x2F
#Define WDT_LDN                 0x07
#Define WDT_Config_offset       0xF5
#Define WDT_Time_offset         0xF6
#Define Time_Unit           0x00 //Time unit, 0=1 second, 1=60 second
#Define Time                0x05 //Time, 5 second for example.

void Enter_F81804_SIO() {
        IoWrite8(SIO_Port_Index, 0x87);
        IoWrite8(SIO_Port_Index, 0x87);
        //Enter F81804 SIO
}

void Set_WDT_LDN() {
        IoWrite8(SIO_Port_Index, 0x07);
        IoWrite8(SIO_Port_Data, WDT_LDN);
}

void Set_Register(UINT8 offset, UINT8 And_Value, UINT8 OR_value) {
        UINT8 Temp;
        IoWrite8(SIO_Port_Index, offset);
        Temp=(IoRead8(SIO_Port_Data) & And_Value) | OR_Value;
        IoWrite8(SIO_Port_Data, Temp);
}

Byte Get_Register(UINT8 offset) {
        UINT8 Temp;
        IoWrite8(SIO_Port_Index, offset);
        Temp=IoRead8(SIO_Port_Data);
        return Temp;
}
```

```
void main()
{
	UINT8 Count_Time;

	Enter_F81804_SIO();
	Set_WDT_LDN();
	Set_Register(WDT_Config_offset,0xBF,0x40);		//Bit6: WDTMOUT_STS, Write 1 to clear Watchdog timeout event.
	Set_Register(WDT_Config_offset,0xF7,(Time_Unit<<3));	//Bit3: Set Time Unit, 0=1 second, 1=60 second
	Set_Register(WDT_Time_offset,0x00,Time);	//Set Time.
	Set_Register(WDT_Config_offset,0xDF,0x20);		//Bit5: 0=Disable WDT , 1=Enable WDT.
	Count_Time=Get_Register(WDT_Time_offset);		//Read watchdog timer.
}
```

5.2 GPIO Signal

```
//F81804 GPIO Sample Code
#Define SIO_Port_Index	0x2E
#Define SIO_Port_Data	0x2F
#Define GPIO_LDN	0x06
#Define GPIO_IOSpace	0x0A00

#Define GPO0_Output0x00 //GPO0 Output Mode, 0:Output Low,	1:Output High
#Define GPO1_Output0x00 //GPO1 Output Mode, 0:Output Low,	1:Output High
#Define GPO2_Output0x00 //GPO2 Output Mode, 0:Output Low,	1:Output High
#Define GPO3_Output0x00 //GPO3 Output Mode, 0:Output Low,	1:Output High
#Define GPI0_Offset	0x06 //GPI0 offset
#Define GPI1_Offset	0x07 //GPI1 offset
#Define GPI3_Offset	0x03 //GPI3 offset

void Enter_F81804_SIO() {
	IoWrite8(SIO_Port_Index, 0x87);
	IoWrite8(SIO_Port_Index, 0x87);
```

```
	//Enter F81804 SIO
}

void Set_GPIO_LDN() {
	IoWrite8(SIO_Port_Index, 0x07);
	IoWrite8(SIO_Port_Data, GPIO_LDN);
}

void Set_Register(UINT8 offset, UINT8 And_Value, UINT8 OR_value) {
	UINT8 Temp;
	IoWrite8(SIO_Port_Index, offset);
	Temp=(IoRead8(SIO_Port_Data) & And_Value) | OR_Value;
	IoWrite8(SIO_Port_Data, Temp);
}

Byte Get_Register(UINT8 offset, UINT8 And_Value) {
	UINT8 Temp;
	IoWrite8(SIO_Port_Index, offset);
	Temp=IoRead8(SIO_Port_Data) & And_Value;
	return Temp;
}

void main()
{
	UINT8 GPI0;
	UINT8 GPI1;
	UINT8 GPI2;
	UINT8 GPI3;

	Enter_F81804_SIO();
	Set_GPIO_LDN();

	//GPO Output and setting
	//GPO0 Setting
	Set_Register(0x99, 0xFB, (GPO0_Output<<2));	//Bit2: GPO0 status, 0: Low 1: High

	//GPO1 Setting
```

```
    Set_Register(0x99, 0xF7, (GPO1_Output<<3));      //Bit3: GPO1 status, 0: Low 1: High

    //GPO2 Setting
    Set_Register(0x99, 0xEF, (GPO2_Output<<4));      //Bit4: GPO2 status, 0: Low 1: High

    //GPO3 Setting
    Set_Register(0x99, 0x7F, (GPO3_Output<<7));      //Bit7: GPO3 status, 0: Low 1: High

    //GPI Input and get status
    GPI0= IoRead8(GPIO_IOSpace+GPI0_Offset);      //Bit0: GPI0 status, 0: Low 1: High

    GPI1= IoRead8(GPIO_IOSpace+GPI1_Offset);      //Bit6: GPI1 status, 0: Low 1: High

    GPI2= Get_Register(0x9A,0x02);                //Bit1: GPI2 status, 0: Low 1: High

    GPI3= IoRead8(GPIO_IOSpace+GPI3_Offset);      //Bit0: GPI3 status, 0: Low 1: High
}
```

Chapter 6

System Overview

6 BIOS Setup
6.1 Entering Setup-Launch System Setup
6.2 Main
6.3 Configuration
6.4 Security
6.5 Boot
6.6 Save & Exit

6. BIOS Setup information

PICO-8020 is equipped with the AMI BIOS stored in Flash ROM. The following section describes the BIOS setup program. The BIOS setup program can be used to view and change the BIOS settings for the module. Only experienced users should change the default BIOS settings.

6.1 Entering Setup

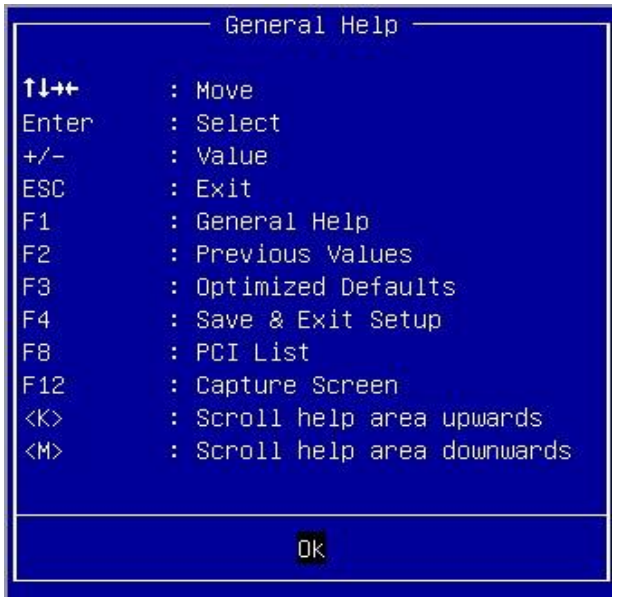
Power on the computer and the system will start POST (Power on Self-Test) Process. When the message below appears on the screen, press<Del> key will enter BIOS setup screen.

Press <Del> to enter SETUP

If the message disappears before responding and still wishes to enter Setup, please restart the system by turning it OFF and On or pressing the RESET button. It can be also restarted by pressing <Ctrl>, <Alt>, and <Delete> keys on keyboard simultaneously.

Press <F1> to Run General Help or Resume

The BIOS setup program provides a General Help screen. The menu can be easily called up from any menu by pressing <F1>. The Help screen lists all the possible keys to use and the selections for the highlighted item. Press <Esc> to exit the Help Screen.

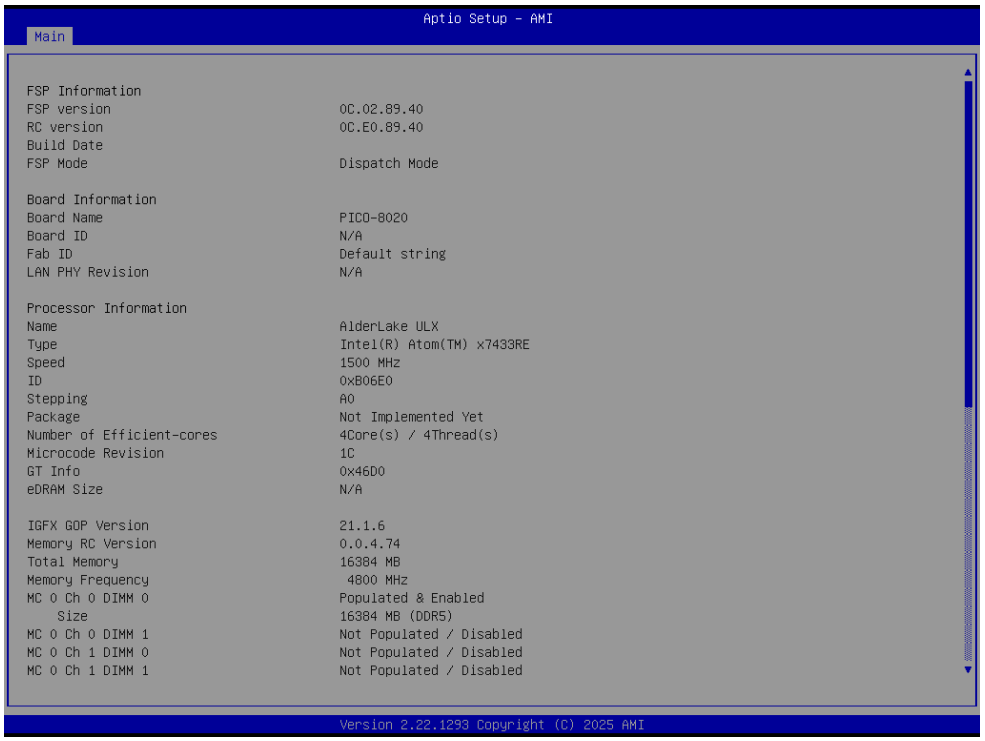


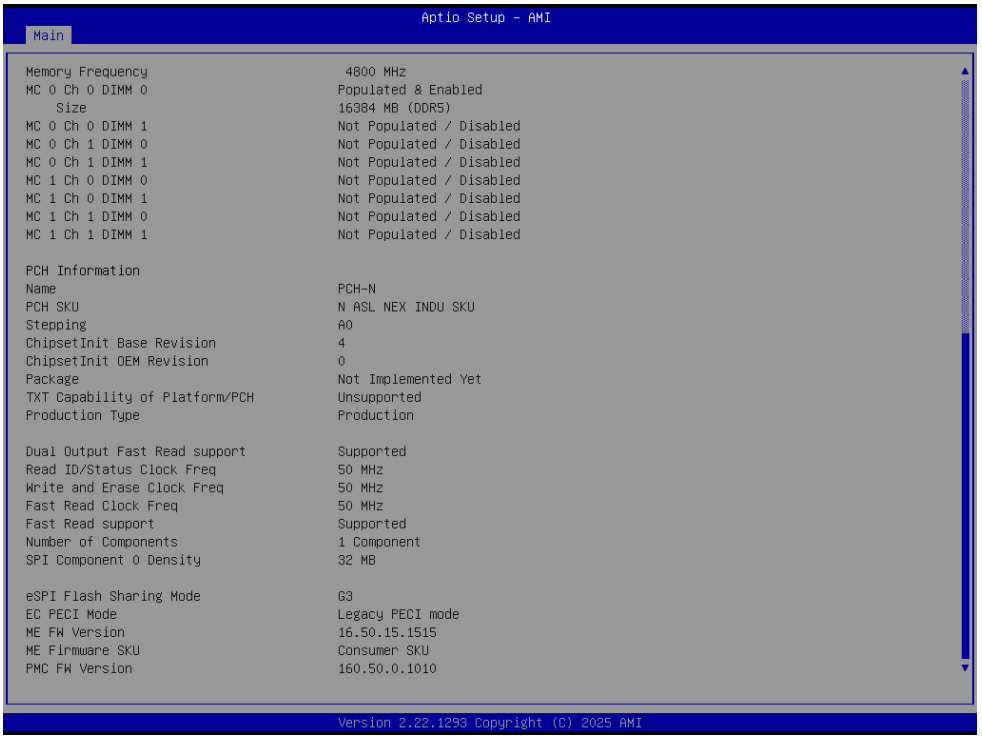
6.2 Main

Use this menu for basic system configurations, such as time, date etc.

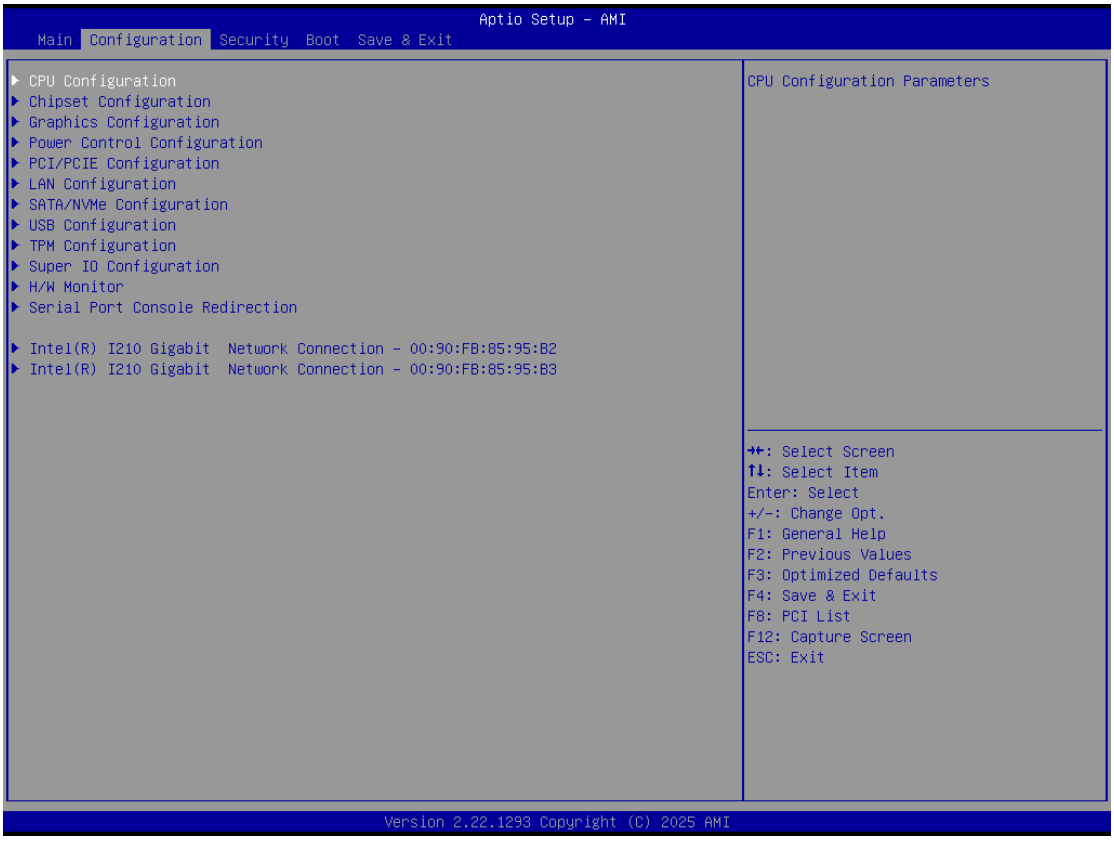
Feature	Description	Options
System Date	The date format is <Day>, <Month><Date><Year>. Use [+] or [−] to configure system Date.	
System Time	The time format is <Hour><Minute><Second>. Use [+] or [−] to configure system Time.	

Detailed System Information

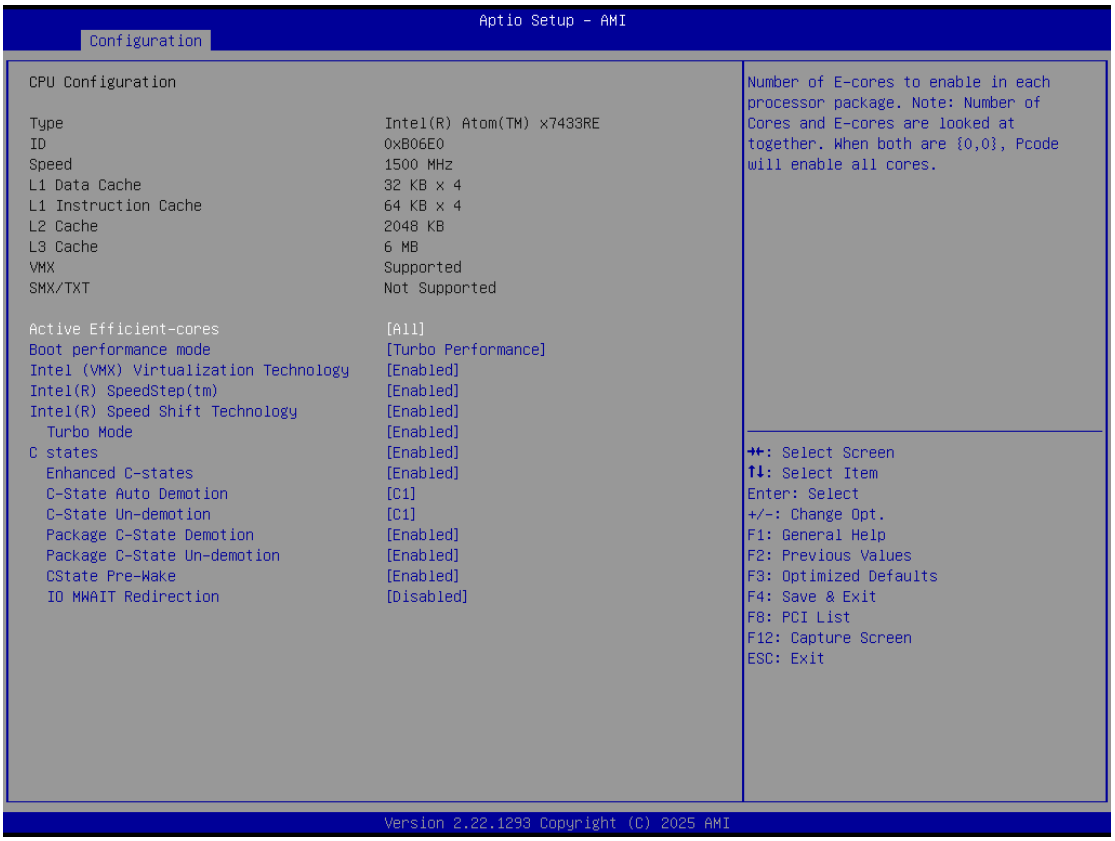




6.3 Configuration



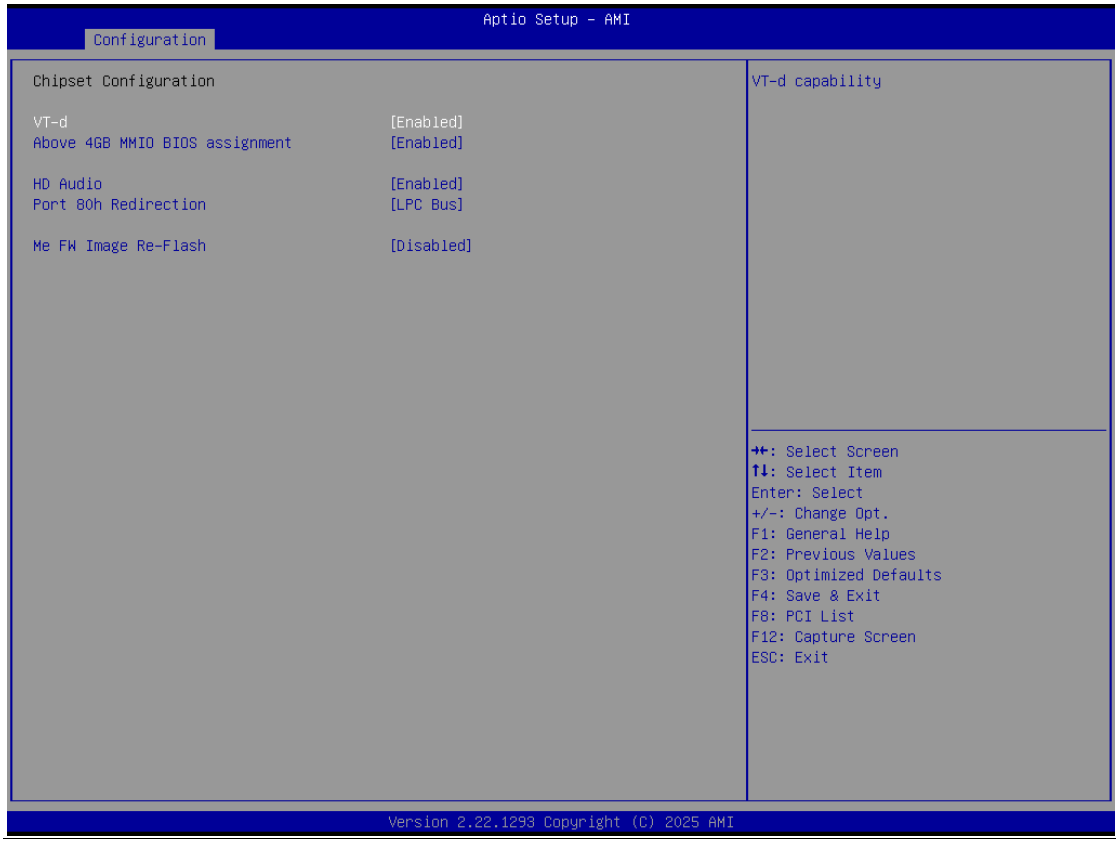
6.3.1 CPU Configuration



Feature	Description	Options
Active Efficient-Cores	Number of E-cores to enable in each processor package. Note: Number of Cores and E-cores are looked at together,	★All, 3, 2, 1
Boot performance mode	Select the performance state that the BIOS will set starting from reset vector	★Turbo Performance , Max Non-Turbo Performance, Max Battery,
Intel (VMX) Virtualization Technology	When enabled, a VMM can utilize the additional hardware capabilities provided by Vander pool Technology.	Disabled, ★Enabled
Intel (R) Speed Step (tm)	Allows more than two frequency ranges to be supported.	Disabled, ★Enabled

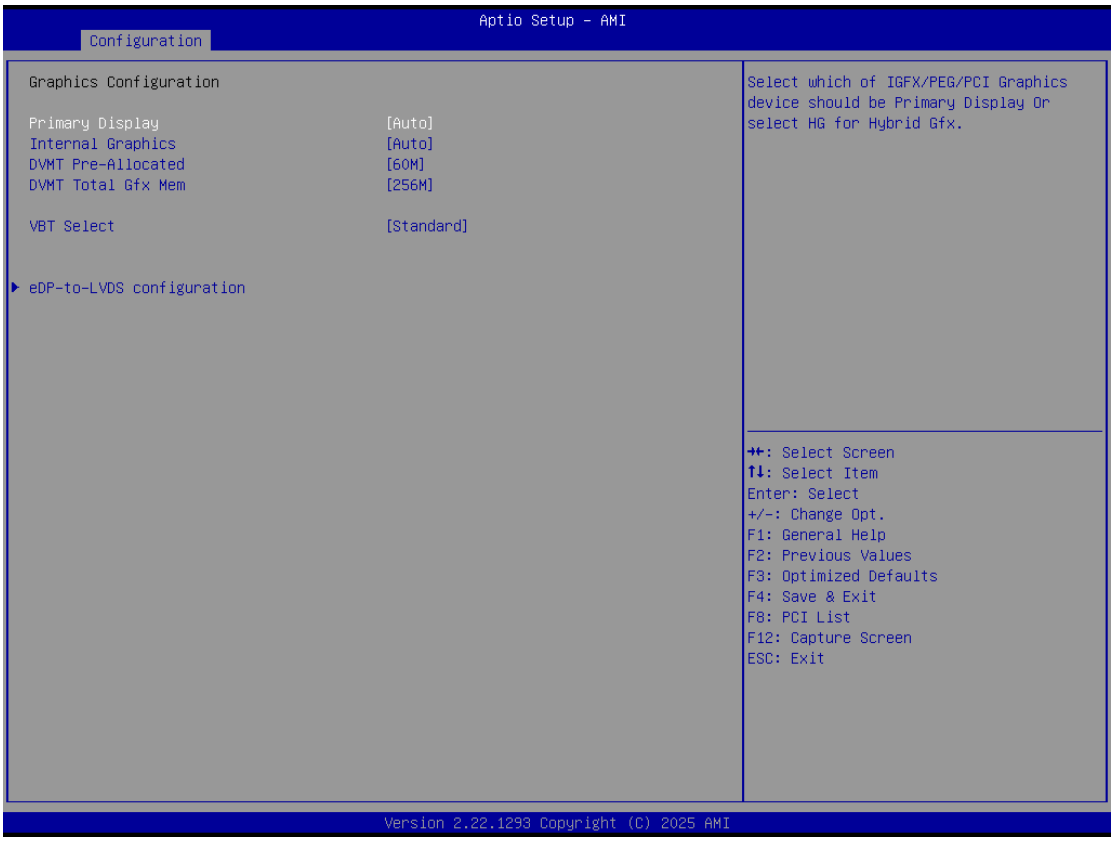
Feature	Description	Options
Intel (R) Speed Shift Technology	Enable/Disable Intel® Speed Shift Technology support. Enabling will expose the CPPC v2 interface to allow for hardware controlled P-states	Disabled, ★Enabled
Turbo Mode	Enable/Disable processor Turbo Mode (requires EMTTM enabled too). AUTO means enabled.	Disabled, ★Enabled
C states	Enable/disable CPU Power Management. Allows CPU to go to C states when it's not 100% utilized	Disabled, ★Enabled
Enhanced C-states	Enable/Disable C1E.When enabled, CPU will switch to minimum speed when all cores enter C-state	Disabled, ★Enabled
C-State Auto Demotion	Configure C-State Auto Demotion	Disabled, ★C1
C-State Un-demotion	Configure C-State Un-demotion	Disabled, ★C1
Package C State Demotion	Package C-State Demotion	Disabled, ★Enabled
Package C State Un-demotion	Package C-State Un-demotion	Disabled, ★Enabled
CState Pre-Wake	Disable – Sets bit 30 of POWER_CTL MSR(0x1FC) to 1 to disable the Cstate Pre-Wake	Disabled, ★Enabled
IO MWAIT Redirection	When set, will map IO_read instructions sent to IO registers PMG_IO_BASE_ADDRBASE+offset to MWAIT(offset)	★Disabled, Enabled

6.3.2 Chipset Configuration



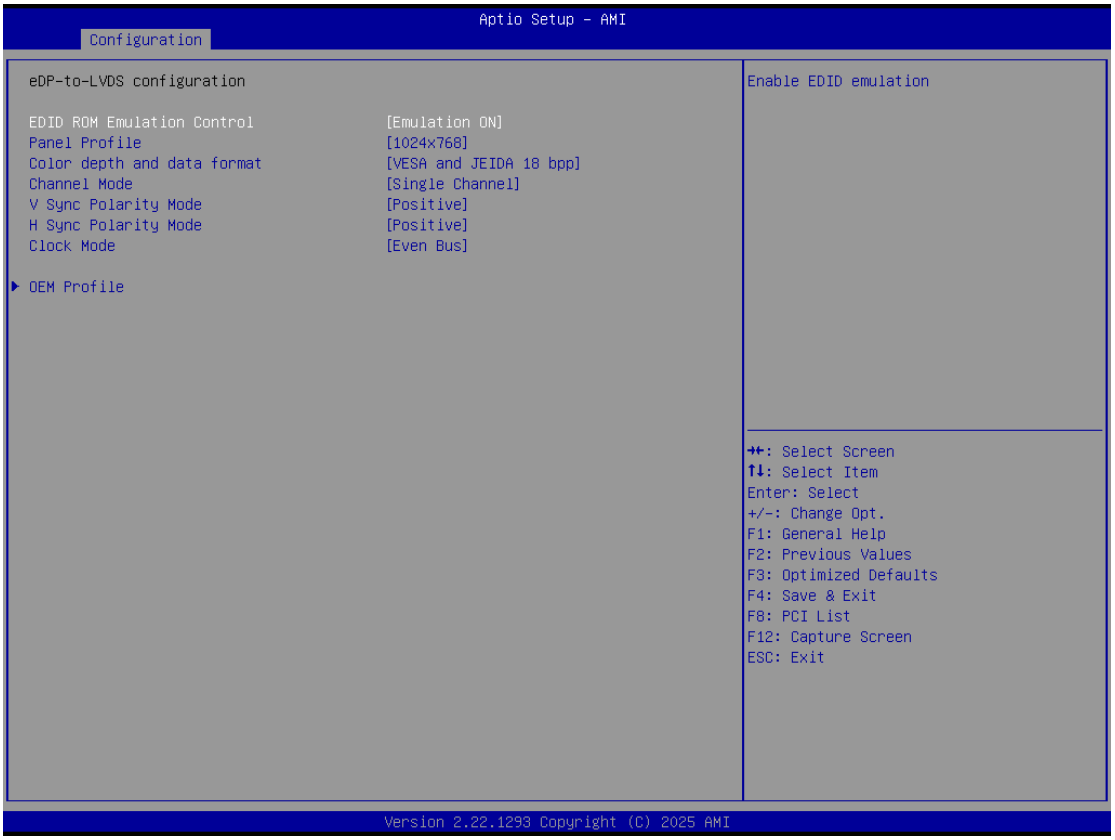
Feature	Description	Options
VT-d	VT-d Capability.	Disabled, ★Enabled
Above 4GB MMIO BIOS assignment	Enable/Disable above 4GB Memory Mapped IO BIOS assignment, This is enabled automatically when Aperture Size is set to 2048MB.	Disabled, ★Enabled
HD Audio	Control Detection of the HD-Audio device. Disabled = HDA will be unconditionally disabled. Enabled = HDA will be unconditionally enabled.	Disabled, ★Enabled
Port 80h Redirection	Control when the Port 80h cycles are sent.	★LPC Bus, PCIE Bus
Me FW Image Re-Flash	Enable/Disable Me FW Image Re-Flash function.	★Disabled, Enabled

6.3.3 Graphics Configuration



Feature	Description	Options
Primary Display	Select which of IGFX/PEG/PCI Graphics device should be Primary Display Or Select HG for Hybrid Gfx.	★Auto, IGFX, PEG Slot, PCH PCI
Internal Graphics	Keep IGFX enable based on the setup options.	★Auto, Disabled, Enabled
DVMT Pre-Allocated	Select DVMT 5.0 Pre-Allocated (Fixed) Graphics Memory size used by the Internal Graphics Device.	32M,64M, 96M, 128M, 160M, 12M, 16M,20M, 24M, 28M, 32M/F7,36M,40M,44M,48M, 52M,56M, ★60M
DVMT Total Gfx Mem	Select DVMT5.0 Total Graphic Memory size used by the Internal Graphics Device	★256M, 128M, MAX
VBT Select	Select VBT for GOP Driver Select VBT to 'No LVDS' in no need LVDS	★Standard, No LVDS

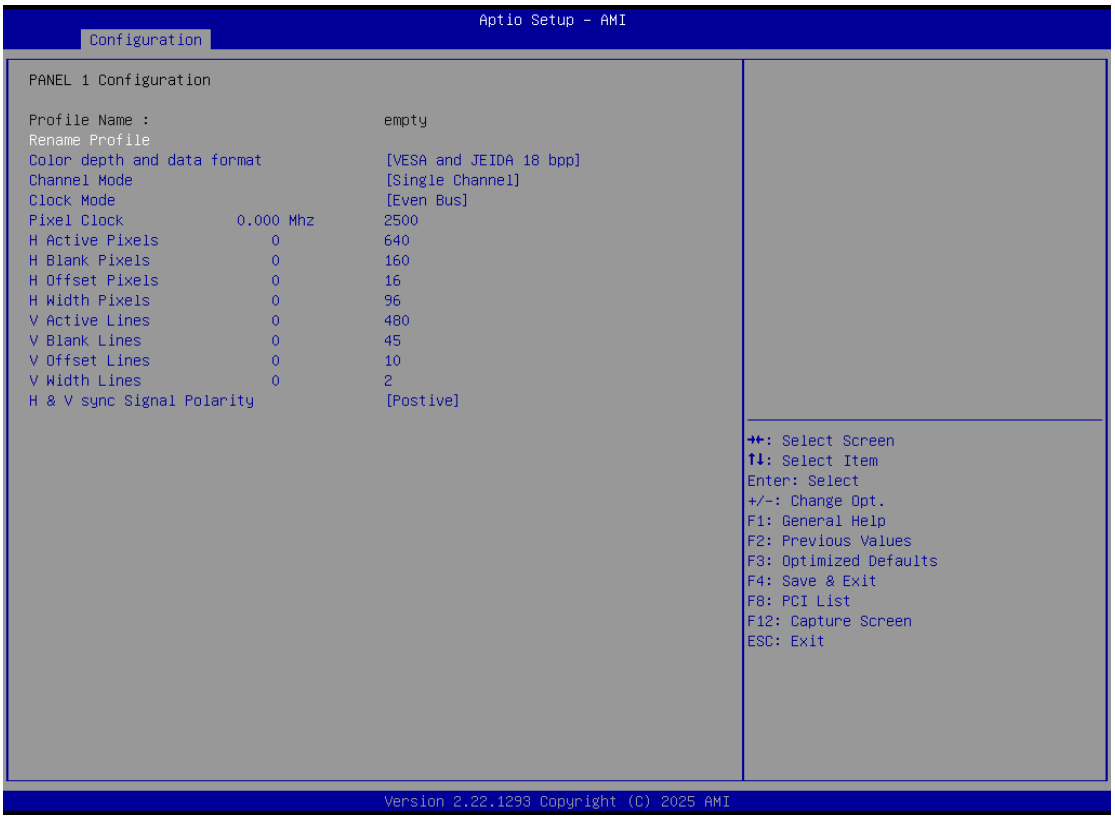
eDP-to-LVDS configuration:



Feature	Description	Options
EDID ROM Emulation Control	Enable EDID emulation.	Emulation OFF, ★Emulation ON
Panel Profile	Select Panel Profile for current use	640x480, 800x480, 800x600, ★1024x768, 1280x1024, 1366x768, 1440x900, 1920x1080, OEM Profile
Color depth and data format	Color depth and data format	★VESA and JEIDA 18 bpp, VESA 24 bpp, JEIDA 24 bpp

Channel Mode	Select LVDS Channel Mode	★Single Channel, Dual Channel
V Sync Polarity Mode	Select V Sync Polarity Mode	★Polarity, Negative
H Sync Polarity Mode	Select H Sync Polarity Mode	★Polarity, Negative
Clock Mode	Select clock output for LVDS.	★Even Bus, Odd Bus, Both Buses

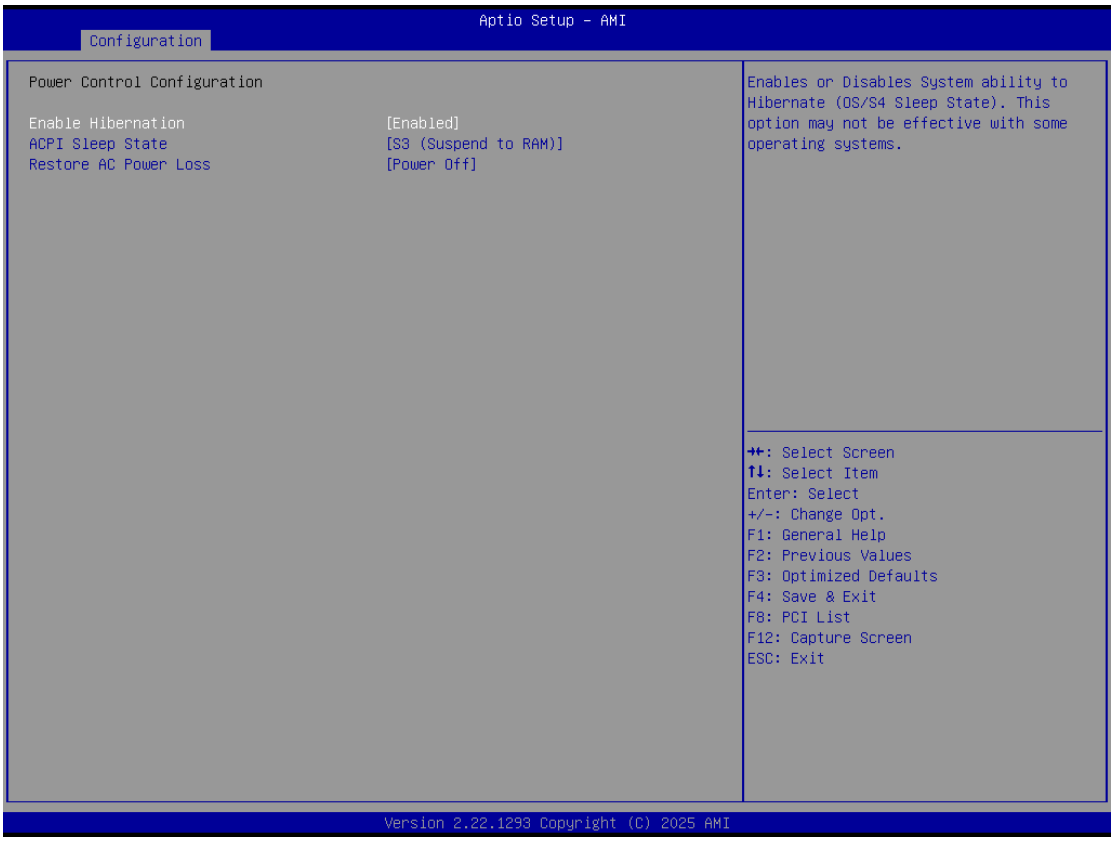
OEM Profile: PANEL 1 Configuration



Feature	Description	Options
Color depth and data format	Select Color depth and data format.	VESA 24 bpp, JEIDA 24 bpp

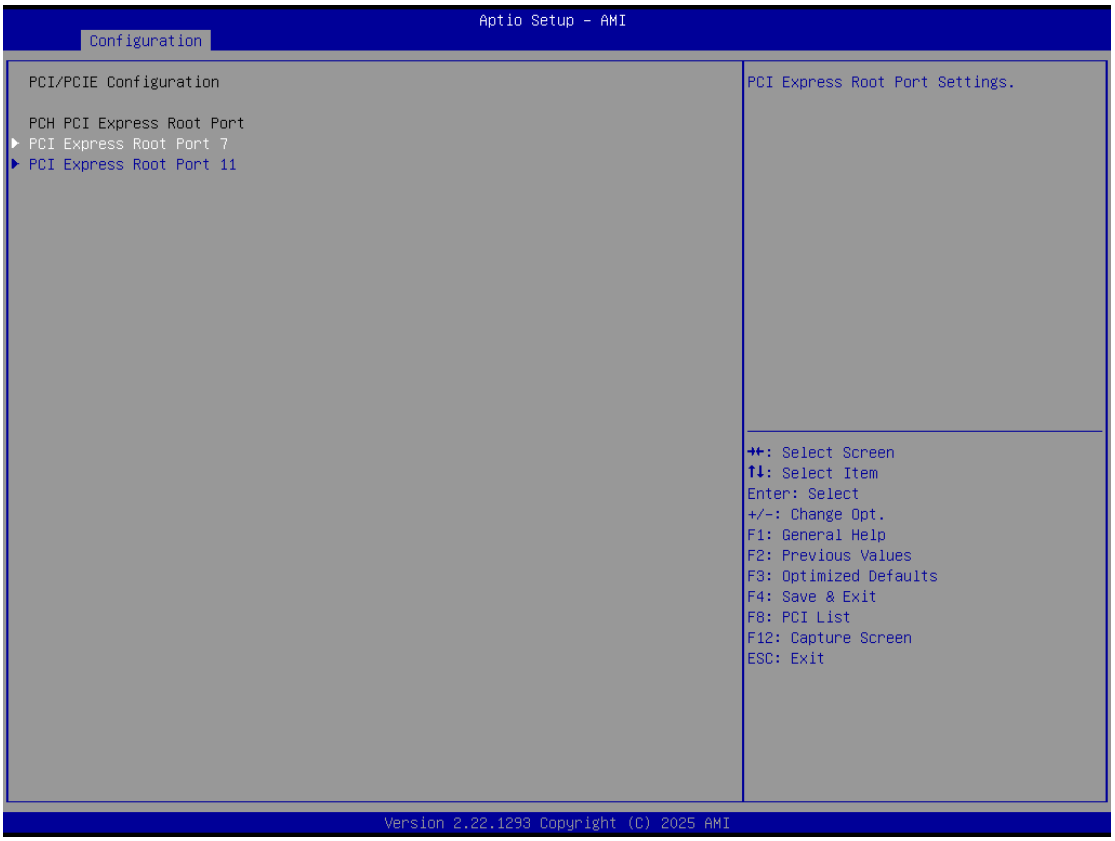
		★VESA and JEIDA 18 bpp
Channel Mode	Select LVDS Channel Mode.	★Single channel, Dual channel
Clock Mode	Select Clock output for LVDS.	★Even Bus, Odd Bus, Both Buses
Pixel Clock	Pixel Clock (10Khz)	★ 2500
H Active Pixels	H Active Pixels (Pixel)	★ 640
H Blank Pixels	H Blank Pixels (Pixel)	★ 160
H Offset Pixels	H Offset Pixels (Pixel)	★ 16
H Width Pixels	H Width Pixels (Pixel)	★ 96
V Active Lines	V Active Lines (Line)	★ 480
V Blank Lines	V Blank Lines (Line)	★ 45
V Offset Lines	V Offset Lines (Line)	★ 10
V Width Lines	V Width Lines (Line)	★ 2
H & V sync Signal Polarity	Flag: 0x1E Signal Polarity is Postive; 0x18 Signal Polarity is Non-Postive	★ Postive, Non-Postive

6.3.4 CPU Power Control Configuration

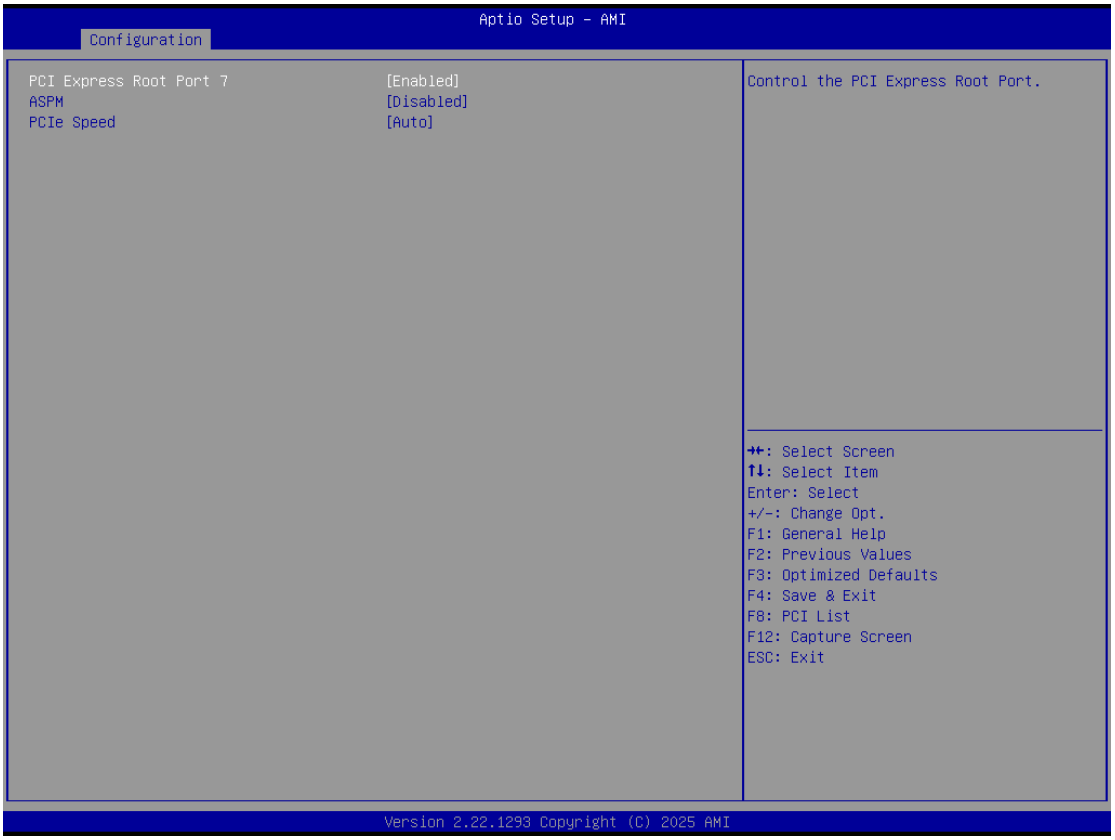


Feature	Description	Options
Enable Hibernation	Enables or Disables System ability to Hibernate (OS/S4 Sleep State). This option may not be effective with some operating systems.	Disabled, ★Enabled
ACPI Sleep State	Select the highest ACPI sleep state the system will enter when the SUSPEND button is pressed.	★S3 (Suspend to RAM), Suspend Disabled
Restore AC Power Loss	Specify what state to go to when power is re-applied after a power failure (G3 state)	★Power Off, Power On, Last State

6.3.5 PCI/PCIE Configuration

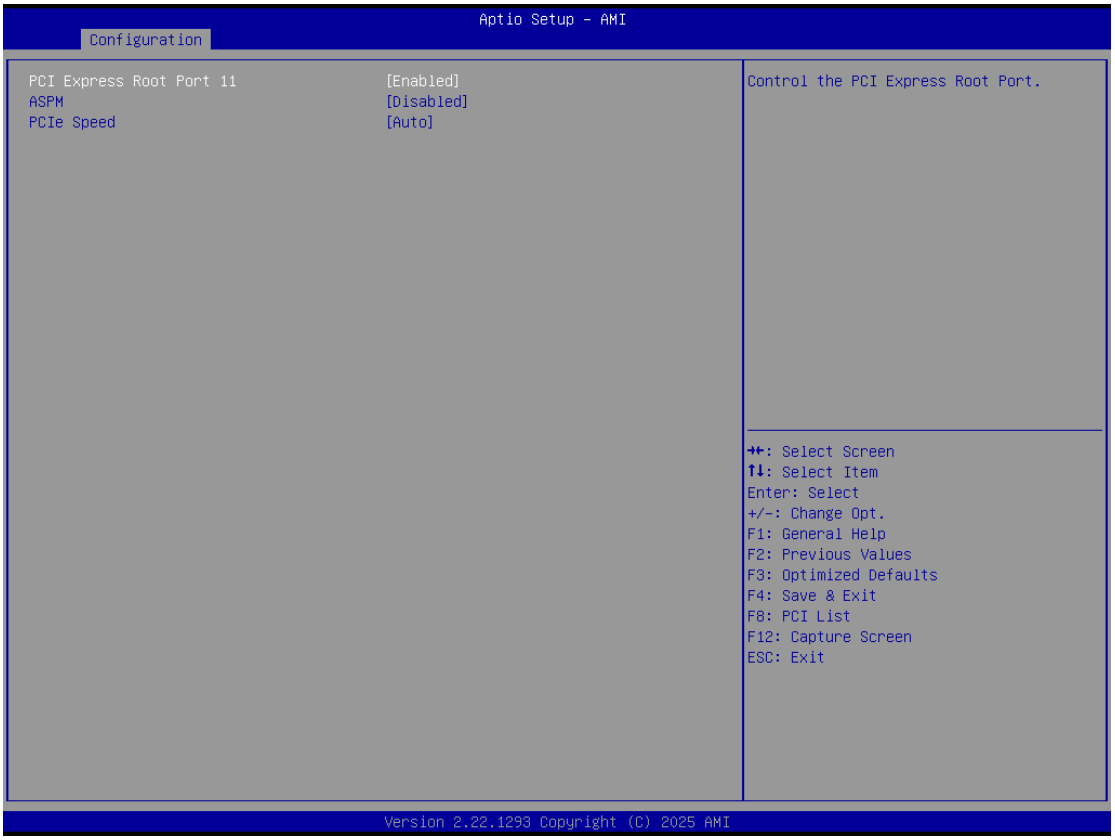


PCI Express Root Port 7



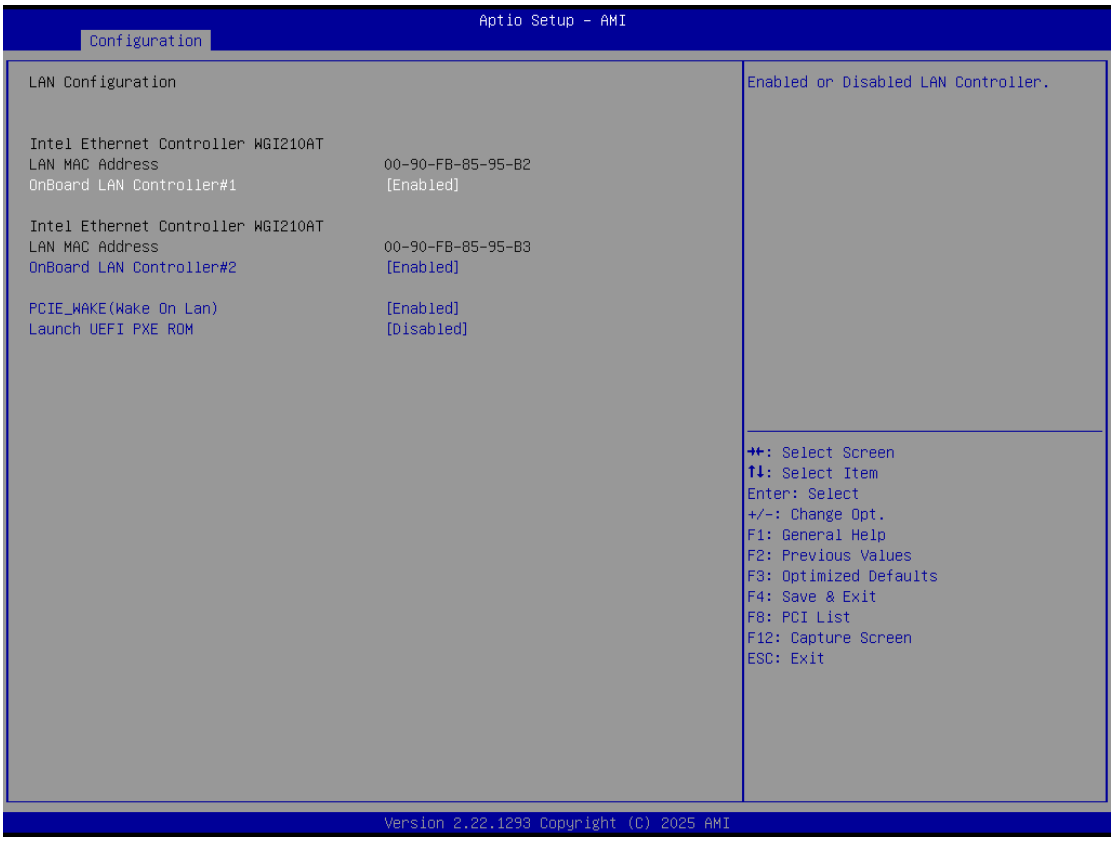
Feature	Description	Options
PCI Express Root Port 7	Control the PCI Express Root Port.	Disabled, ★Enabled
ASPM	Set the ASPM Level: Force L0s – Force all links to L0s State AUTO-BIOS auto configure DISABLE – Disables ASPM	★Disabled, L1, Auto
PCIe Speed	Configure PCIe Speed	★Auto, Gen1, Gen2, Gen3

PCI Express Root Port 11



Feature	Description	Options
PCI Express Root Port 11	Control the PCI Express Root Port.	Disabled, ★Enabled
ASPM	Set the ASPM Level: Force L0s – Force all links to L0s State AUTO-BIOS auto configure DISABLE – Disables ASPM	★Disabled, L1, Auto
PCIe Speed	Configure PCIe Speed	★Auto, Gen1, Gen2, Gen3

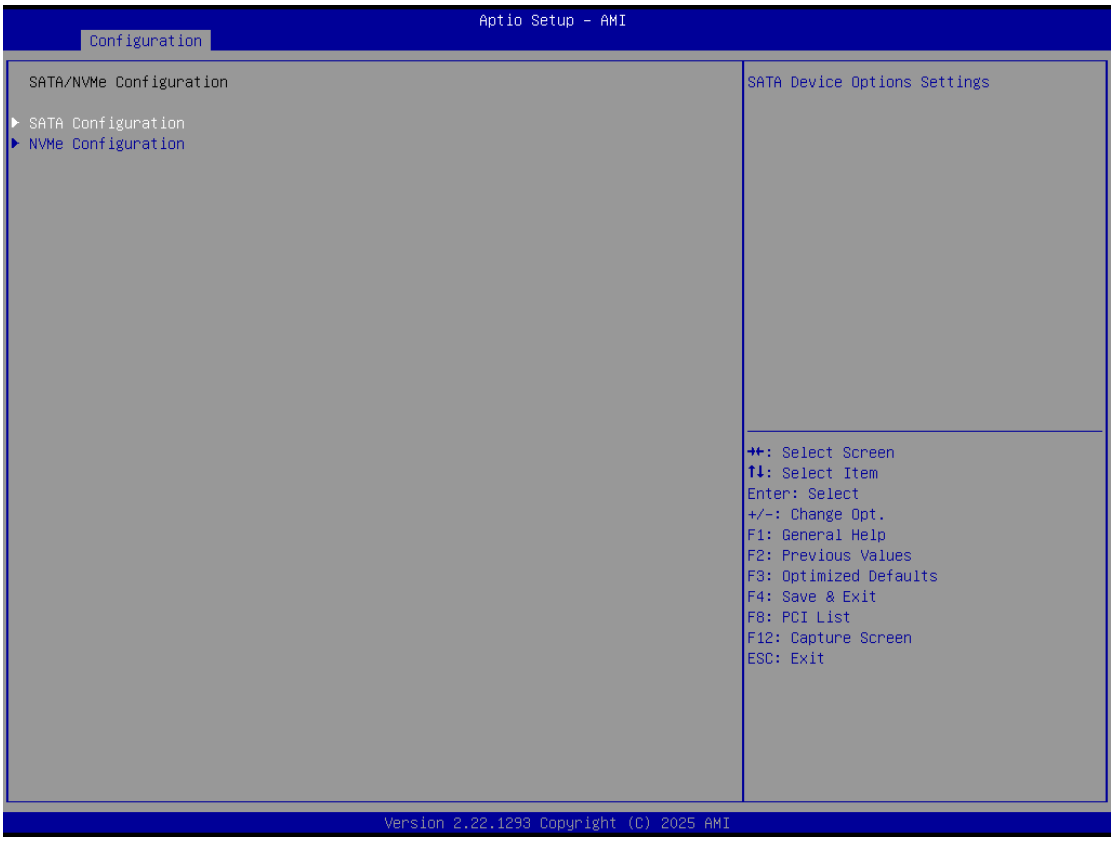
6.3.6 LAN Configuration



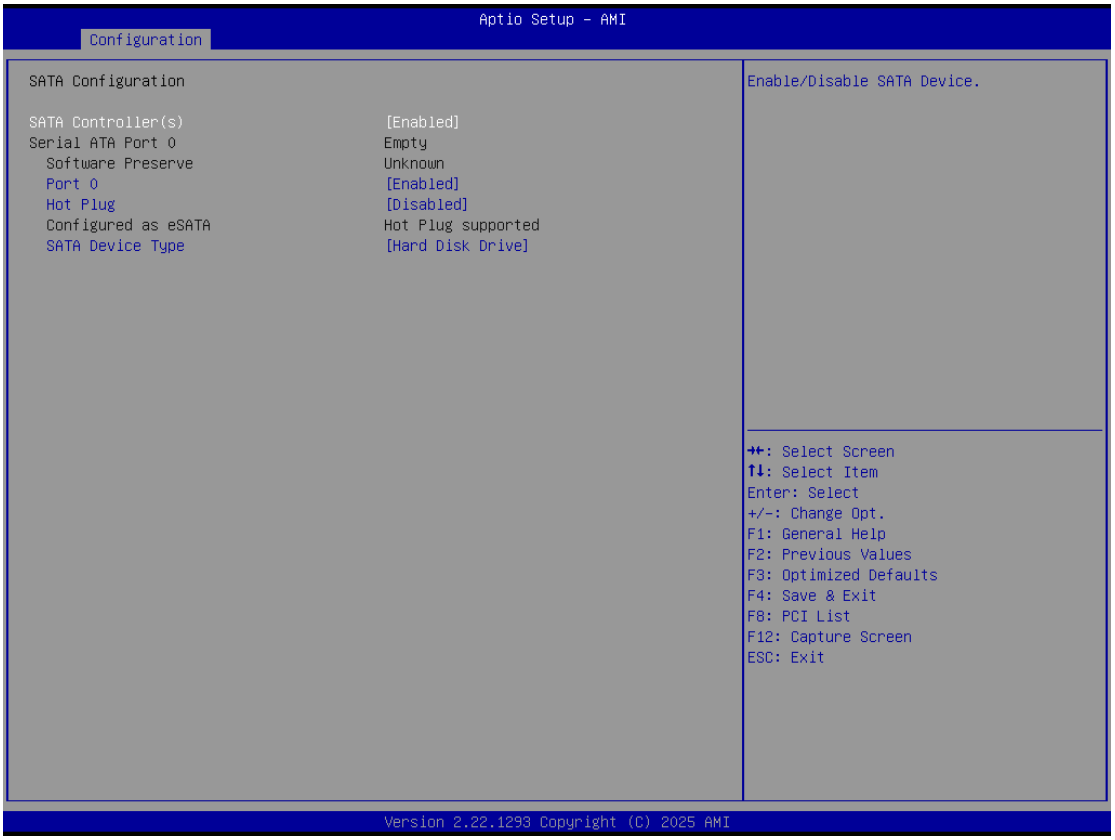
Feature	Description	Options
OnBoard LAN Controller #1	Enable or Disable LAN Controller.	Disabled, ★Enabled
OnBoard LAN Controller #2	Enable or Disable LAN Controller.	Disabled, ★Enabled
PCIE_WAKE (Wake On Lan)	Control the PCIE Wake# pin for Wake On Lan function.	Disabled, ★Enabled
Launch UEFI PXE ROM	Enable/Disable UEFI Network Stack	★Disabled, Enabled

Feature	Description	Options
Launch UEFI PXE ROM (Enabled)		
IPv4 PXE Support	Enable/Disable IPv4 PXE boot support. If disabled, IPv4 PXE boot support will not be available.	Disabled, ★Enabled
IPv4 HTTP Support	Enable/Disable IPv4 HTTP boot support. If disabled, IPv4 HTTP boot support will not be available.	Disabled, ★Enabled
IPv6 PXE Support	Enable/Disable IPv6 PXE boot support. If disabled, IPv6 PXE boot support will not be available.	Disabled, ★Enabled
IPv6 HTTP Support	Enable/Disable IPv6 HTTP boot support. If disabled, IPv6 HTTP boot support will not be available.	Disabled, ★Enabled
PXE boot wait time	Wait time in seconds to press ESC key to abort the PXE boot. Use either +/- or numeric keys to set the value.	★0
Media detect count	Number of times the presence of media will be checked. Use either +/- or numeric keys to set the value.	★1

6.3.7 SATA / NVMe Configuration

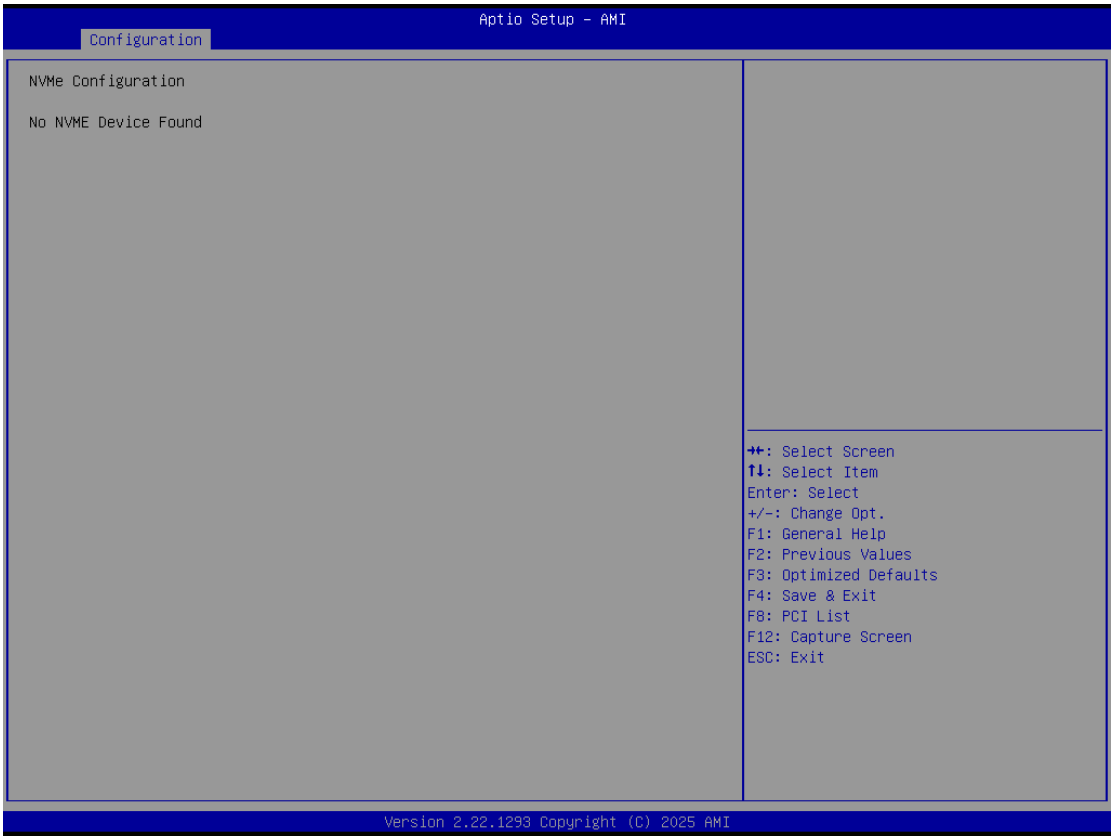


SATA Configuration

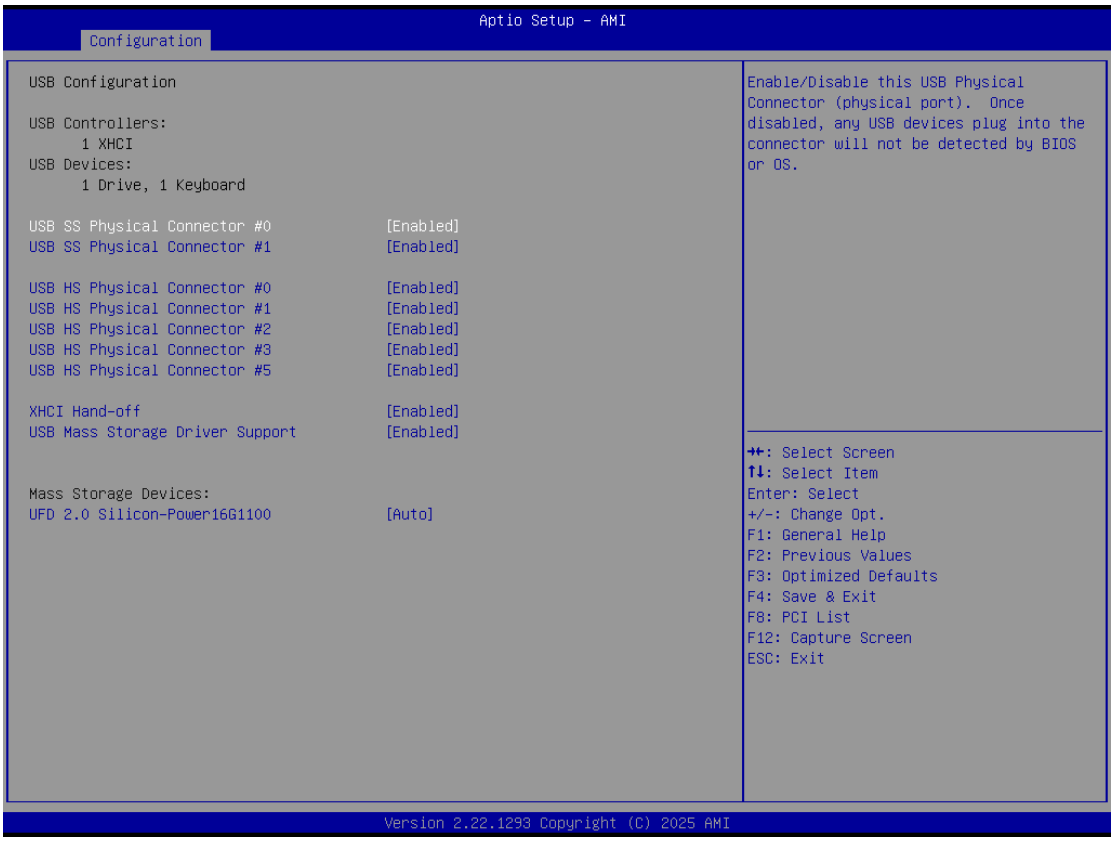


Feature	Description	Options
SATA Controller(s)	Enable/Disable SATA Device	Disabled, ★Enabled
Serial ATA Port 0		
Port 0	Enabled or Disabled SATA Port	Disabled, ★Enabled
Hot plug	Designates this port as Hot pluggable.	★Disabled, Enabled
SATA Device Type	Identify the SATA port is connected to Solid State Drive or Hard Disk Drive.	★Hard Disk Drive, Solid State Drive

NVMe Configation



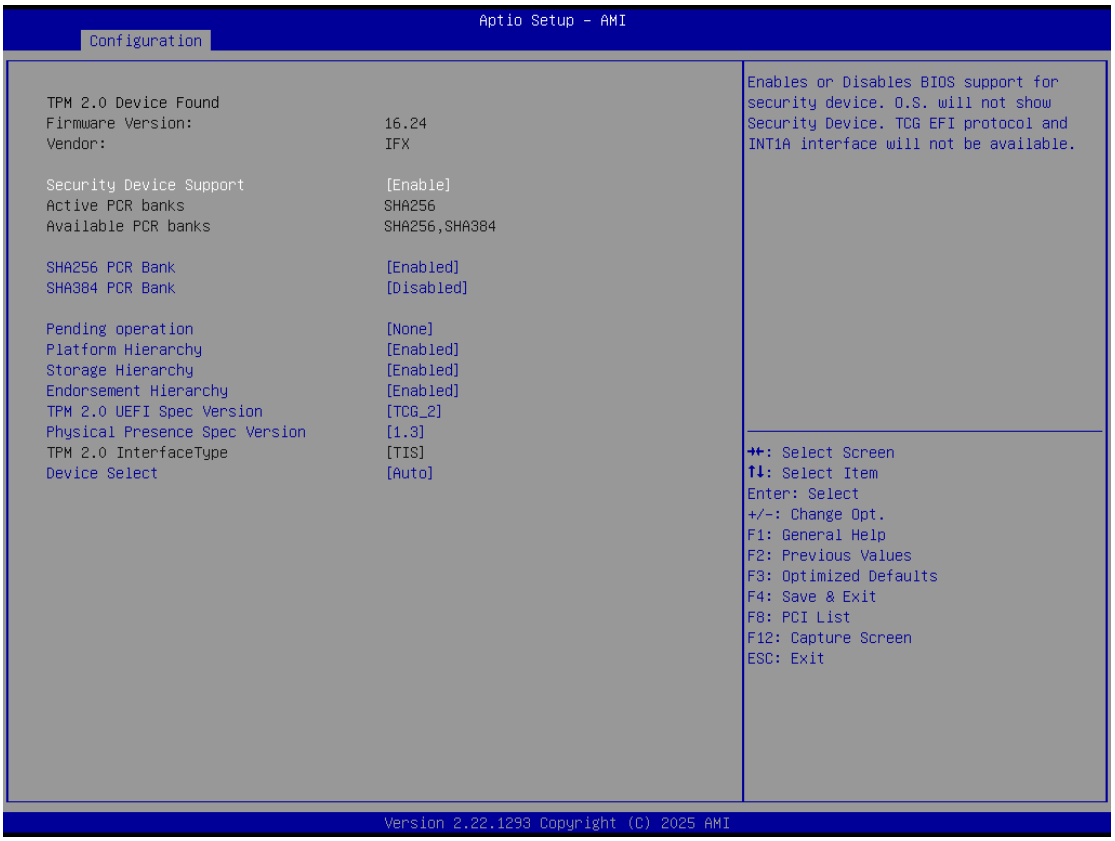
6.3.8 USB Configuration



Feature	Description	Options
USB SS Physical Connector #0	Enabled/Disabled this USB Physical connector (physical port). Once disabled, any USB devices plug into the connector will not be detected by BIOS or OS.	Disabled, ★Enabled
USB SS Physical Connector #1	Enabled/Disabled this USB Physical connector (physical port). Once disabled, any USB devices plug into the connector will not be detected by BIOS or OS.	Disabled, ★Enabled
USB HS Physical Connector #0	Enabled/Disabled this USB Physical connector (physical port). Once disabled, any USB devices plug into the connector will not be detected by BIOS or OS.	Disabled, ★Enabled

Feature	Description	Options
USB HS Physical Connector #1	Enabled/Disabled this USB Physical connector (physical port). Once disabled, any USB devices plug into the connector will not be detected by BIOS or OS.	Disabled, ★Enabled
USB HS Physical Connector #2	Enabled/Disabled this USB Physical connector (physical port). Once disabled, any USB devices plug into the connector will not be detected by BIOS or OS.	Disabled, ★Enabled
USB HS Physical Connector #3	Enabled/Disabled this USB Physical connector (physical port). Once disabled, any USB devices plug into the connector will not be detected by BIOS or OS.	Disabled, ★Enabled
USB HS Physical Connector #5	Enabled/Disabled this USB Physical connector (physical port). Once disabled, any USB devices plug into the connector will not be detected by BIOS or OS.	Disabled, ★Enabled
XHCI Hand-off	This is a workaround for OSes without XHCI hand-off support. The XHCI ownership change should be claimed by XHCI driver	Disabled, ★Enabled
USB Mass Storage Driver Support	Enable/Disable USB Mass Storage Driver Support	Disabled, ★Enabled
Mass storage Devices:		
UFD 2.0 Silicon-Power 16G1100	Mass storage device emulation type. 'AUTO' enumerates devices according to their media format. Optical drives are emulated as 'CDROM'; drives with no media will be emulated according to a drive type.	★Auto, Floppy, Forced FDD, Hard Disk, CD-ROM

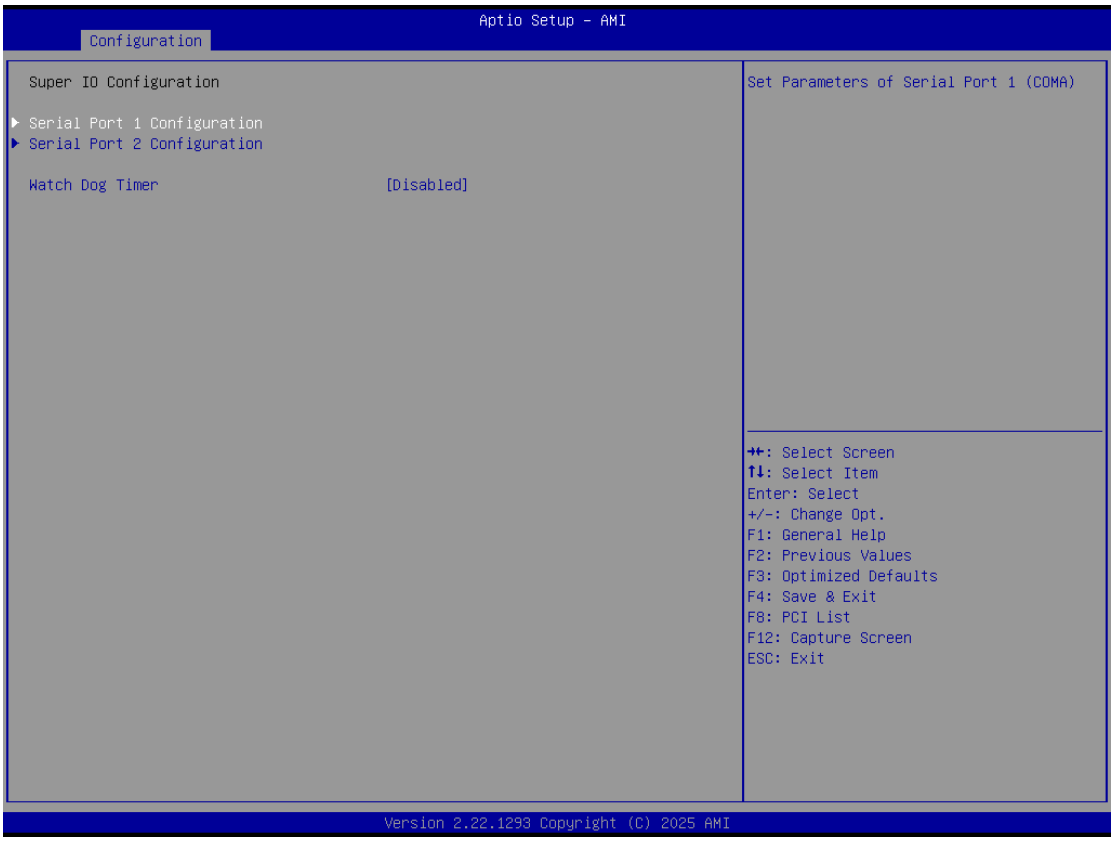
6.3.9 TPM Configuration



Feature	Description	Options
Security Device Support	Enables or Disables BIOS support for security device. O.S. will not show Security Device. TCG EFI protocol and INT1A Interface will not be available.	Disabled, ★Enabled
SHA256 PCR Bank	Enables or Disables SHA256 PCR Bank.	Disabled, ★Enabled
SHA384 PCR Bank	Enables or Disables SHA384 PCR Bank.	★Disabled, Enabled
Pending operation	Schedule an Operation for the Security Device. Note: Your Computer will reboot during restart in order to change State of Security Device.	★None, TPM Clear
Platform Hierarchy	Enables or Disables Platform Hierarchy.	Disabled, ★Enabled

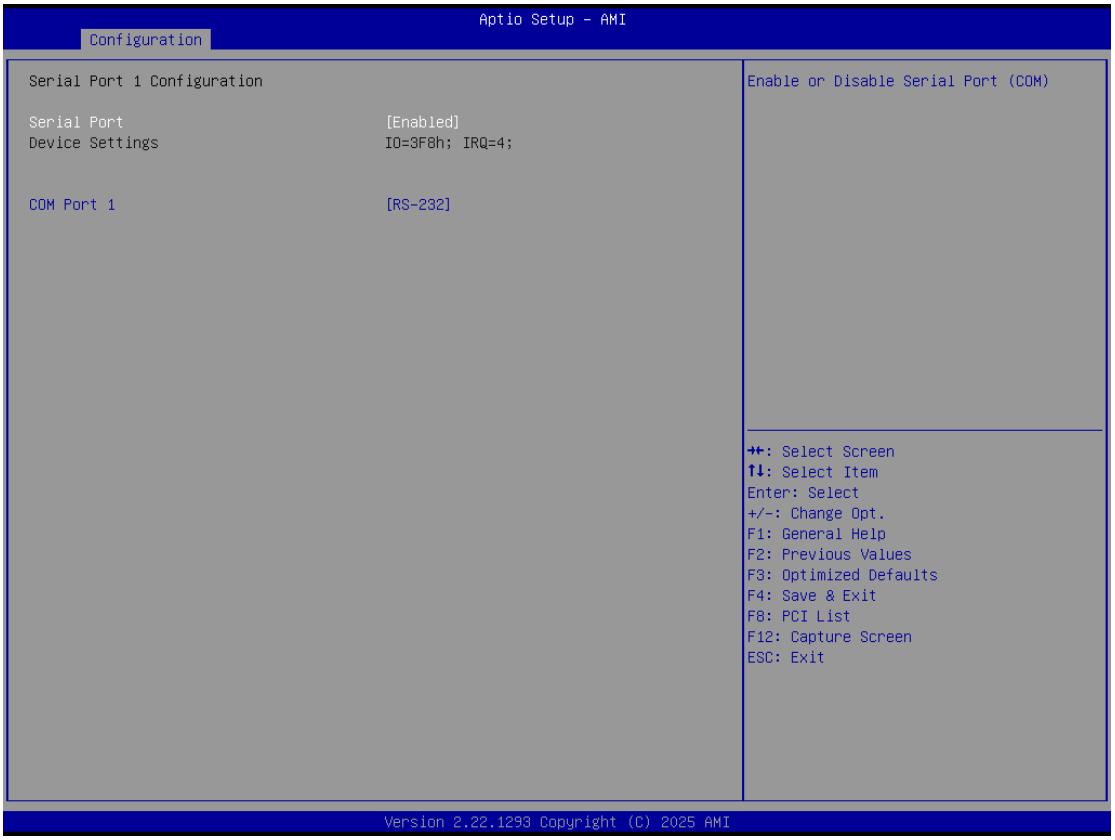
Feature	Description	Options
Storage Hierarchy	Enables or Disables Storage Hierarchy.	Disabled, ★Enabled
Endorsement Hierarchy	Enables or Disables Endorsement Hierarchy.	Disabled, ★Enabled
TPM2.0 UEFI Spec Version	Select the TCG2 Spec Version Support. CG_1_2: the Compatible mode for Win8/Win10. TCG_2: Support new TCG2 protocol and event format for Win10 or later.	TCG_1_2, ★TCG_2
Physical Presence Spec Version	Select to Tell O.S. to Support PPI Spec Version 1.2 or 1.3. Note some HCK tests might not support 1.3.	1.2, ★1.3
Device Select	TPM 1.2 will restrict support to TPM 1.2 devices, TPM 2.0 will restrict support to TPM 2.0 devices, Auto will support both with the default set to TPM 2.0 devices if not found, TPM 1.2 devices will be enumerated.	★Auto, TPM 1.2, TPM 2.0

6.3.10 Super IO Configuration



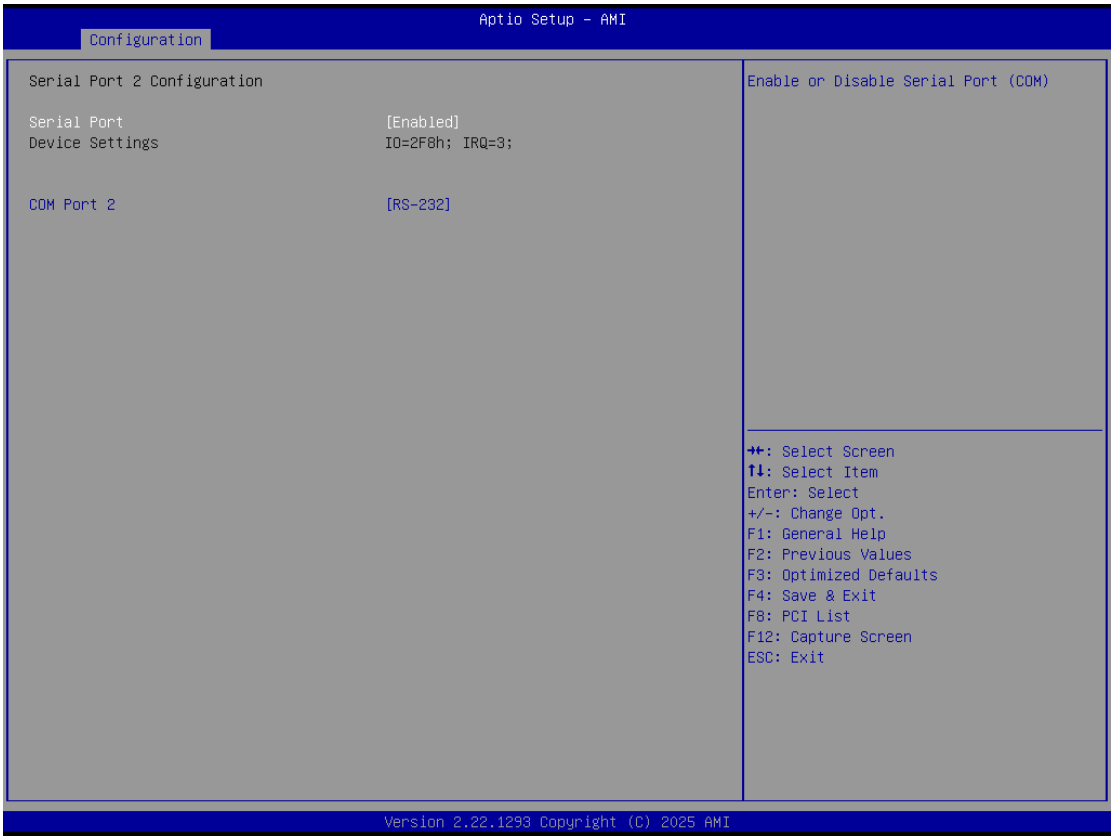
Feature	Description	Options
Serial Port 1 Configuration		
Serial Port 2 Configuration		
Watch Dog Timer	Enable/Disable Watch Dog Timer	★Disabled, Enabled
Watch Dog Timer [Enabled]		
Timer Unit	Select Timer count unit of WDT	★Second, Minute
Timer value	Set WDT Timer value seconds / minutes	★60

Serial Port 1 Configuration



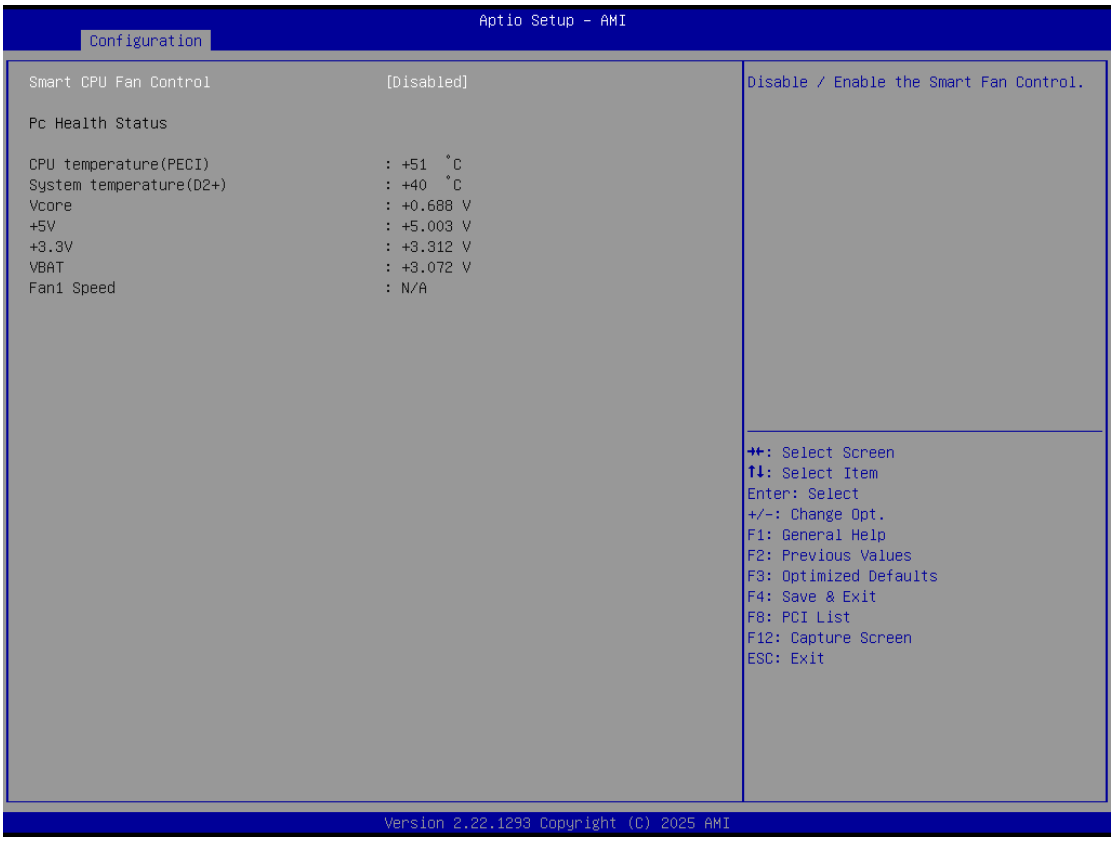
Feature	Description	Options
Serial Port	Enable or Disable Serial Port (COM)	Disabled, ★Enabled
COM Port 1	RS-232/422/485 Control Option.	★RS-232, RS-485 HALF DUPLEX, RS-422 FULL DUPLEX,

Serial Port 2 Configuration



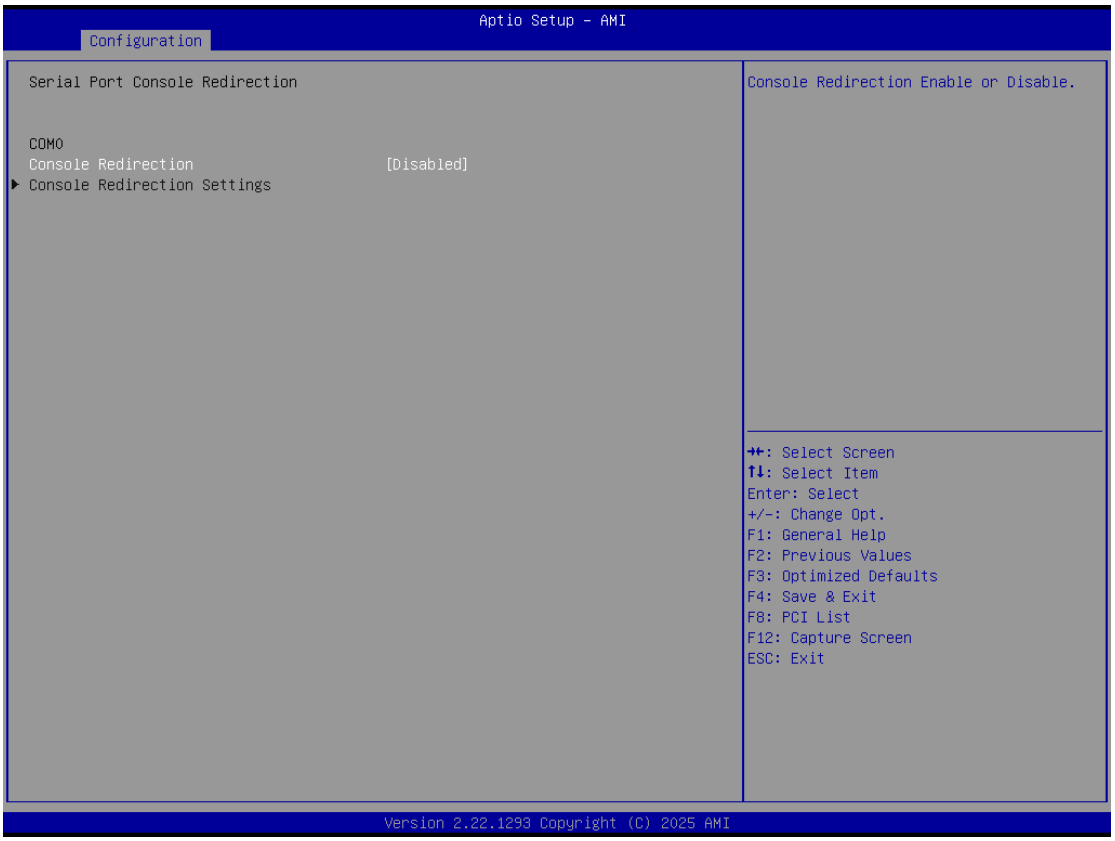
Feature	Description	Options
Serial Port	Enable or Disable Serial Port (COM)	Disabled, ★Enabled
COM Port 2	RS-232/422/485 Control Option.	★RS-232, RS-485 HALF DUPLEX, RS-422 FULL DUPLEX,

6.3.11 HW Monitor



Feature	Description	Options
Smart CPU Fan Control	Disable / Enable the Smart Fan Control.	★Disabled, Enabled
Smart CPU Fan Control [Enabled]		
Smart Fan Start Target Temp	Set Fan Start Target Temperature range from 20 to 80 degree.	★20
Smart Fan Full Target Temp	Set Fan Full Target Temperature range from 20 to 80 degree.	★80
Smart Fan Low and RPM	Smart Fan Low and RPM Percentage.	★50

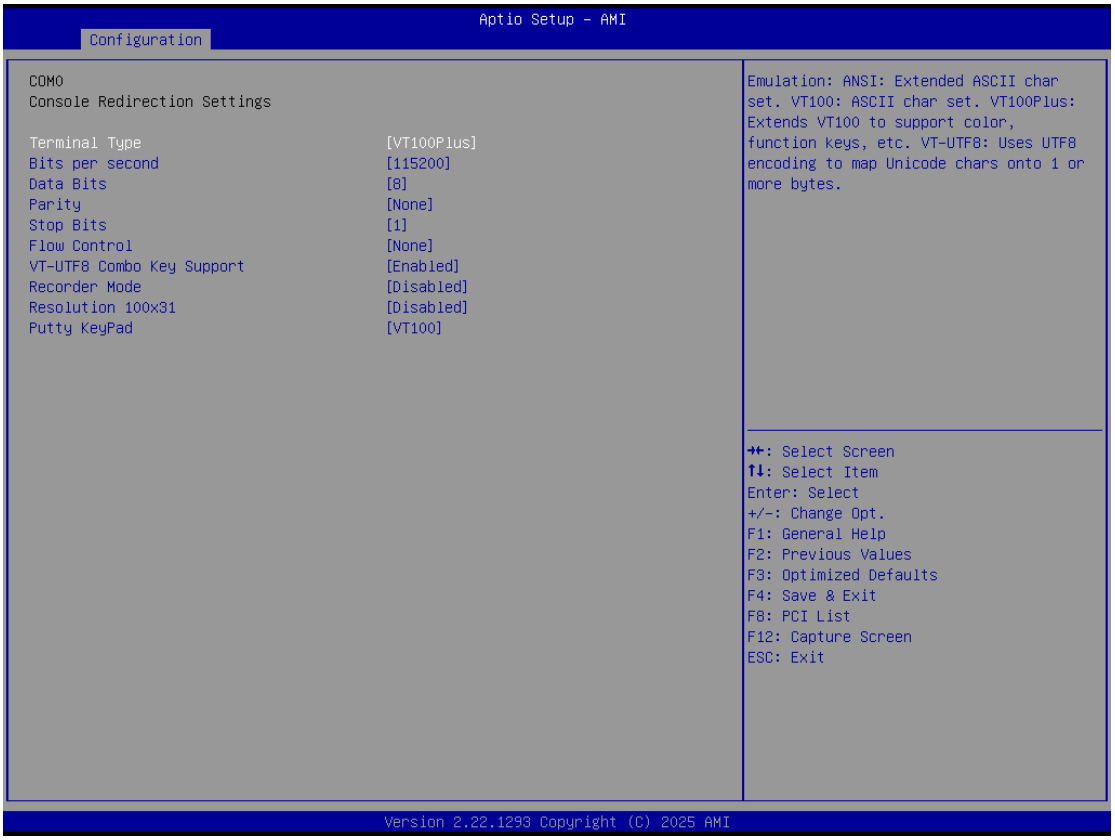
6.3.12 Serial Port Console Redirection



Feature	Description	Options
Console Redirection	Console Redirection Enable or Disable	★Disabled, Enabled

COM0 Console Redirection Settings:

The settings specify how the host computer and the remote computer (which the user is using) will exchange data. Both computers should have the same or compatible settings.

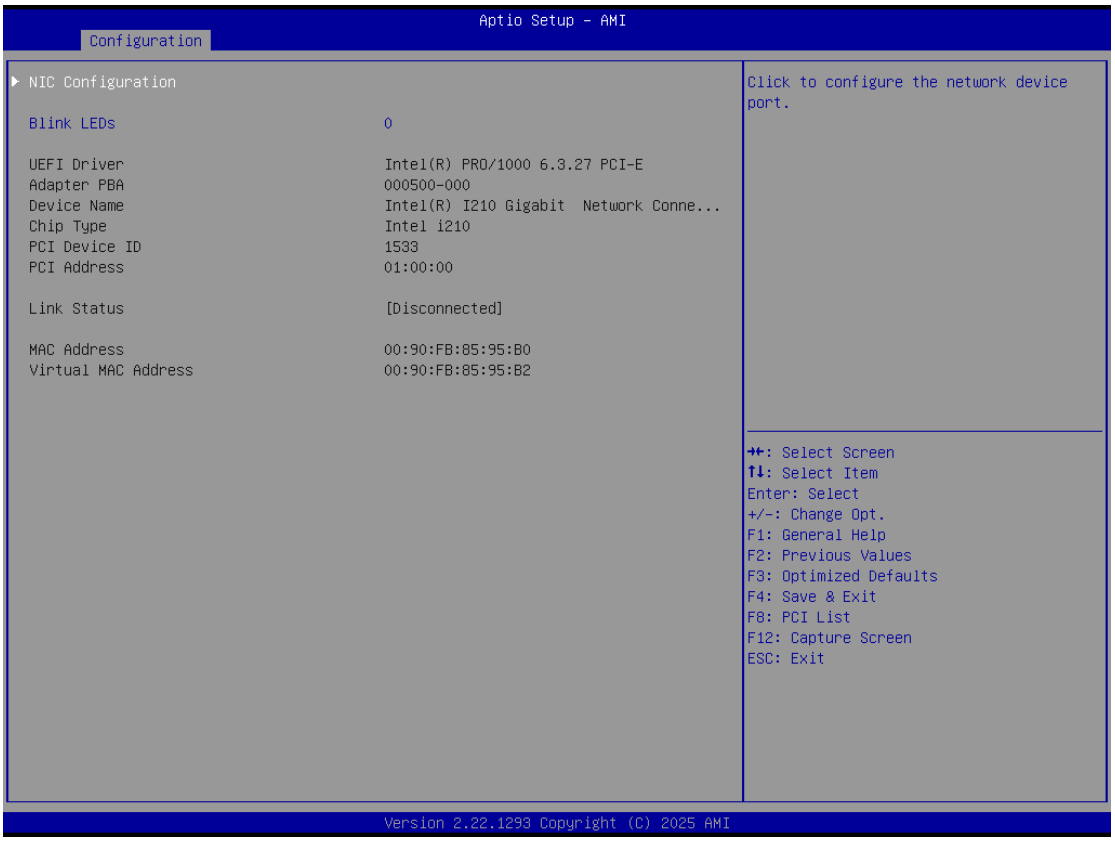


Feature	Description	Options
Terminal Type	Emulation: ANSI: Extended ASCII char set. VT100: ASCII char set. VT100Plus: Extends VT100 to support color, function keys, etc. VT-UTF8: Uses UTF8 encoding to map Unicode chars onto 1 or more bytes.	★VT100Plus, ANSI, VT100, VT-UTF8
Bits per second	Select Serial port transmission speed. The speed must be matched on other side. Long or noisy lines may require lower speeds.	★115200, 9600, 19200, 38400, 57600
Data bits	Data bits	★8, 7
Parity	A parity bit can be sent with the data bits to detect some transmission errors. Even: parity bit is 0 if the num of 1's in the data bits is even. Odd: parity bit is 0 if num of 1's in the data bits is odd. Mark: parity bit is always	★None, Even, Odd, Mark, Space

	1. Space parity bit is always 0. Mark and Space Parity do not allow for error detection. They can be used as an additional data bit.	

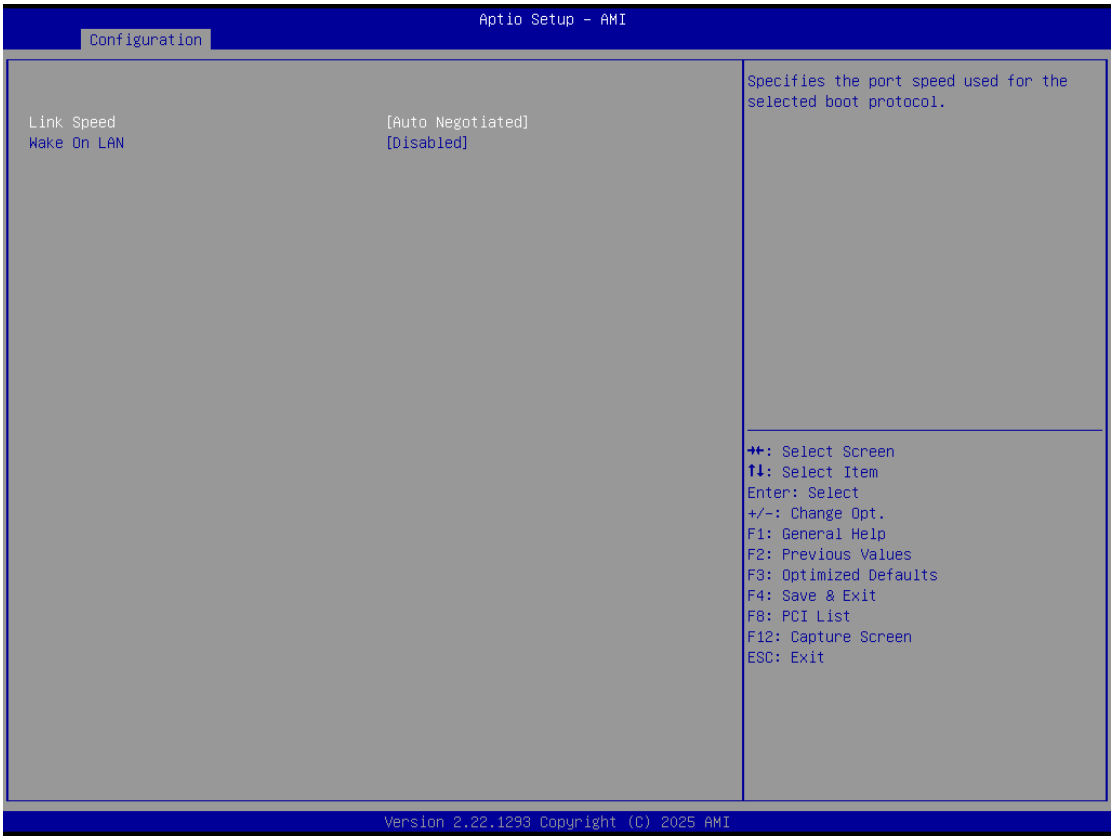
Feature	Description	Options
Stop Bits	Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may require more than 1 stop bit.	★1,2
Flow Control	Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signal.	★None, Hardware RTS/CTS
VT-UTF8 Combo Key Support	Enable VT-UTF8 Combination Key Support for ANSI/VT100 terminals	Disabled, ★Enabled
Recorder Mode	With this mode enabled only text will be sent. This is to capture Terminal data.	★Disabled, Enabled
Resolution 100x31	Enables or disables extended terminal resolution	★Disabled, Enabled
Putty KeyPad	Select FunctionKey and KeyPad on Putty	★VT100, LINUX, XTERMR6, SCO, ESCN, VT400

6.3.13 Intel (R) I210 Gigabit Network Connection – 00:90:FB:85:95:B2



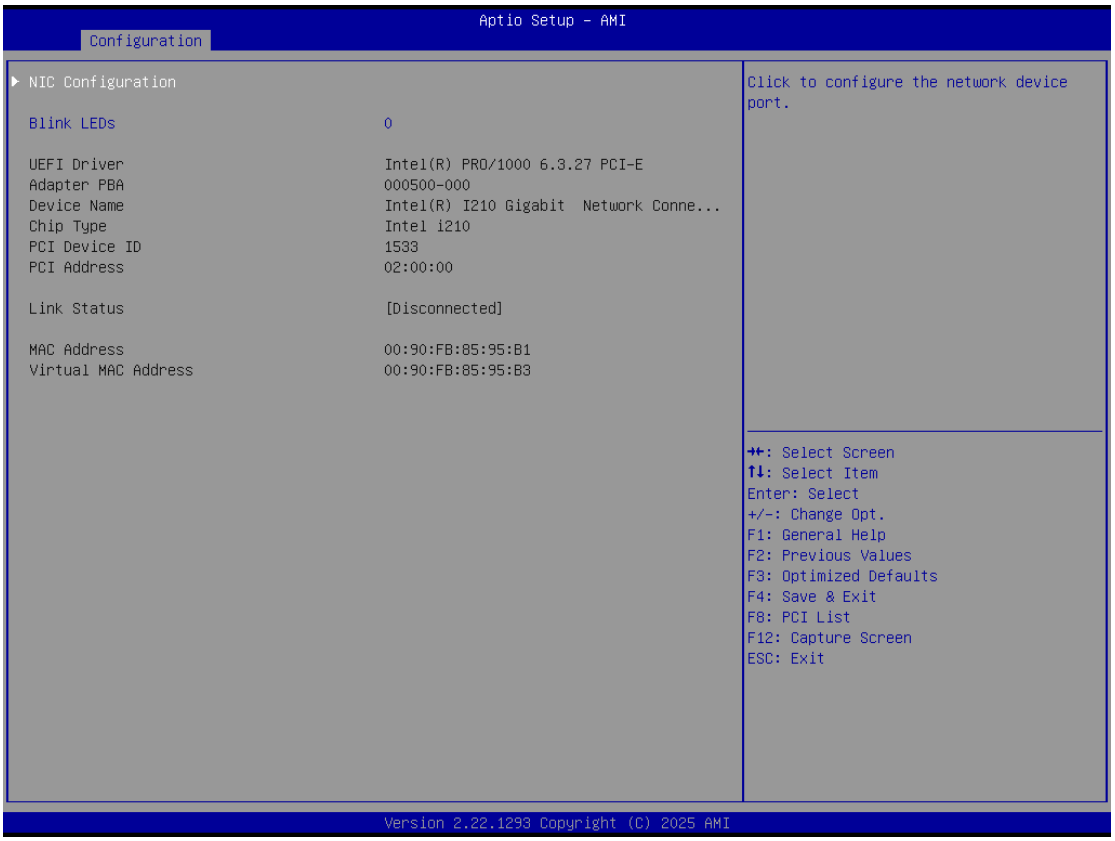
Feature	Description	Options
Blink LEDs	Identify the physical network port by blinking the associated LED.	★0

NIC Configuration



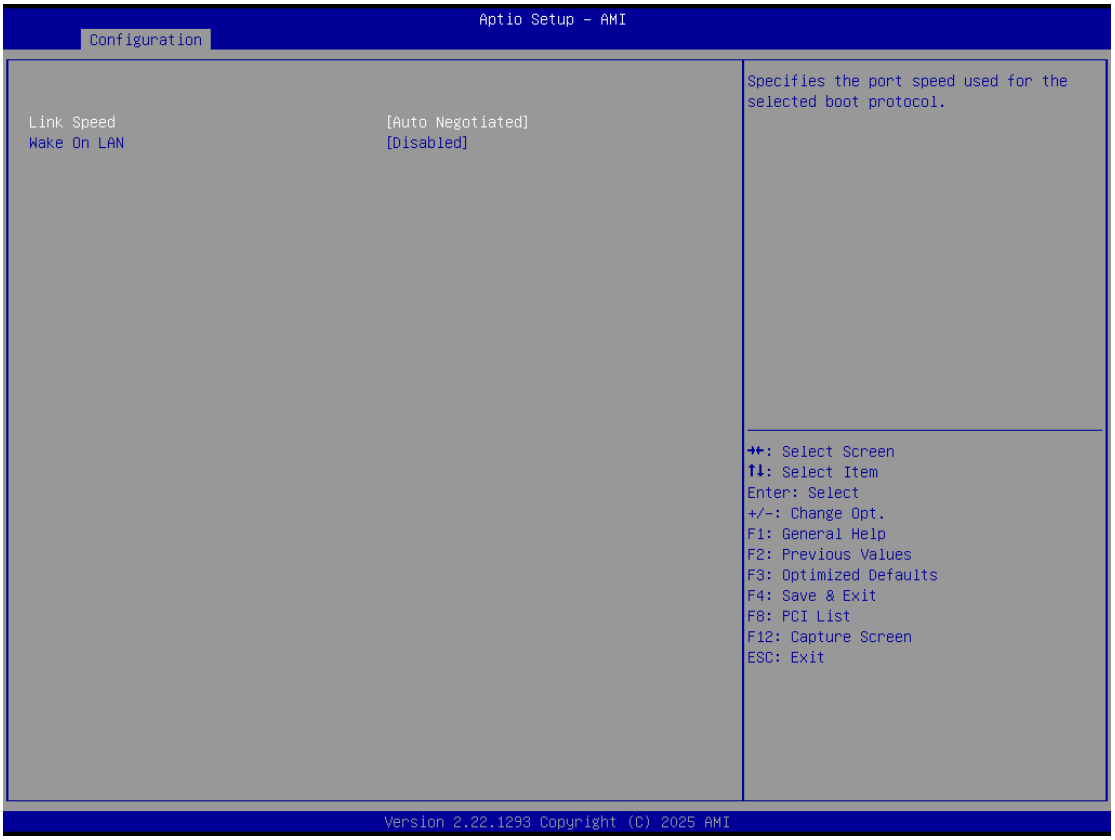
Feature	Description	Options
Link Speed	.Specifies the port speed used for the selected boot protocol.	★Auto Negotiated, 10 Mbps Half, 10 Mbps Full, 100 Mbps Half, 100 Mbps Full
Wake On Lan	Enables the server to be powered on using an in-band magic packet.	★Disabled, Enabled

6.3.14 Intel (R) I210 Gigabit Network Connection – 00:90:FB:85:95:B3



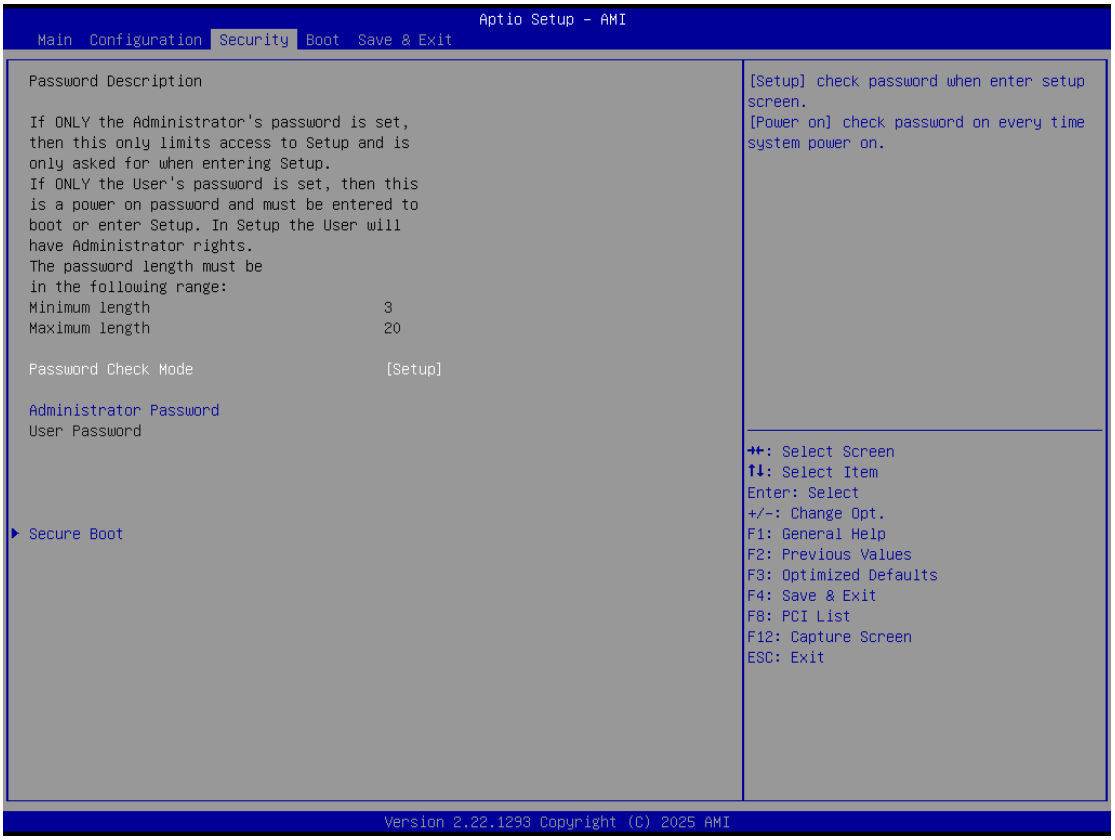
Feature	Description	Options
Blink LEDs	Identify the physical network port by blinking the associated LED.	★0

NIC Configuration



Feature	Description	Options
Link Speed	.Specifies the port speed used for the selected boot protocol.	★Auto Negotiated, 10 Mbps Half, 10 Mbps Full, 100 Mbps Half, 100 Mbps Full
Wake On Lan	Enables the server to be powered on using an in-band magic packet.	★Disabled, Enabled

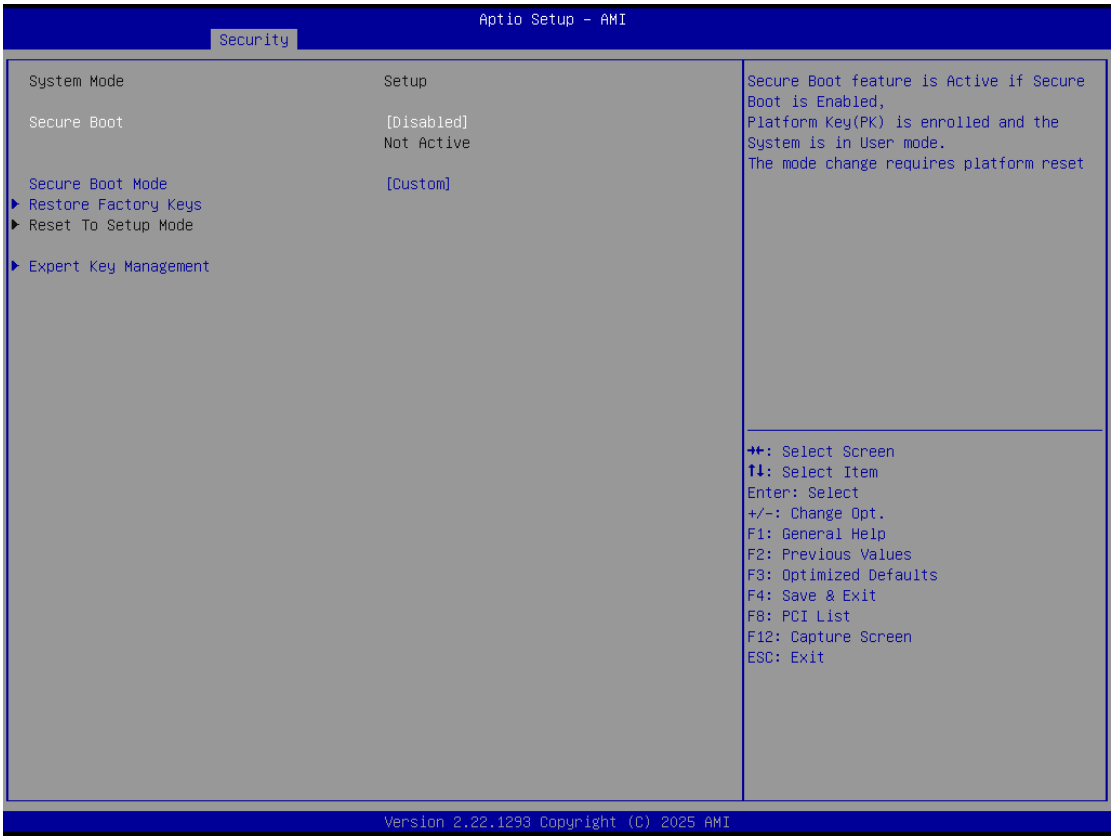
6.4 Security



Feature	Description	Options
Password Check Mode	[Setup] check password when enter setup screen. [Power on] check password on every time system power on.	★Setup, Power On
Administrator Password	Set Administrator Password	
Secure Boot	Secure Boot configuration	

Secure Boot

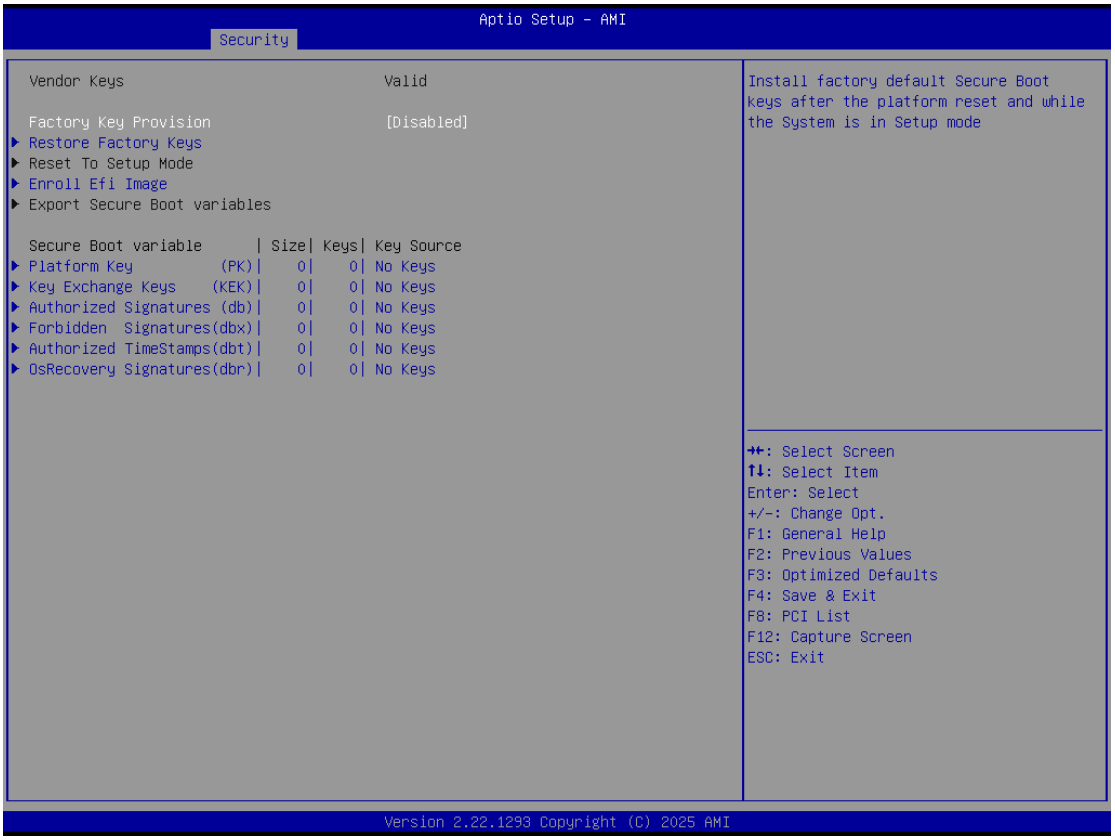
Secure Boot configuration



Feature	Description	Options
Secure Boot	Secure Boot feature is Active if Secure Boot is Enabled, Platform Key (PK) is enrolled and the System is in User mode. The mode change requires platform reset.	★Disabled, Enabled
Secure Boot Mode	Secure Boot Mode options: Standard or Custom. In Custom mode, Secure Boot Policy variables can be configured by a physically present user without full authentication	★Custom, Standard
Restore Factory keys	Force System to User Mode. Install factory default Secure Boot key databases	Yes, No
Key Management	Enables expert users to modify Secure Boot Policy variables without variable authentication	

Key Management

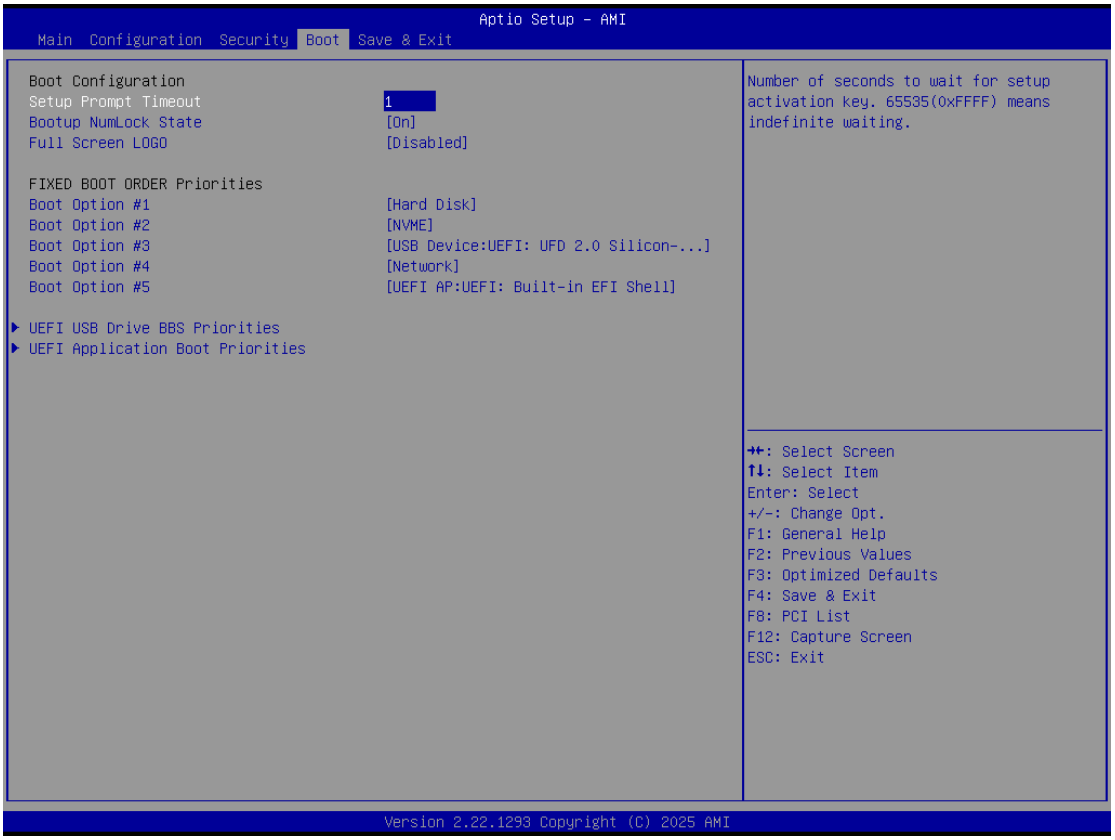
Enables expert users to modify Secure Boot Policy variables without variable authentication



Feature	Description	Options
Factory keys Provision	Install factory default Secure Boot key after the platform reset and while the System is in Setup mode.	★Disabled, Enabled
Restore Factory keys	Force System to User Mode. Install factory default Secure Boot key databases	Yes, No
Enroll Efi Image	Allow Efi image to run in Secure Boot mode. Enroll SHA256 Hash certificate of a PE image into Authorized Signature Database (db)	

Feature	Description	Options
Platform Key(PK) Key Exchange Keys(KEK) Authorized Signatures (db) Forbidden Signatures (dbx) Authorized TimeStamps (dbt) OsRecovery Signatures (dbr)	Enroll Factory Defaults or load certificates from a file: 1.Public Key Certificate: a)EFI_SIGNATURE_LIST b) EFI_CERT_X509 (DER) c) EFI_CERT_RSA2048 (bin) d)EFI_CERT_SHAXXX 2.Authenticated UEFI Variable 3.EFI PE/COFF Image(SHA256) Key Source: Factory, Modified, Mixed	

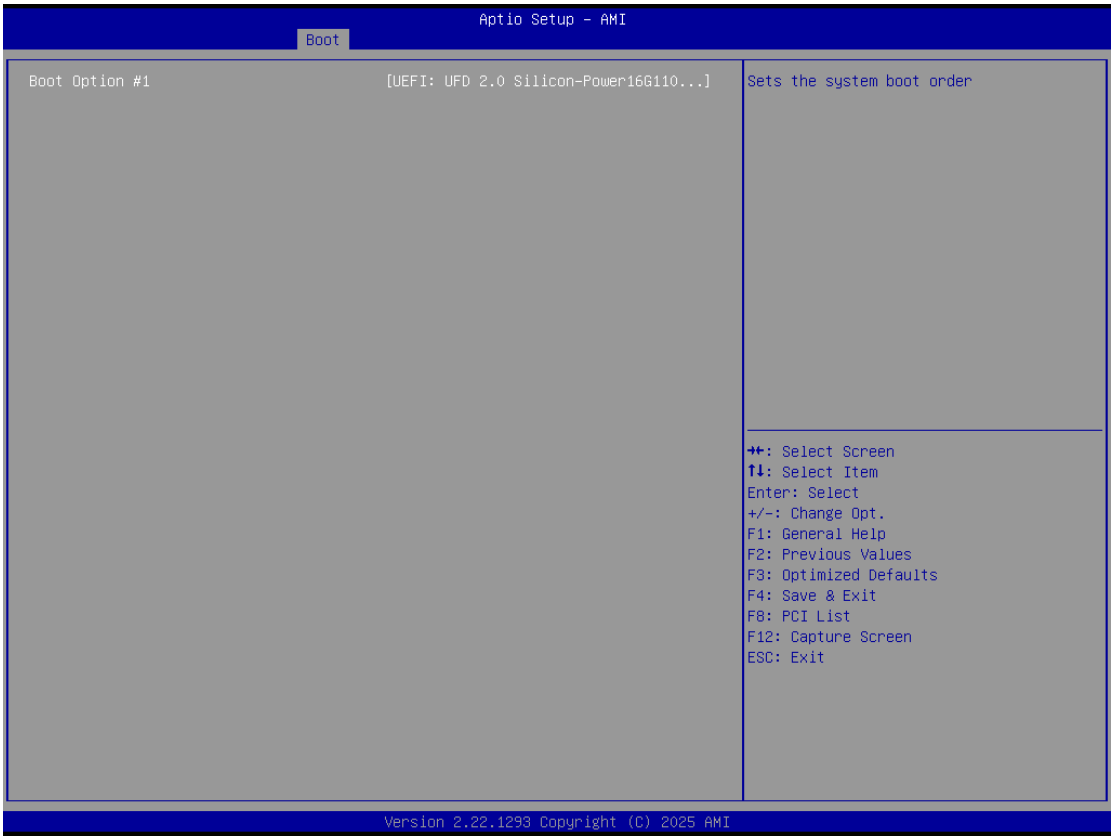
6.5 Boot



Feature	Description	Options
Setup Prompt Timeout	Number of seconds to wait for setup activation key. 65535(0xFFFF) means indefinite waiting.	★1
Bootup NumLock State	Select the keyboard NumLock state.	★On, Off
Full Screen LOGO	Enables or disables Quiet Boot option and Full screen Logo.	★Disabled, Enabled
Boot Option #1 ~ #5	Sets the system boot order	Hard Disk, NVME, USB Device, Network, UEFI AP: UEFI: Built-in EFI Shell, Disabled
UEFI USB Drive BBS Priorities	Specifies the Boot Device Priority sequence from available UEFI USB Drivers.	
UEFI Application Boot Priorities	Specifies the Boot Device Priority sequence from available UEFI Application	

UEFI USB Drive BBS Priorities:

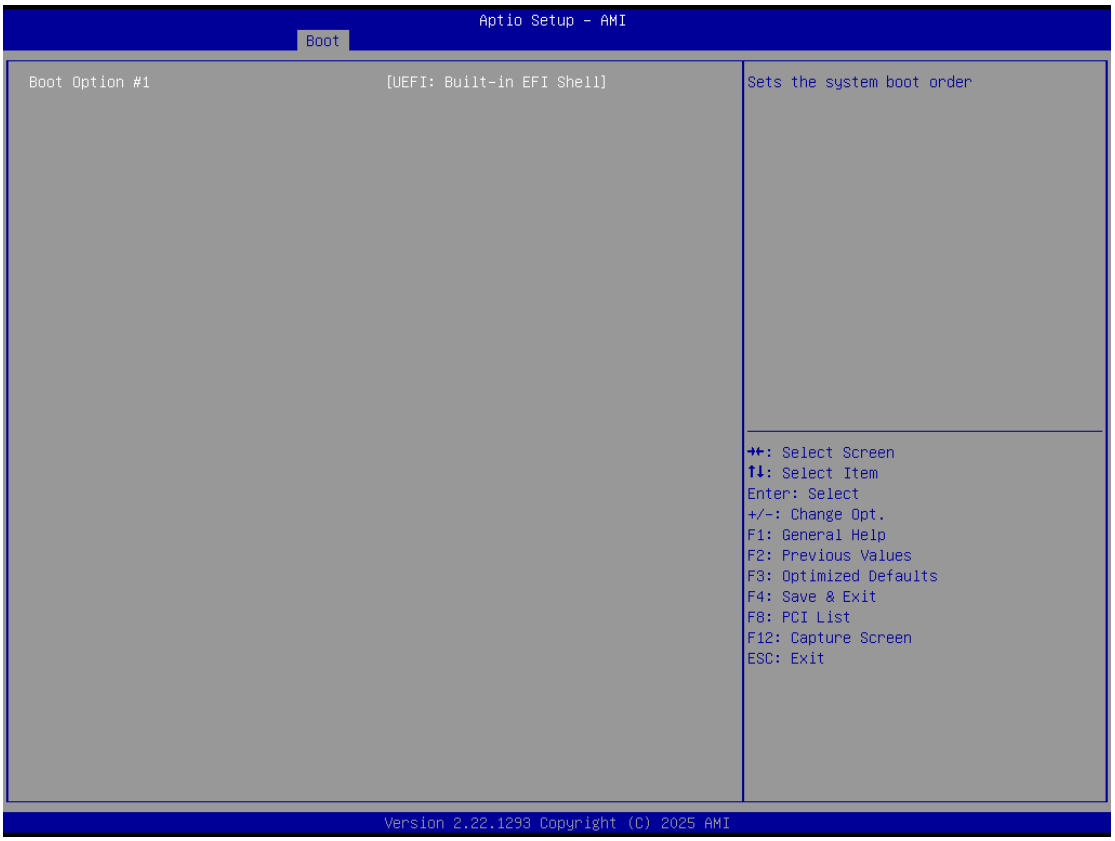
Specifies the Boot Device Priority sequence from available UEFI Hard Drive Application.



Feature	Description	Options
Boot Option #1	Sets the system boot order.	

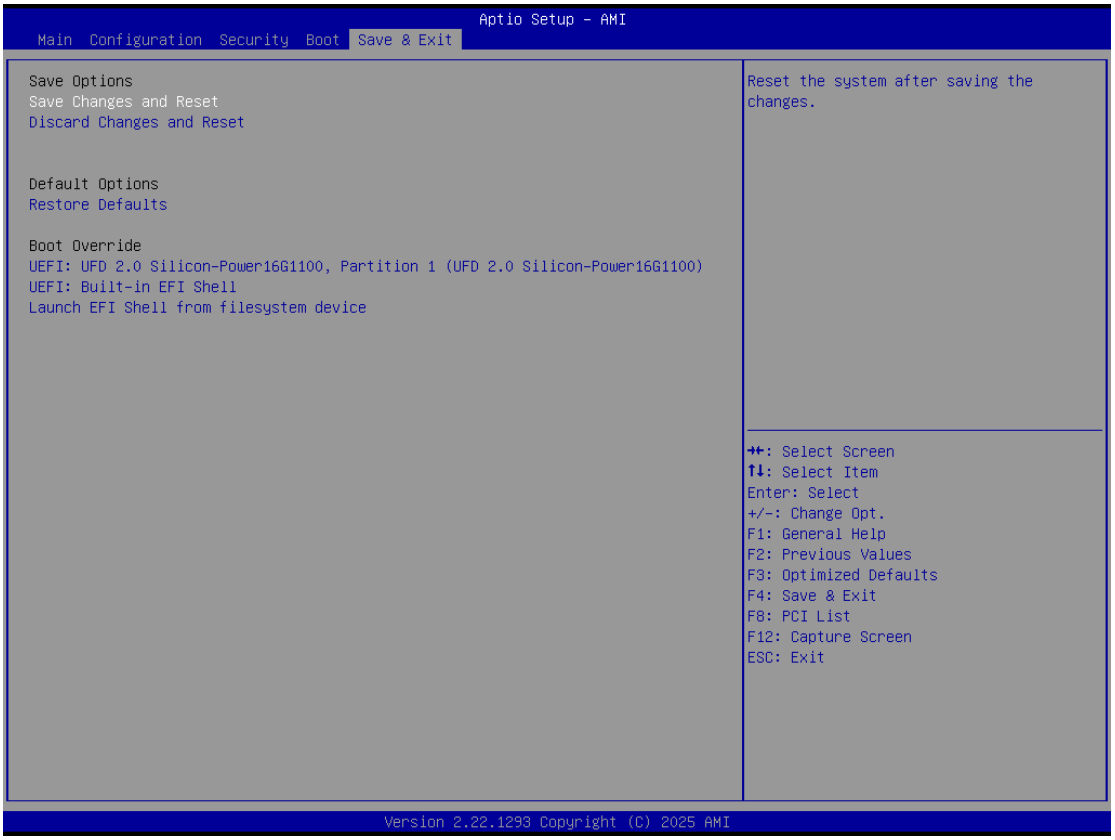
UEFI Application Boot Priorities:

Sets the system boot order.



Feature	Description	Options
Boot Option #1	Sets the system boot order.	

6.6 Save& Exit



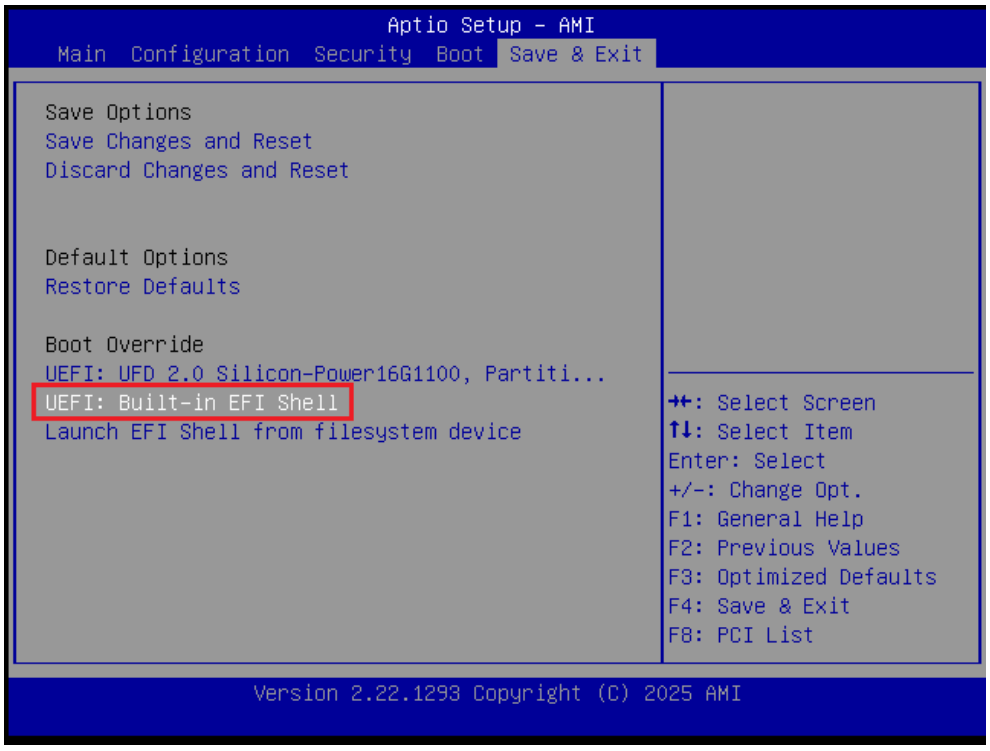
Feature	Description	Options
Save Changes and Reset	Reset the system after saving the changes.	
Discard Changes and Reset	Reset system setup without saving any changes.	
Restore Defaults	Restore/Load Default values for all the setup options.	
UEFI: Built-in EFI Shell		
Launch EFI Shell from filesystem device	Attempts to Launch EFI Shell application (Shell.efi) from one of the available filesystem devices.	

PICO-8020 BIOS UEFI Update SOP process under UEFI Shell

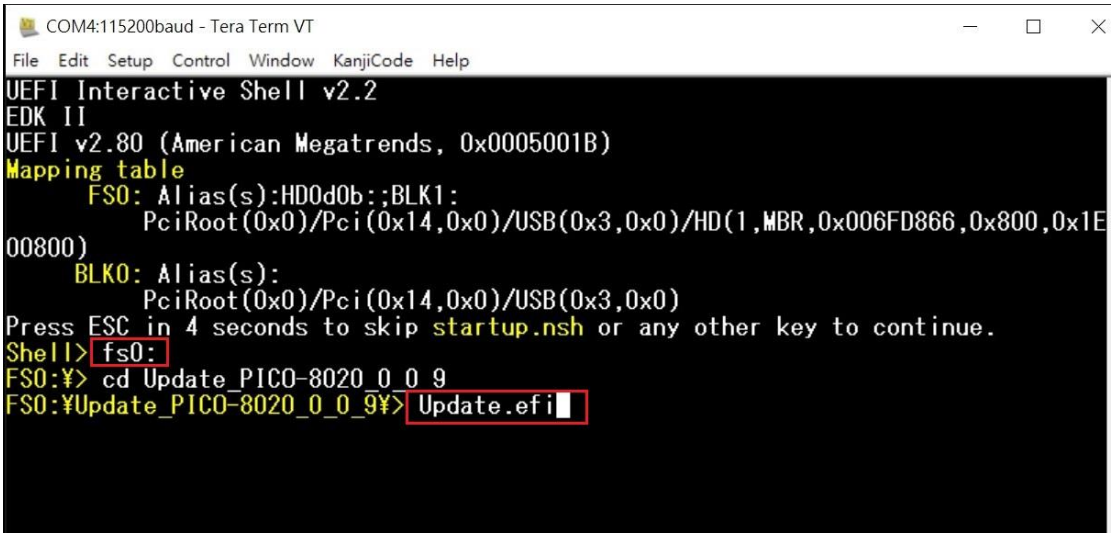
Step1. Prepare a USB DOK.

Step2. Unzip BIOS update file to the USB DOK.

Step3. Plug the USB DOK into the target system and then boot in UEFI Shell By selecting UEFI: Built-In EFI shell in the BIOS save & Exit page.



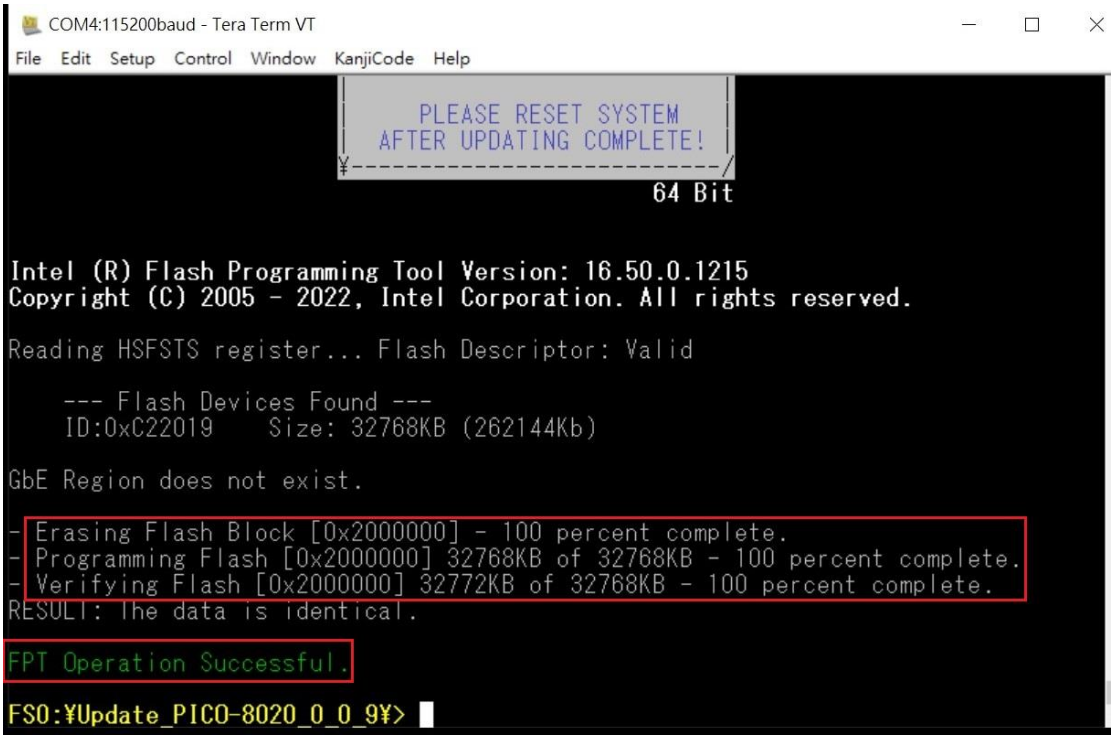
Step4. Under the UEFI shell, direct to your USB DOK, below picture is an example using FS0. Then direct to the folder with BIOS updated file and then enter command:" Update.efi" to start updating BIOS.



Step5. The updating process will start, and you can see the updating progress.

When you see the following pictures, which means the BIOS update processes finished.

Please cut the AC power off and wait for 10 seconds before powering on.



Chapter 7

System Overview

7 System Resources
7.1 Intel Twin Lake SoC
7.2 Main Memory
7.3 Installing the Single Board Computer

7. System Resources

7.1 Intel® Twin Lake & Amston Lake Soc

Intel® Processor N150 (4C, 0.8GHz, 6W)
Intel® Atom x7433RE (4C, 1.5GHz, 9W)
Intel® Atom x7211RE (2C, 1.0GHz, 6W)

7.2 Main Memory

PICO-8020 provides 1x 262-pin SO-DIMM sockets which supports DDR5 non-ECC memory. The maximum memory can be up to 16GB. Memory clock and related settings can be detected by BIOS via SPD interface.

7.3 Installing the Single Board Computer

To install your PICO-8020 into standard chassis or proprietary environment, please perform the following:
Step 1: Check that all jumper settings are in the correct positions.
Step 2: Install and configure the memory module in the proper slot.
Step 3: Install the heat spreader or heat sink in the correct position.
Step 4: Place the PICO-8020 into the designated position in the system.
Step 5: Attach cables to the existing peripheral devices and secure them.
WARNING

Please ensure that motherboard is properly inserted and fixed by mechanism.

Chapter 8

System Overview

8 Troubleshooting
8.1 Hardware Quick Installation
8.2 BIOS Setting
8.3 FAQ

8. Troubleshooting

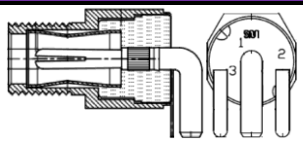
This chapter provides a few useful tips to quickly get PICO-8020 running with success.

8.1 Hardware Quick Installation

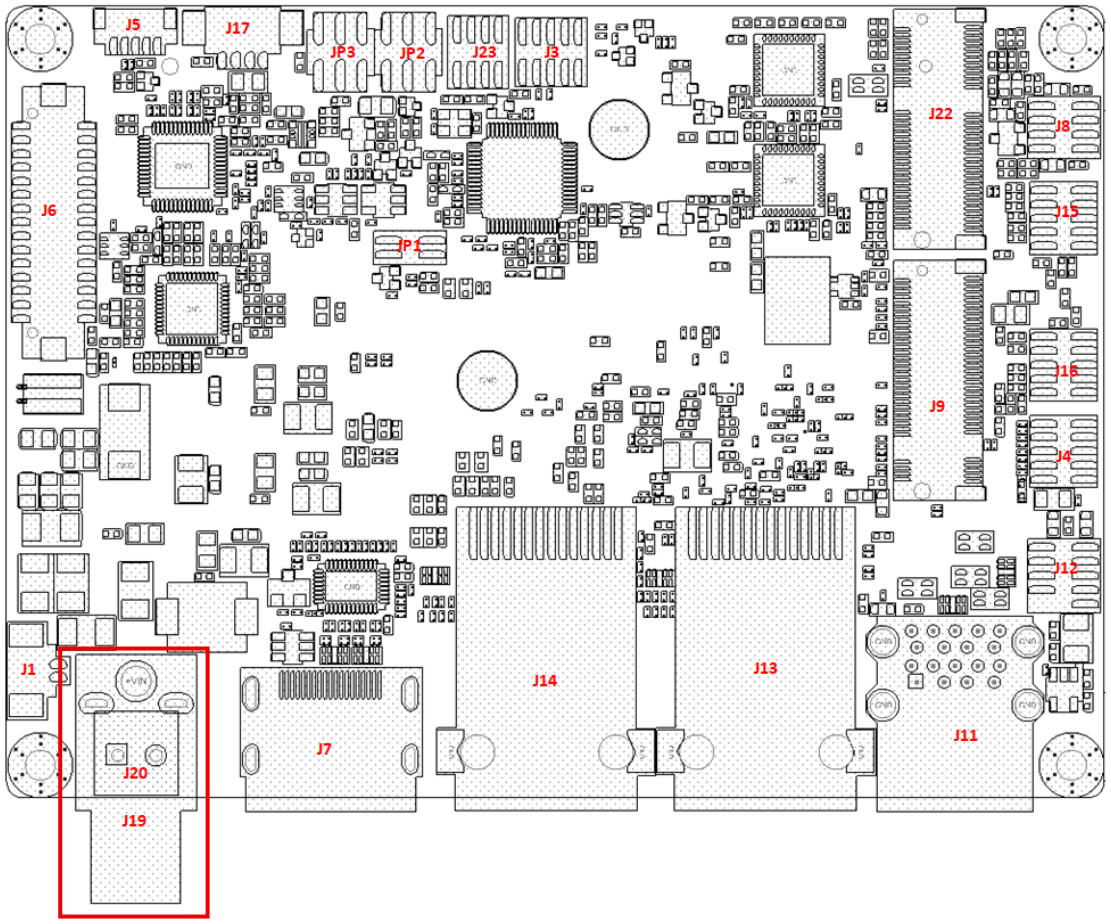
DC Jack Power

PICO-8020 is powered via a DC Jack connector, supporting a wide input voltage range from 12V to 24V.

J19 : DC Jack

PCB Footprint	Pin No.	Signal Description	Pin No.	Signal Description
	1	Vin	3	GND
	2	GND		

Connector



8.2 BIOS Setting

It is assumed that users have correctly adopted modules and connected all the devices cables required before turning on DC power.

262-pin DDR5 4800MT/s SO-DIMM Memory, keyboard, mouse, M.2 M-key storage, HDMI connector, device power cables, DC jack accessories are good examples that deserve attention. With no assurance of properly and correctly accommodating these modules and devices, it is very possible to encounter system failures that result in malfunction of any device.

To make sure that you have a successful start with PICO-8020, it is recommended, when going with the boot-up sequence, to hit “DEL” and ”ESC” key and enter the BIOS

setup menu to tune up a stable BIOS configuration so that you can wake up your system far well.

Loading the default optimal setting

When prompted with the main setup menu, please scroll down to “RestoreDefaults”, press “Enter” and select “Yes” to load default optimal BIOS setup.

This will force your BIOS setting back to the initial factory configurations. It is recommended to do this so you can be sure the system is running with the BIOS setting that Portwell has highly endorsed. As a matter of fact, users can load the default BIOS setting at any time when system appears to be unstable in boot up sequence.

8.3 FAQ

Information & Support

● Question: I forgot my password for system BIOS, what am I supposed to do?

Answer: You can switch off your power supply then find the RTC Battery on PICO-8020. Then remove the RTC battery and wait 5 seconds to clean your password then to switch on your power supply.

● Question: How to update the BIOS file of PICO-8020?

Answer:

1. Please visit the web site of Portwell download center as below hyperlink https://download.portwell.tw/
2. Select “Search download” and type the keyword “PICO-8020”.
3. Find the “BIOS “page and download the ROM file and flash utility.
4. Unzip file to bootable USB flash drive which can boot to shell mode. Then execute the “update.efi”. It will start to update BIOS.
5. When you see the “FPT Operation Passed” message, which means the BIOS update processes finished. Please cut the AC power off and wait for 10 seconds before powering on.
6. If you have other additional technical information or requests which are not covered in this manual, please fill in the technical request form as below hyperlink. https://www.portwell.com.tw/support-center/service-request/
We will do our best to provide a suggestion or solution for you.

Chapter 9

System Overview

9 Portwell Software Service

9. Portwell Software Service

1. If you have customized requirements of BIOS, you can contact people from our company or branch.
2. If you have requirements of WDT、GPIO APP, you can contact our headquarter or branch, and we can render your assistance on developing.
https://www.portwell.com.tw/portwell-worldwide/

Portwell

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