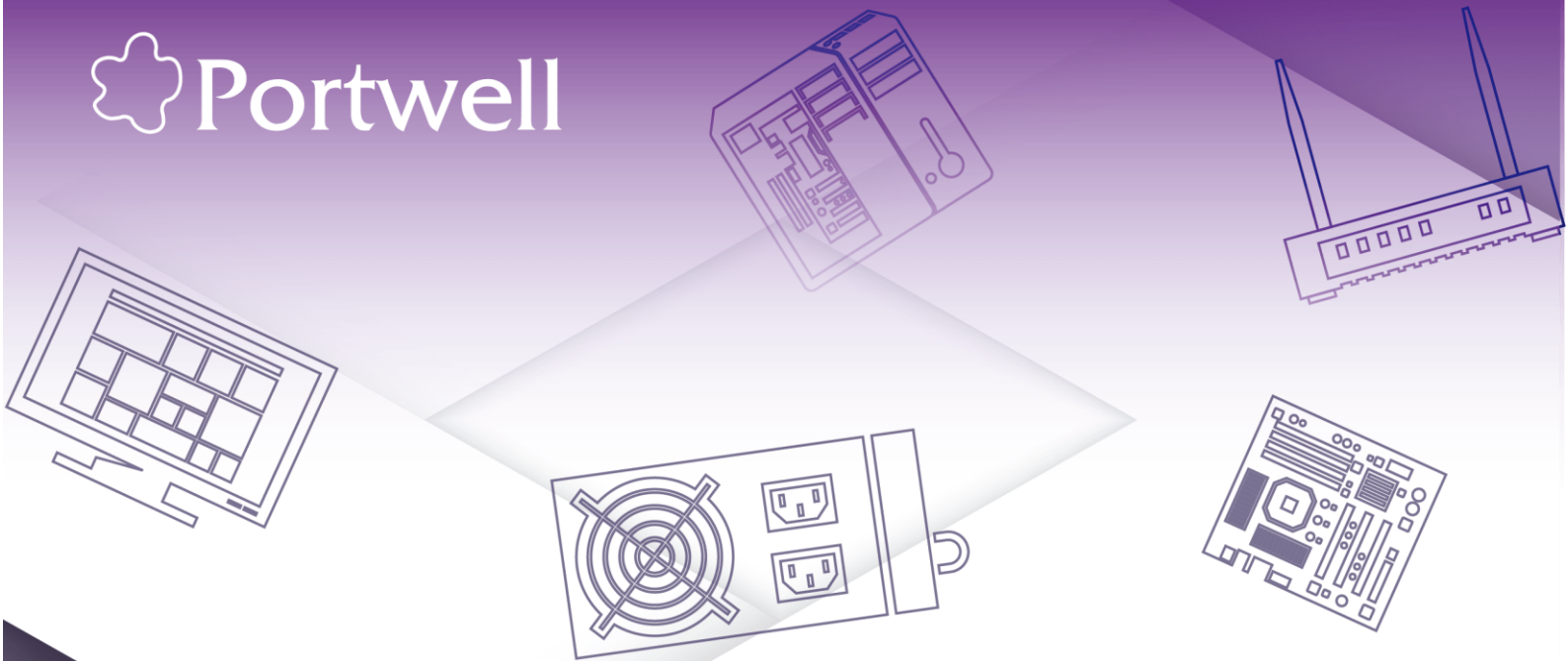
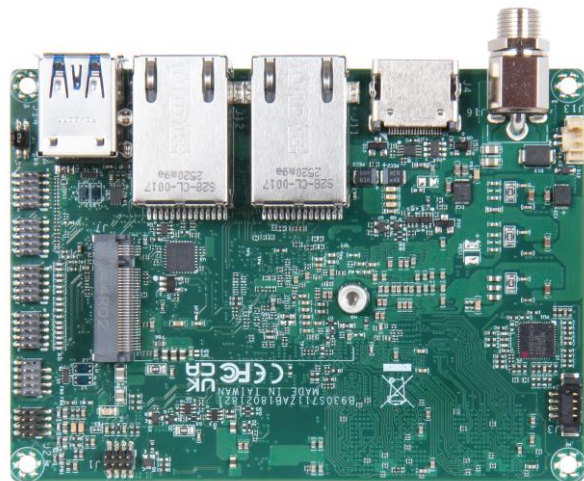




PICO-8021 Series

PICO-ITX Embedded Board

User Manual

Version R 1.1

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Revision History

R 1.0	Official Release Rev. 1.0
R1.1	<ol style="list-style-type: none">1. Add a warning regarding thermal kit usage in Section 2 (Specifications) and Section 2.4 (Environmental Specifications)2. Modify the motherboard installation steps and recommend using a thermal kit in Section 7.3 (Installing the Single Board Computer)3. Remove the DC-in Colay 2-pin terminal block from Section 2 (Specifications)

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Chapter 1

System Overview

1 Introduction

1. Introduction

The PICO-8021 is a high-performance, ultra-compact, fanless SBC based on the PICO-ITX form factor, featuring Intel® Twin Lake and Amston Lake processors, including the Intel® Processor N150 and Atom® x7433RE/x7211RE. It delivers exceptional computing and graphics capabilities while maintaining low power consumption, making it ideal for space-constrained edge applications.

Designed with versatility in mind, the PICO-8021 supports onboard LPDDR5 memory (up to 16GB) and one M.2 M-Key (2242) slot for PCIe or SATA storage. Powered by Intel® Gen12 UHD Graphics with up to 32 execution units (EUs), it supports a single display via HDMI 1.4. Feature-rich and robust, the board provides dual Intel® Gigabit Ethernet ports, dual USB 3.2 Gen2, dual RS-232, audio I/O, GPIO, and onboard TPM 2.0. Its wide operating temperature range (-40° C to 85° C for industrial SKUs) ensures reliable performance in harsh environments.

Whether deployed in medical equipment (e.g., ward monitoring systems, operating room displays), retail and self-service terminals, or industrial automation scenarios (e.g., environmental monitoring, production line dashboards), the PICO-8021 empowers developers to build reliable, intelligent, and connected systems with ease.

Chapter 2

System Overview

- 2 Specifications
 - 2.1 Supported Operating Systems
 - 2.2 Mechanical Dimensions
 - 2.3 Power Consumption
 - 2.4 Environmental Specifications

2. Specifications

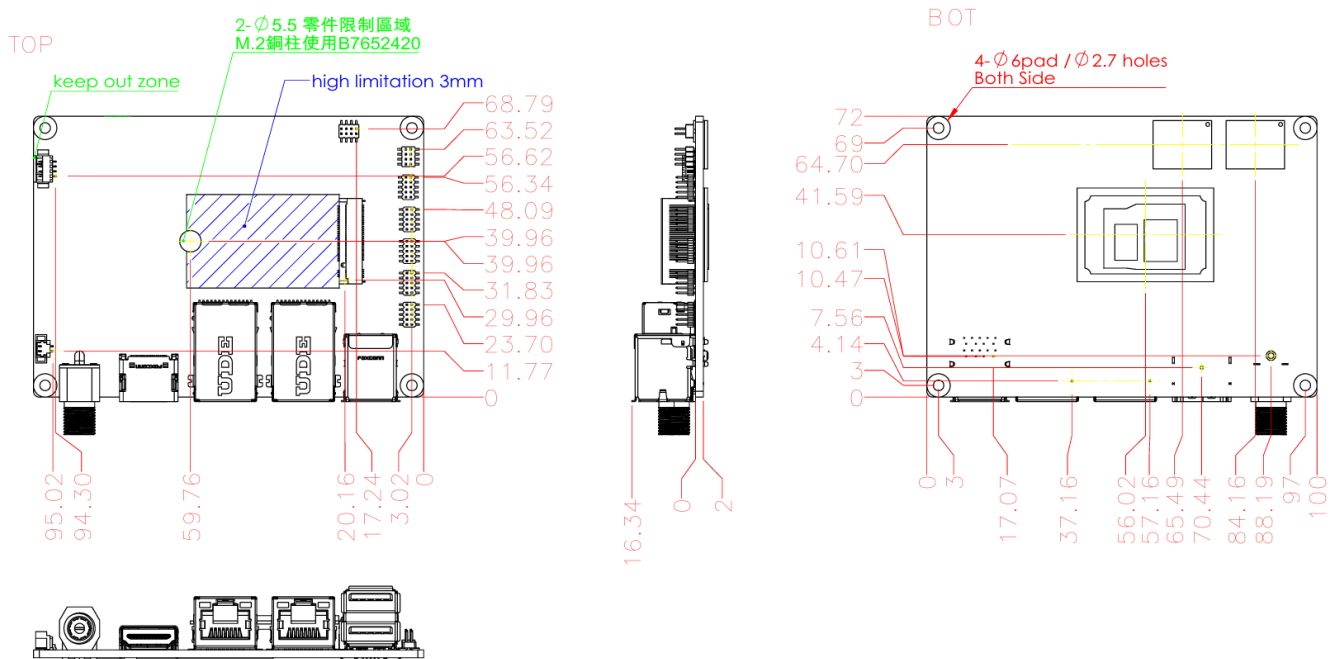
Main Processor	Intel® Processor N150 Intel® Atom x7433RE Intel® Atom x7211RE
System BIOS	AMI UEFI BIOS
Main Memory	LPDDR5 8GB up to 16GB
Graphics	Intel® Graphics Gen12 with up to 24 EUs HDMI: 1x HDMI port on rear I/O (HDMI 1.4, 3840x2160 @ 30Hz)
Expansion Interface	NA
Storage Interface	1x M.2 M key 2242
Input/Output	Serial Port: 2x RS-232 port 2x USB 3.2 Gen2 on rear I/O, 2x USB 2.0 on board pin header Audio Interface: line-in, line-out, mic-in on board pin header 1x 4-pin smart fan header
Ethernet	2x Intel® GbE Controller(I210) 2x RJ45 connectors on rear I/O
High Drive GPIO	1x pin-header for GPIO(8bit)
Mechanical and environmental specifications	Operating temperature: 0 ~ 60° C (Twin Lake)/ -40 to +85° C (Asmton Lake) Storage temperature: -40 ~ 85° C Humidity: 5 ~ 95% non-condensing Power supply voltage: 12 ~24V DC jack on rear I/O Board size: 100mm x 72 mm (3.94" x 2.83") ※Please be sure to use active or passive heat dissipation equipment
Certification	CE/FCC

2.1 Supported Operating Systems

The PICO-8021 supports the following operating systems:

	Windows IoT Enterprise	Ubuntu
Twin Lake	Windows 11 LTSC (24H2)	24.04
Amston Lake	Windows 10 LTSC (21H2) Windows 11 LTSC (24H2)	22.04/24.04

2.2 Mechanical Dimensions



2.3 Power Consumption

Test Configuration	
CPU Type	Intel® Atom™ x7433RE 1.50GHz,L3:6MBytes
SBC BIOS	Portwell, Inc. PICO_8021_MED BIOS Rev.: 0.0.4 (082025)
Memory	On board LPDDR5 16GB 4800MT/s
Graphic Card	Intel® UHD Graphics
Graphic Driver	Intel® UHD Graphics, Version: 31.0.101.5081
LAN Card #1	Intel® I210 Gigabit Network Connection
LAN Driver #1	Intel® I210 Gigabit Network Connection, Version: 12.19.1.32

LAN Card #2	Intel® I210 Gigabit Network Connection #2
LAN Driver #2	Intel® I210 Gigabit Network Connection #2, Version: 12.19.1.32
Audio Card	Realtek High Definition Audio
Audio Driver	Realtek High Definition Audio, Version: 6.0.9239.1
Chip Driver	Intel® Chipset Device Software, Version: 10.1.19199.8340
USB 3.0 Driver	Intel® USB 3.10 eXtensible Host Controller – 1.20 (Microsoft), Version: 10.0.26100.1591
OS Edition	Windows 11 Pro (24H2)
Hard Drive	HFM128GD3HX015N
Power Supply	FSP040-1ADF03A
Boot Mode Select	UEFI

Power consumption(12V)				
Item		Power ON		Full Loading 10mins
DC in (+12V)		1.19A		1.17A
USB Port and the Spec.		Result		
USB 3.2 Gen1 Port J11		4.87 V/ 1.02 A		
USB 3.2 Gen1 Port J11		4.87 V/ 1.00 A		
USB 2.0 Port J12		4.87 V/ 0.57 A		
USB 2.0 Port J12		4.86 V/ 0.44 A		
Full USB port Loading Test (4)		USB 3.2 Gen1 Port J14 up : 4.86 V/ 0.96 A USB 2.0 Port J5 left : 4.81 V/ 0.57 A		
Item	S0	S3	S4	S5
DC in (+12V)	0.76A	0.29A	0.29A	0.29A

2.4 Environmental Specifications

Storage Temperature : 0 ~ 60° C (Twin Lake)/ -40 to +85° C (Asmtan Lake)

Operation Temperature : 0~60° C

Storage Humidity : 5~95%, non-condensing

Operation Humidity: 5~95%, non-condensing

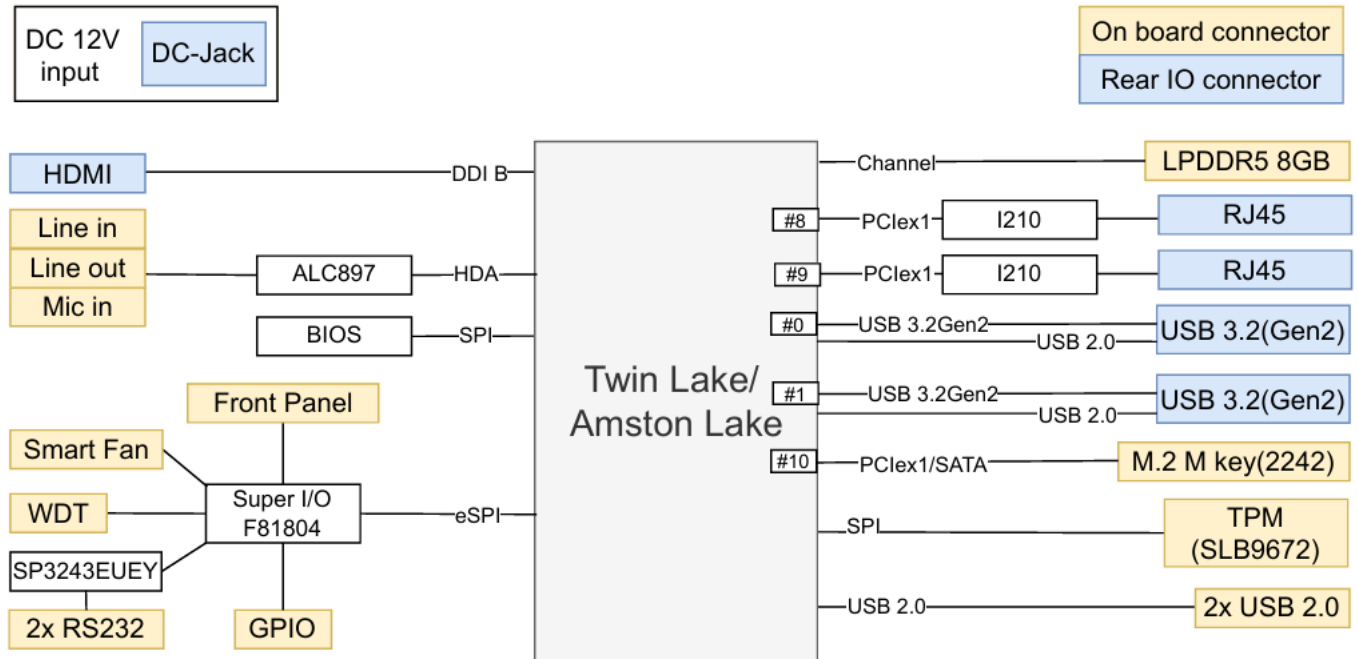
※Please be sure to use active or passive heat dissipation equipment

Chapter 3

System Overview

3 Block Diagram

3. Block Diagram



Chapter 4

System Overview

- 4 Hardware Configuration
 - 4.1 Drawing Overview
 - 4.2 Jumper Setting List
 - 4.3 Connector Function List

4. Hardware Configuration

This chapter indicates the locations of jumpers, headers, and connectors. Users may find useful information related to hardware settings in this chapter.

4.1 Drawing Overview

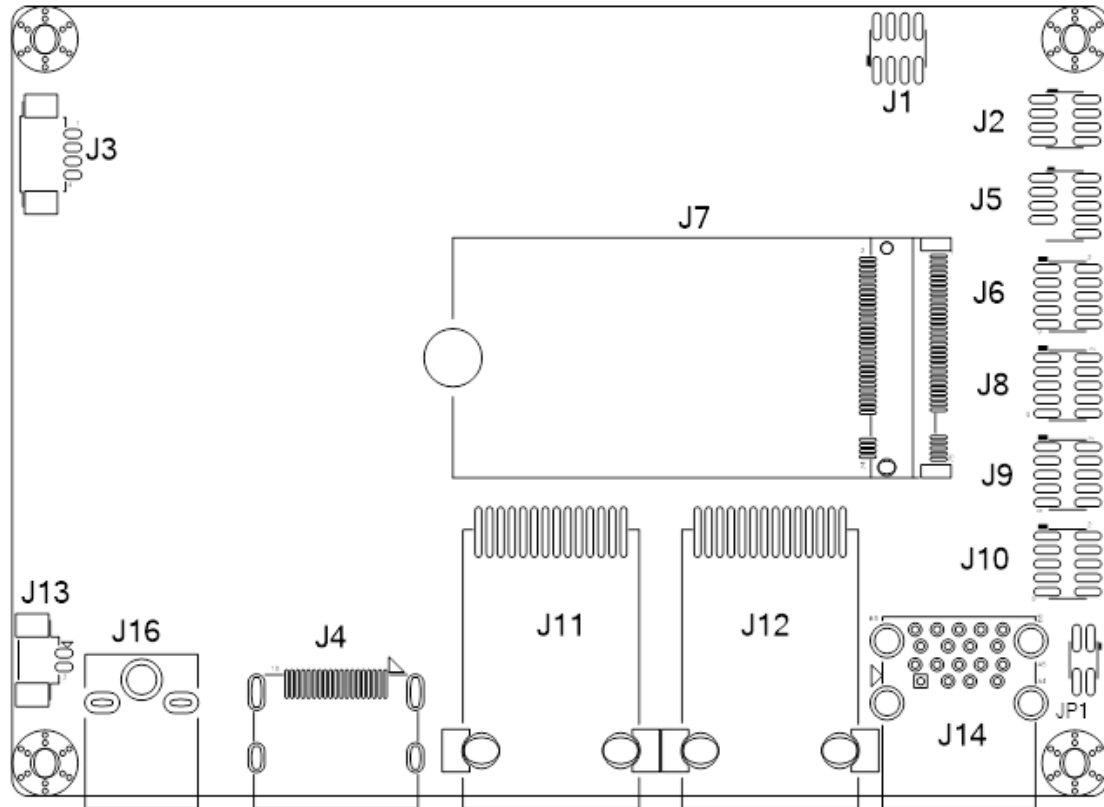


Figure1. PICO-8021 Top View

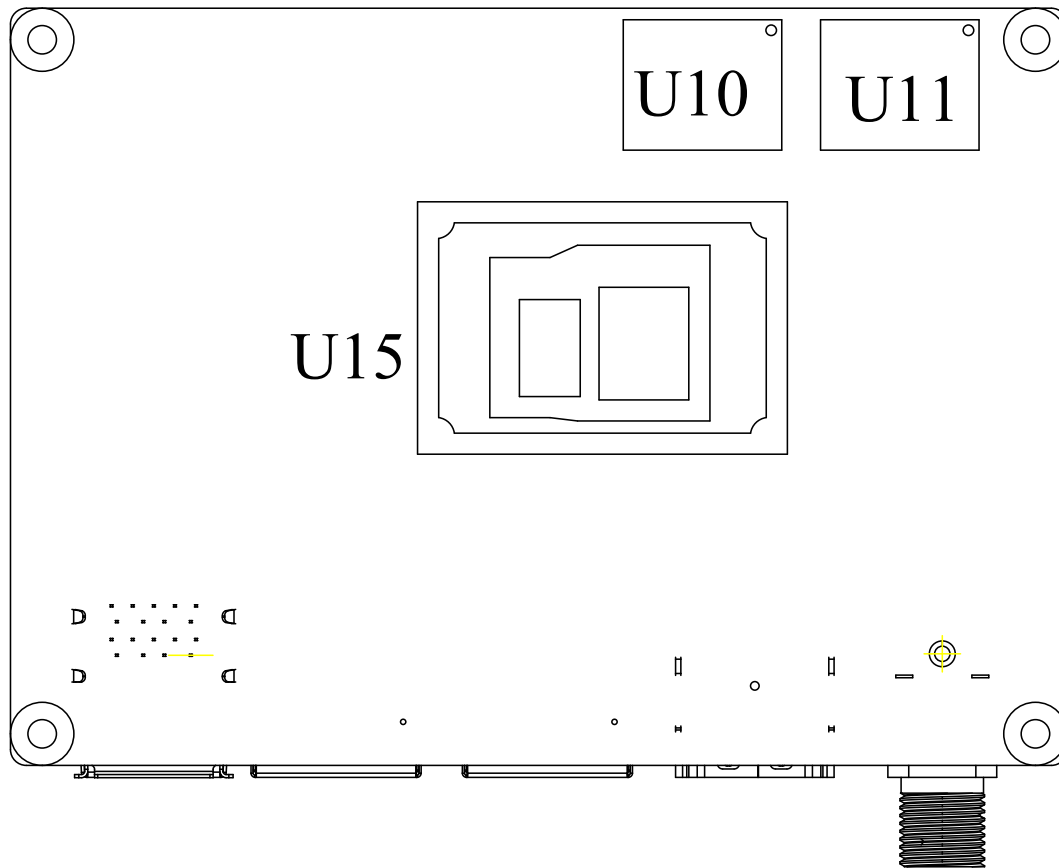


Figure1. PICO-8021 Bot View

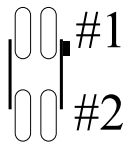
4.2 Jumper Setting List

For users to customize PICO-8021 features, the following sections define jumper settings. “Short” means covering the jumper pins with a jumper cap, while “Open” or “N/C” (Not Connected) means removing the jumper cap from the jumper pins. Users can refer to Figure 1 for jumper allocations.

Jump Function List:

Location	Connector	Function
JP1	Pin Header 2Px2 P=1.27mm 180D	Clear CMOS Jumper & AT & ATX mode

JP1: Clear CMOS Jumper & AT & ATX mode

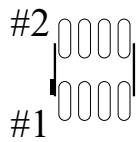


PIN No.	Signal Description
1-2 Short	Save CMOS (Default)
2-4 Short	Clear CMOS
3-4 Open	ATX MODE
3-4 Short	AT MODE (Default)

4.3 Connector Function List

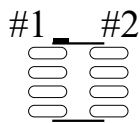
Jump	Function	Remark
J1	Front Panel Pin HDR	4x2 pin header P=1.27mm 180D
J2	External Audio (Mic + Line_in + Line_out)Pin HDR.	4x2 pin header P=1.27mm 180D
J3	FAN Connector	Wafer 4Px1 P=1.25mm 90D
J4	HDMI Port	
J5	USB2.0	Pin Header 5Px2(-9) P=1.27mm 180D
J6/J8	RS232	Pin Header 5Px2 P=1.27mm 180D
J7	M.2 key M Socket	
J9	80 Port	Pin Header 5Px2 P=1.27mm 180D
J10	GPIO	Pin Header 5Px2 P=1.27mm 180D
J11/J12	RJ45(1G)	
J13	Battery	Wafer 2Px1 P=1.25mm
J14	USB3.2 GEN2 X1	
J16	DC Jack	+12 Input

J1: Front Panel Pin HDR



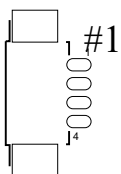
PIN No.	Signal Description	PIN No.	Signal Description
1	Power LED (+)	2	Power LED (-)
3	HDD LED (+)	4	HDD LED (-)
5	Reset (+)	6	Reset (-)
7	Power On(-)	8	Power On(+)

J2 : External Audio Connector



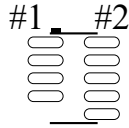
PIN No.	Signal Description	PIN No.	Signal Description
1	MIC_L	2	Line_in_L
3	Ground	4	Line_in_R
5	Line_out_L	6	Ground
7	Line_out_R	8	MIC_R

J3 : FAN



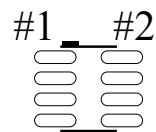
PIN No.	Signal Description	PIN No.	Signal Description
1	Ground	2	12V
3	CPU_FANIN	4	CPU_FANOUT

J5 : USB2.0



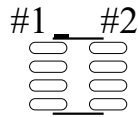
PIN No.	Signal Description	PIN No.	Signal Description
1	VUSB	2	VUSB
3	USB2_N	4	USB3_N
5	USB2_P	6	USB3_P
7	GND	8	GND
		10	NC

J6/J8 : RS232



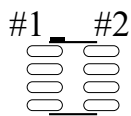
PIN No.	Signal Description	PIN No.	Signal Description
1	DCD	2	RXD
3	TXD	4	DTR
5	GND	6	DSR
7	RTS	8	CTS
9	RI	10	N/C

J9 : 80 Port



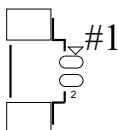
PIN No.	Signal Description	PIN No.	Signal Description
1	SEG_A	2	3.3V
3	SEG_B	4	SEG_E
5	SEG_C	6	SEG_F
7	SEG_D	8	SEG_G
9	SEG_L#	10	GND

J10 : GPIO



PIN No.	Signal Description	PIN No.	Signal Description
1	GPIO	2	GPO0
3	GPI1	4	GPO1
5	GPI2	6	GPO2
7	GPI3	8	GPO3
9	GND	10	3.3V

J13 : Battery



PIN No.	Signal Description	PIN No.	Signal Description
1	VBAT	2	GND

Chapter 5

System Overview

- 5 Sample Code
- 5.1 Watch Dog Timer
- 5.2 GPIO Signal

5. Sample Code

5.1 Watch Dog Timer

//F81804 WDT Sample Code

```
#Define SIO_Port_Index      0x2E
#Define SIO_Port_Data       0x2F
#Define WDT_LDN             0x07
#Define WDT_Config_offset   0xF5
#Define WDT_Time_offset     0xF6
#Define Time_Unit           0x00 //Time unit, 0=1 second, 1=60 second
#Define Time                 0x05 //Time, 5 second for example.
```

```
void Enter_F81804_SIO() {
```

```
    IoWrite8(SIO_Port_Index, 0x87);
```

```
    IoWrite8(SIO_Port_Index, 0x87);
```

```
    //Enter F81804 SIO
```

```
}
```

```
void Set_WDT_LDN() {
```

```
    IoWrite8(SIO_Port_Index, 0x07);
```

```
    IoWrite8(SIO_Port_Data, WDT_LDN);
```

```
}
```

```
void Set_Register(UINT8 offset, UINT8 And_Value, UINT8 OR_value) {
```

```
    UINT8 Temp;
```

```
    IoWrite8(SIO_Port_Index, offset);
```

```
    Temp=(IoRead8(SIO_Port_Data) & And_Value) | OR_Value;
```

```
    IoWrite8(SIO_Port_Data, Temp);
```

```
}
```

```
Byte Get_Register(UINT8 offset) {
```

```
    UINT8 Temp;
```

```
    IoWrite8(SIO_Port_Index, offset);
```

```
    Temp=IoRead8(SIO_Port_Data);
```

```
    return Temp;
```

```
}
```

```

void main()
{
    UINT8 Count_Time;

    Enter_F81804_SIO();
    Set_WDT_LDN();
    Set_Register(WDT_Config_offset,0xBF,0x40);          //Bit6: WDTMOUT_STS, Write 1
to clear Watchdog timeout event.
    Set_Register(WDT_Config_offset,0xF7,(Time_Unit<<3)); //Bit3: Set Time Unit, 0=1
second, 1=60 second
    Set_Register(WDT_Time_offset,0x00,Time);           //Set Time.
    Set_Register(WDT_Config_offset,0xDF,0x20);         //Bit5: 0=Disable WDT , 1=Enable
WDT.
    Count_Time=Get_Register(WDT_Time_offset);          //Read watchdog timer.
}

```

5.2 GPIO Signal

```

//F81804 GPIO Sample Code
#define SIO_Port_Index    0x2E
#define SIO_Port_Data     0x2F
#define GPIO_LDN    0x06
#define GPIO_IOSpace    0x0A00

#define GPO0_Output0x00 //GPO0 Output Mode, 0:Output Low, 1:Output High
#define GPO1_Output0x00 //GPO1 Output Mode, 0:Output Low, 1:Output High
#define GPO2_Output0x00 //GPO2 Output Mode, 0:Output Low, 1:Output High
#define GPO3_Output0x00 //GPO3 Output Mode, 0:Output Low, 1:Output High
#define GPIO_Offset  0x06 //GPIO offset
#define GPI1_Offset  0x07 //GPI1 offset
#define GPI3_Offset  0x03 //GPI3 offset

void Enter_F81804_SIO() {
    IoWrite8(SIO_Port_Index, 0x87);
    IoWrite8(SIO_Port_Index, 0x87);
}

```

```
//Enter F81804 SIO
}

void Set_GPIO_LDN() {
    IoWrite8(SIO_Port_Index, 0x07);
    IoWrite8(SIO_Port_Data, GPIO_LDN);
}

void Set_Register(UINT8 offset, UINT8 And_Value, UINT8 OR_value) {
    UINT8 Temp;
    IoWrite8(SIO_Port_Index, offset);
    Temp=(IoRead8(SIO_Port_Data) & And_Value) | OR_Value;
    IoWrite8(SIO_Port_Data, Temp);
}

Byte Get_Register(UINT8 offset, UINT8 And_Value) {
    UINT8 Temp;
    IoWrite8(SIO_Port_Index, offset);
    Temp=IoRead8(SIO_Port_Data) & And_Value;
    return Temp;
}

void main()
{
    UINT8 GPIO0;
    UINT8 GPI1;
    UINT8 GPI2;
    UINT8 GPI3;

    Enter_F81804_SIO();
    Set_GPIO_LDN();

    //GPO Output and setting
    //GPO0 Setting
    Set_Register(0x99, 0xFB, (GPO0_Output<<2));    //Bit2: GPO0 status, 0: Low 1: High

    //GPO1 Setting
```

```
Set_Register(0x99, 0xF7, (GPO1_Output<<3));    //Bit3: GPO1 status, 0: Low 1: High

//GPO2 Setting
Set_Register(0x99, 0xEF, (GPO2_Output<<4));    //Bit4: GPO2 status, 0: Low 1: High

//GPO3 Setting
Set_Register(0x99, 0x7F, (GPO3_Output<<7));    //Bit7: GPO3 status, 0: Low 1: High

//GPI Input and get status
GPI0= IoRead8(GPIO_IOSpace+GPI0_Offset);      //Bit0: GPI0 status, 0: Low 1: High

GPI1= IoRead8(GPIO_IOSpace+GPI1_Offset);      //Bit6: GPI1 status, 0: Low 1: High

GPI2= Get_Register(0x9A,0x02);                 //Bit1: GPI2 status, 0: Low 1: High

GPI3= IoRead8(GPIO_IOSpace+GPI3_Offset);      //Bit0: GPI3 status, 0: Low 1: High
}
```

Chapter 6

System Overview

- 6 BIOS Setup
- 6.1 Entering Setup
- 6.2 Main
- 6.3 Configuration
- 6.4 Security
- 6.5 Boot
- 6.6 Save & Exit

6. BIOS Setup information

PICO-8021 is equipped with the AMI BIOS stored in Flash ROM. The following section describes the BIOS setup program. The BIOS setup program can be used to view and change the BIOS settings for the module. Only experienced users should change the default BIOS settings.

6.1 Entering Setup

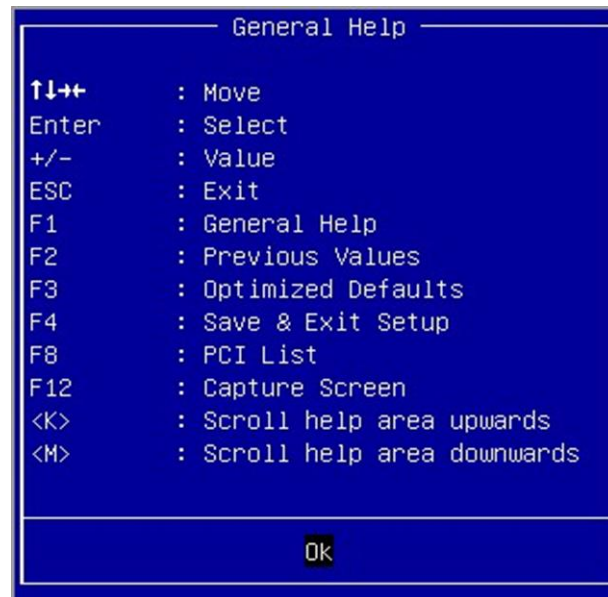
Power on the computer and the system will start POST (Power on Self Test) Process. When the message below appears on the screen, press key will enter BIOS setup screen.

Press to enter SETUP

If the message disappears before responding and still wish to enter Setup, please restart the system by turning it OFF and On or pressing the RESET button. It can be also restarted by pressing <Ctrl>, <Alt>, and <Delete> keys on keyboard simultaneously.

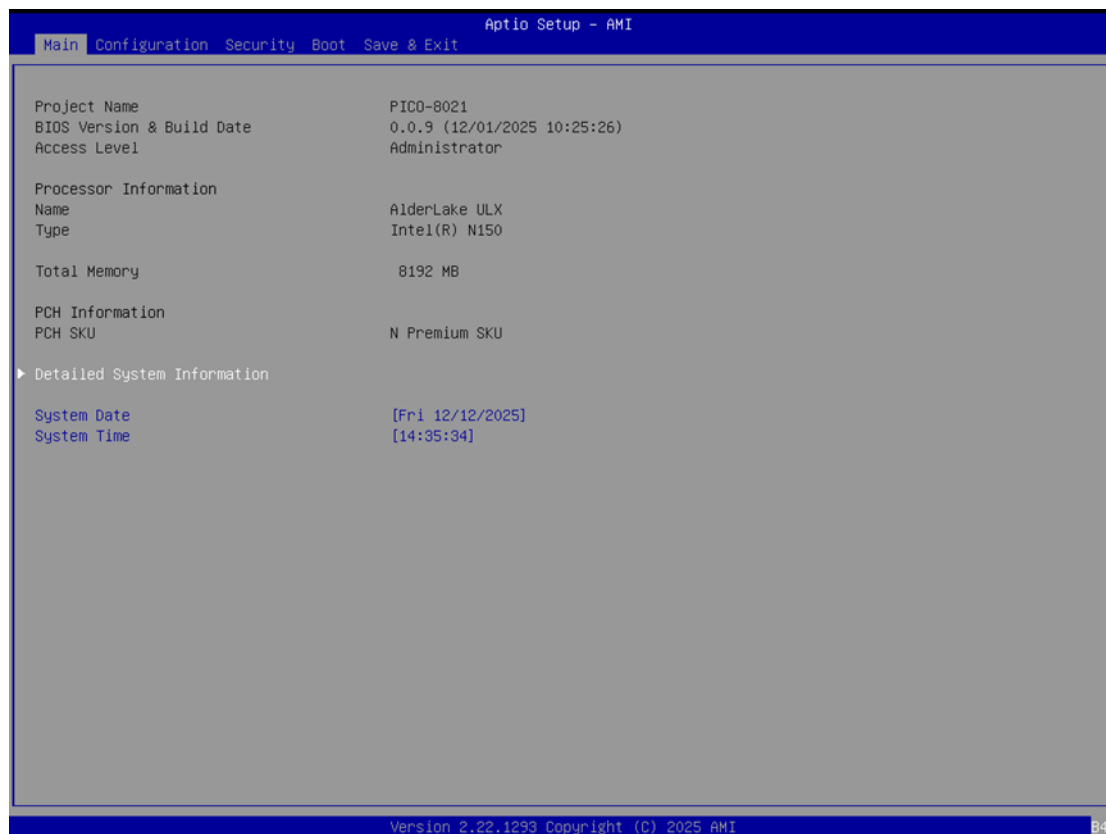
Press <F1> to Run General Help or Resume

The BIOS setup program provides a General Help screen. The menu can be easily called up from any menu by pressing <F1>. The Help screen lists all the possible keys to use and the selections for the highlighted item. Press <Esc> to exit the Help Screen.



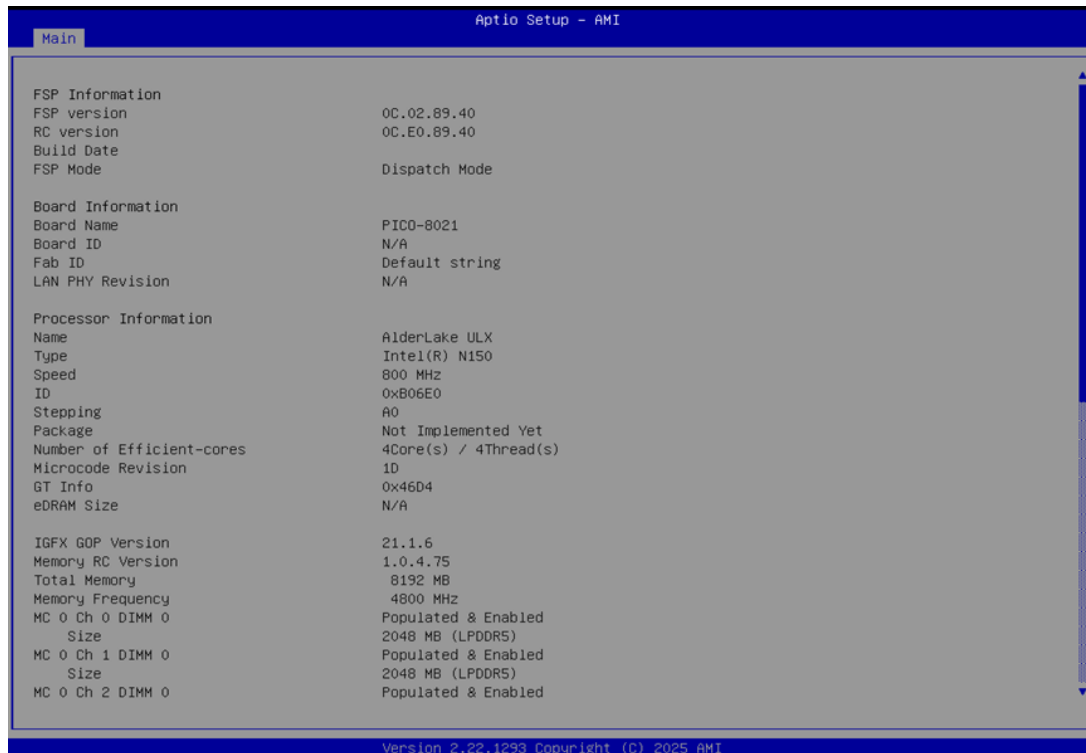
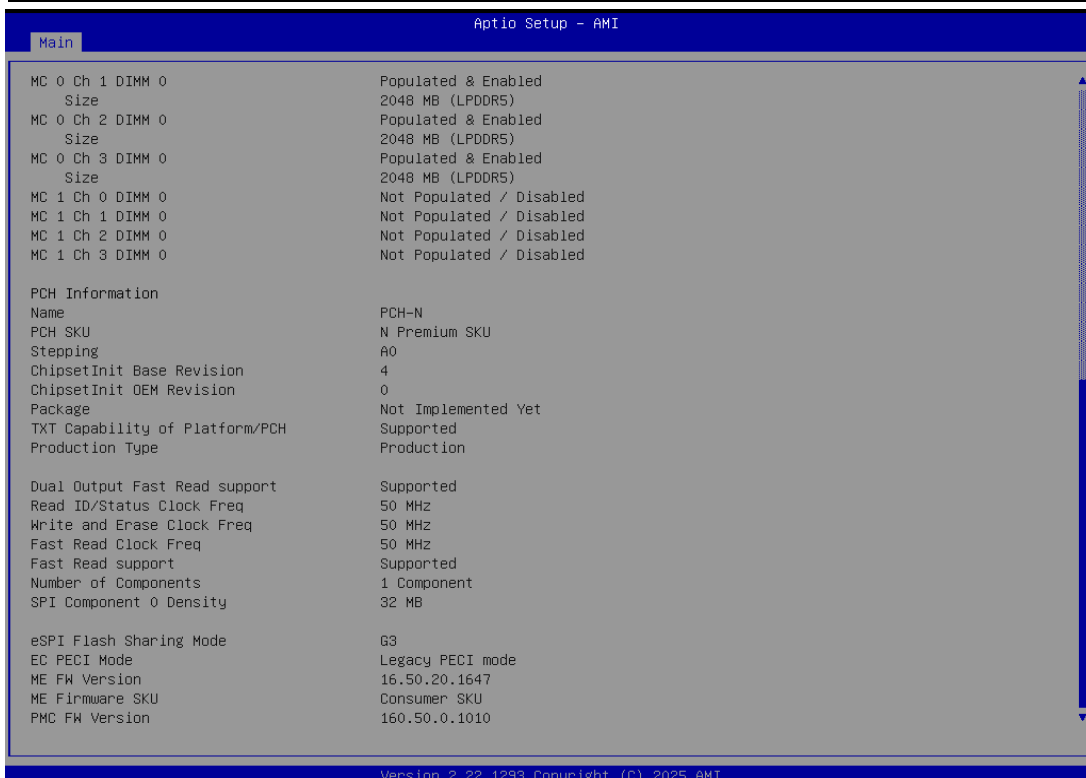
6.2 Main

Use this menu for basic system configurations, such as time, date etc.

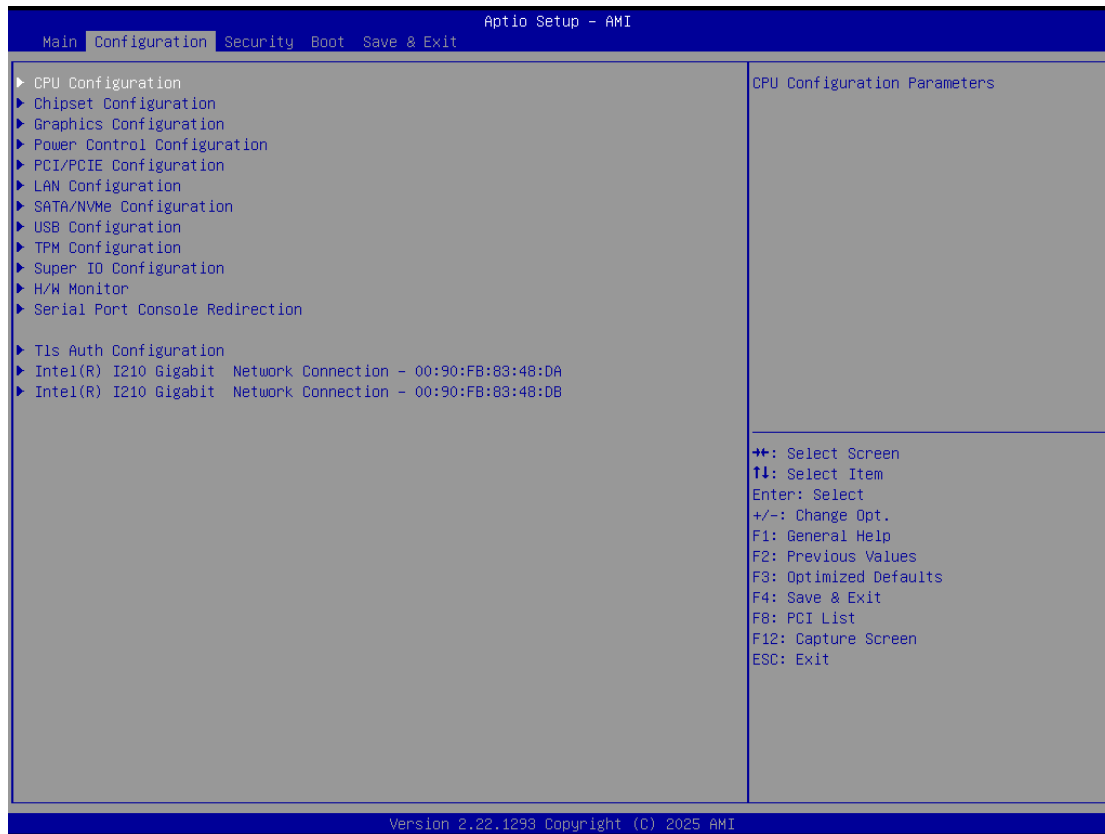


Feature	Description	Options
System Date	The date format is <Day>, <Month><Date><Year>. Use [+] or [-] to configure system Date.	
System Time	The time format is <Hour><Minute><Second>. Use [+] or [-] to configure system Time.	

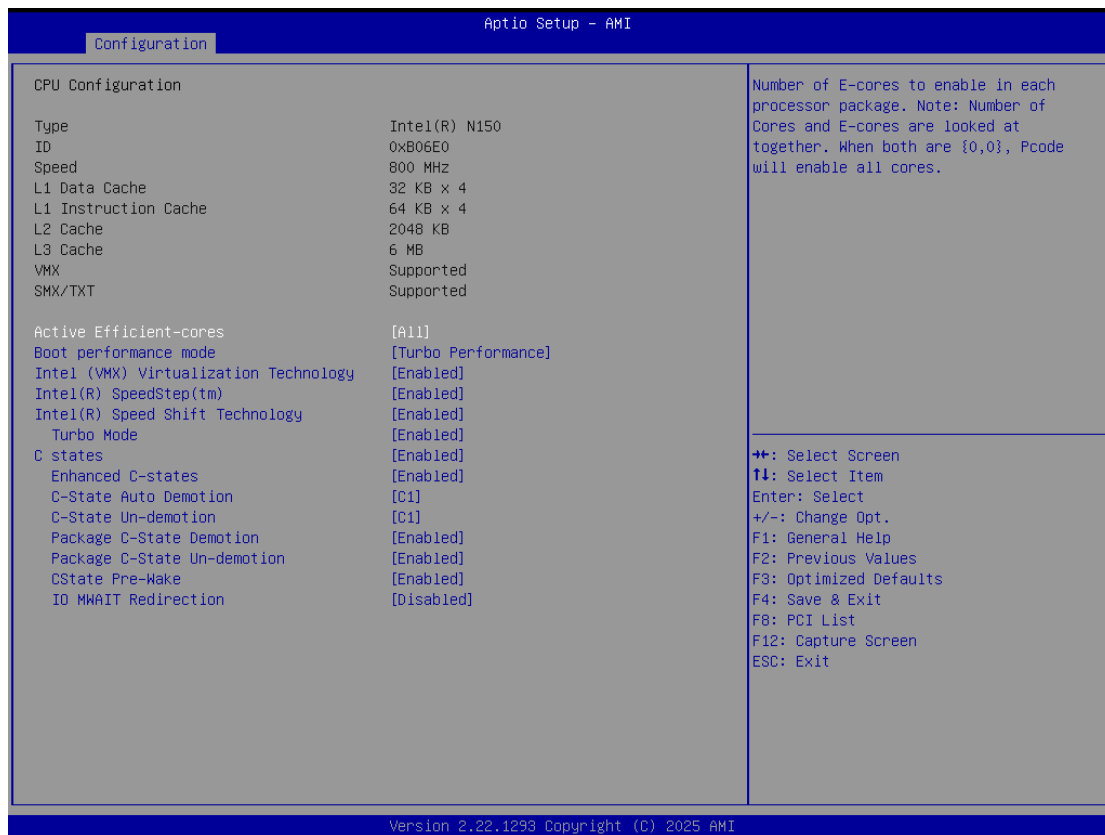
Detailed System Information



6.3 Configuration



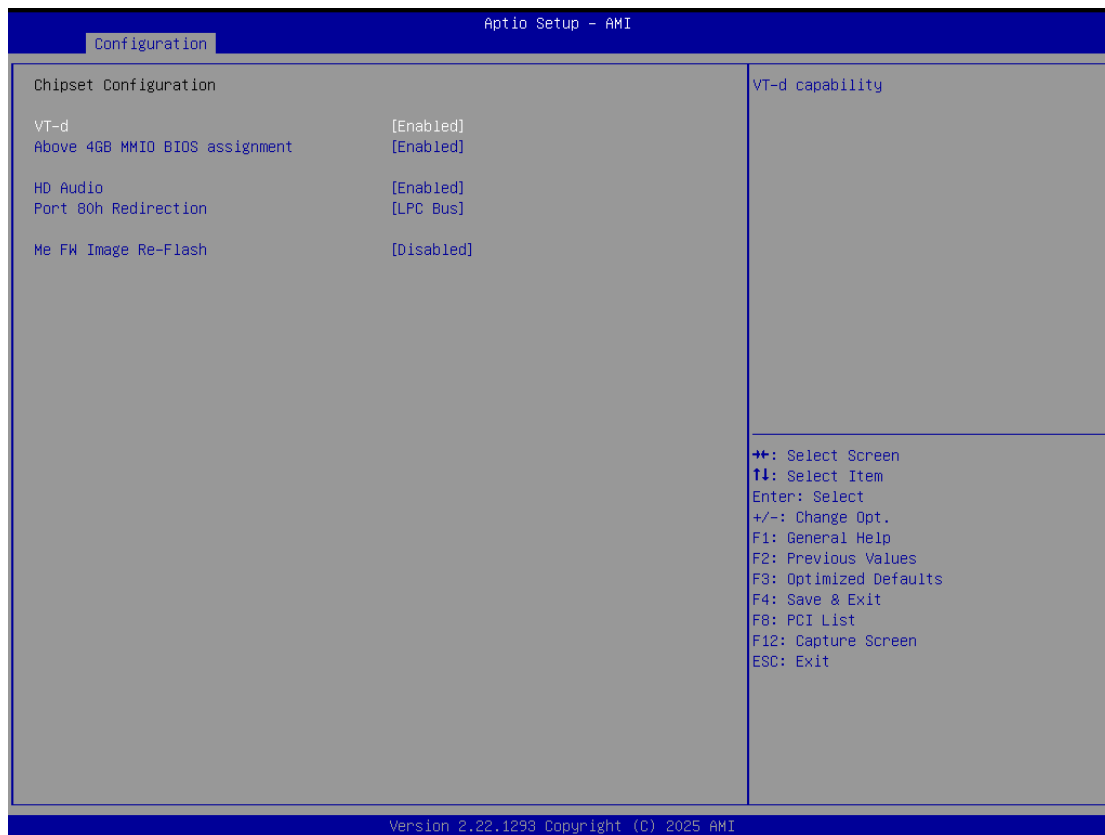
6.3.1 CPU Configuration



Feature	Description	Options
Active Efficient-Cores	Number of E-cores to enable in each processor package. Note: Number of Cores and E-cores are looked at together, When both are {0,0}, Pcode will enable all cores.	★All, 3, 2, 1
Boot performance mode	Select the performance state that the BIOS will set starting from reset vector	★Turbo Performance , Max Non-Turbo Performance, Max Battery,
Intel (VMX) Virtualization Technology	When enabled, a VMM can utilize the additional hardware capabilities provided by Vander pool Technology.	Disabled, ★Enabled
Intel (R) Speed Step (tm)	Allows more than two frequency ranges to be supported.	Disabled, ★Enabled

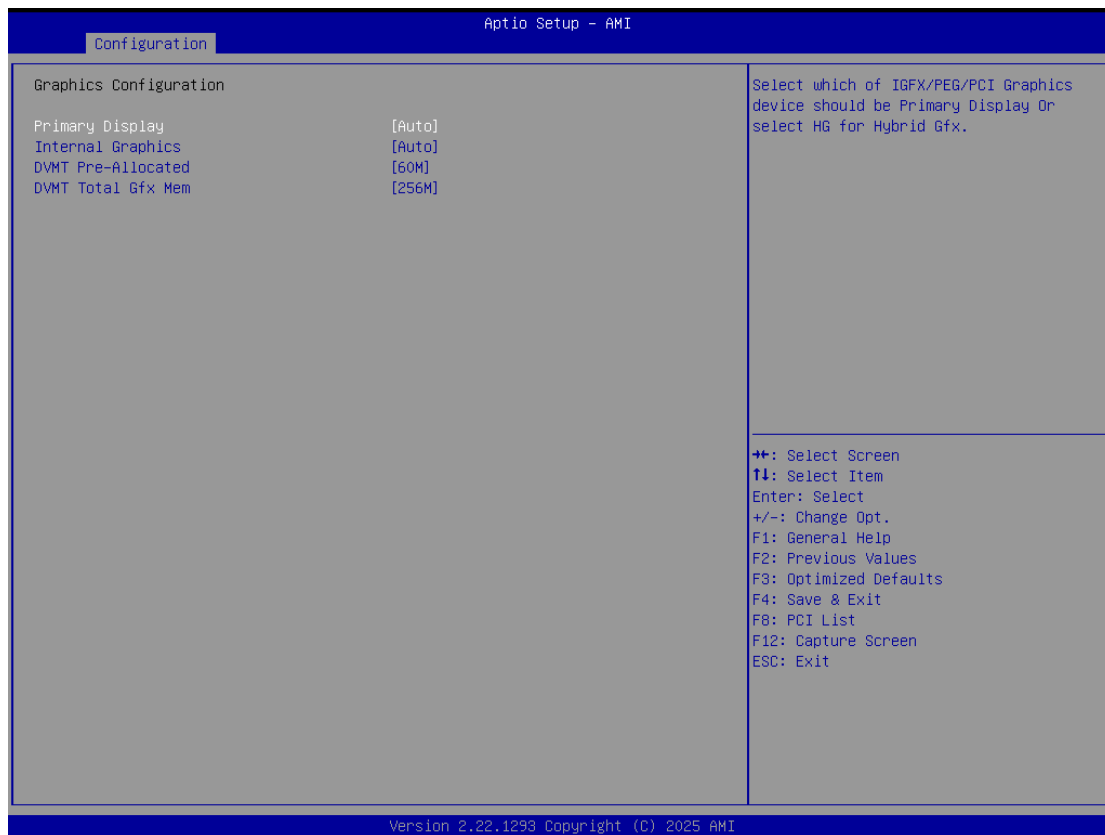
Feature	Description	Options
Intel (R) Speed Shift Technology	Enable/Disable Intel® Speed Shift Technology support. Enabling will expose the CPPC v2 interface to allow for hardware controlled P-states	Disabled, ★Enabled
Turbo Mode	Enable/Disable processor Turbo Mode (requires EMTM enabled too). AUTO means enabled.	Disabled, ★Enabled
C states	Enable/disable CPU Power Management. Allows CPU to go to C states when it's not 100% utilized	Disabled, ★Enabled
Enhanced C-states	Enable/Disable C1E. When enabled, CPU will switch to minimum speed when all cores enter C-state	Disabled, ★Enabled
C-State Auto Demotion	Configure C-State Auto Demotion	Disabled, ★C1
C-State Un-demotion	Configure C-State Un-demotion	Disabled, ★C1
Package C State Demotion	Package C-State Demotion	Disabled, ★Enabled
Package C State Un-demotion	Package C-State Un-demotion	Disabled, ★Enabled
CState Pre-Wake	Disable – Sets bit 30 of POWER_CTL MSR(0x1FC) to 1 to disable the Cstate Pre-Wake	Disabled, ★Enabled
IO MWAIT Redirection	When set, will map IO_read instructions sent to IO registers PMG_IO_BASE_ADDRBASE+offset to MWAIT(offset)	★Disabled, Enabled

6.3.2 Chipset Configuration



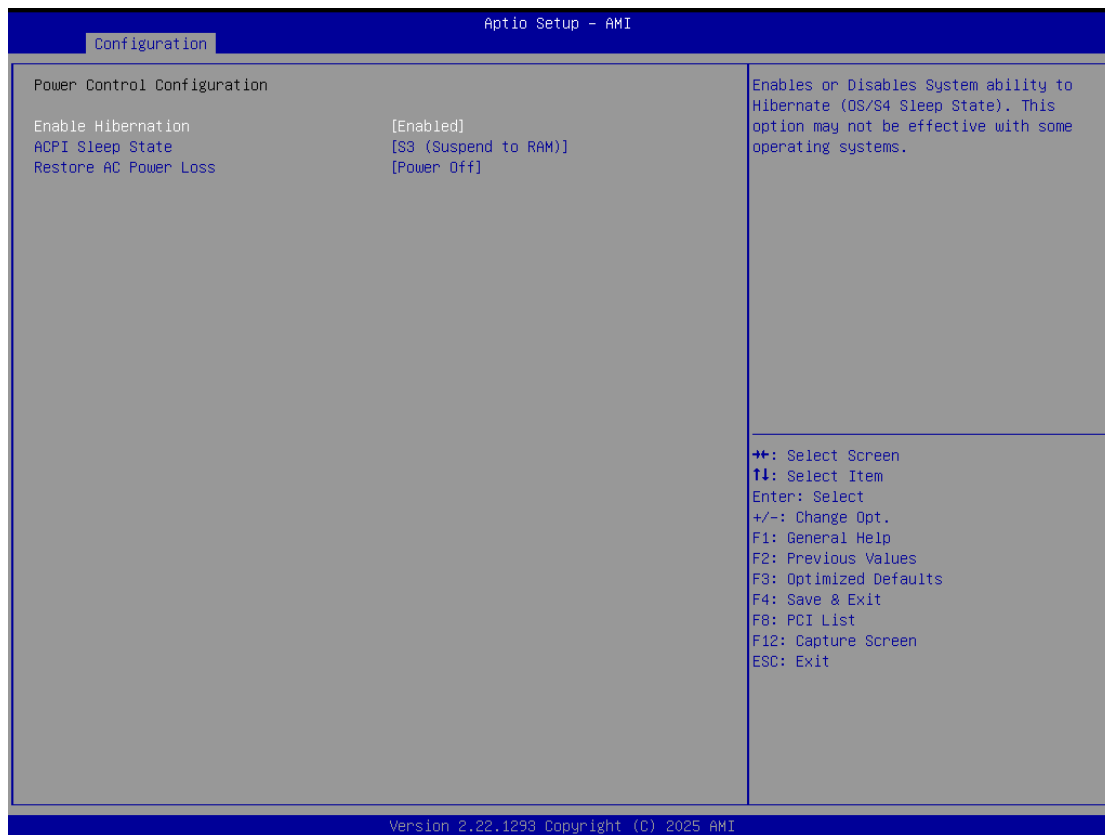
Feature	Description	Options
VT-d	VT-d Capability.	Disabled, ★Enabled
Above 4GB MMIO BIOS assignment	Enable/Disable above 4GB Memory Mapped IO BIOS assignment, This is enabled automatically when Aperture Size is set to 2048MB.	Disabled, ★Enabled
HD Audio	Control Detection of the HD-Audio device. Disabled = HDA will be unconditionally disabled. Enabled = HDA will be unconditionally enabled.	Disabled, ★Enabled
Port 80h Redirection	Control when the Port 80h cycles are sent.	★LPC Bus, PCIE Bus
Me FW Image Re-Flash	Enable/Disable Me FW Image Re-Flash function.	★Disabled, Enabled

6.3.3 Graphics Configuration



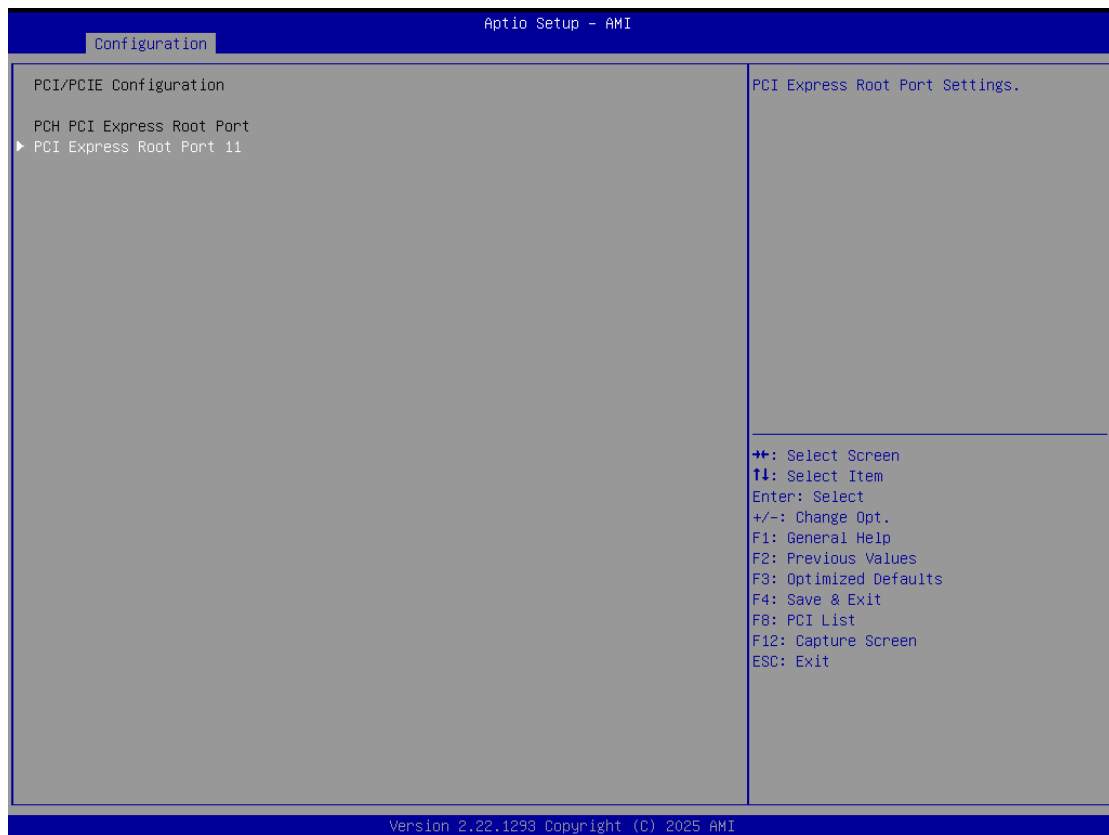
Feature	Description	Options
Primary Display	Select which of IGFX/PEG/PCI Graphics device should be Primary Display Or Select HG for Hybrid Gfx.	★Auto, IGFX, PEG Slot, PCH PCI
Internal Graphics	Keep IGFX enable based on the setup options.	★Auto, Disabled, Enabled
DVMT Pre-Allocated	Select DVMT 5.0 Pre-Allocated (Fixed) Graphics Memory size used by the Internal Graphics Device.	32M,64M, 96M, 128M, 160M, 12M, 16M,20M, 24M, 28M, 32M/F7,36M,40M,44M,48M, 52M,56M, ★60M
DVMT Total Gfx Mem	Select DVMT5.0 Total Graphic Memory size used by the Internal Graphics Device	★256M, 128M, MAX

6.3.4 Power Control Configuration



Feature	Description	Options
Enable Hibernation	Enables or Disables System ability to Hibernates (OS/S4 Sleep State). This option may not be effective with some operating systems.	Disabled, ★Enabled
ACPI Sleep State	Select the highest ACPI sleep state the system will enter when the SUSPEND button is pressed.	★S3 (Suspend to RAM), Suspend Disabled
Restore AC Power Loss	Specify what state to go to when power is re-applied after a power failure (G3 state)	★Power Off, Power On, Last State

6.3.5 PCI/PCIE Configuration



PCI Express Root Port 11

Configuration

Aptio Setup - AMI

PCI Express Root Port 11	[Enabled]	Control the PCI Express Root Port.
ASPM	[Disabled]	
PCIe Speed	[Auto]	

⇐: Select Screen
 ↑↓: Select Item
 Enter: Select
 +/-: Change Opt.
 F1: General Help
 F2: Previous Values
 F3: Optimized Defaults
 F4: Save & Exit
 F8: PCI List
 F12: Capture Screen
 ESC: Exit

Version 2.22.1293 Copyright (C) 2025 AMI

Feature	Description	Options
PCI Express Root Port 11	Control the PCI Express Root Port.	Disabled, ★Enabled
ASPM	Set the ASPM Level: Force L0s – Force all links to L0s State AUTO-BIOS auto configure DISABLE – Disables ASPM	★Disabled, L1, Auto
PCIe Speed	Configure PCIe Speed	★Auto, Gen1, Gen2, Gen3

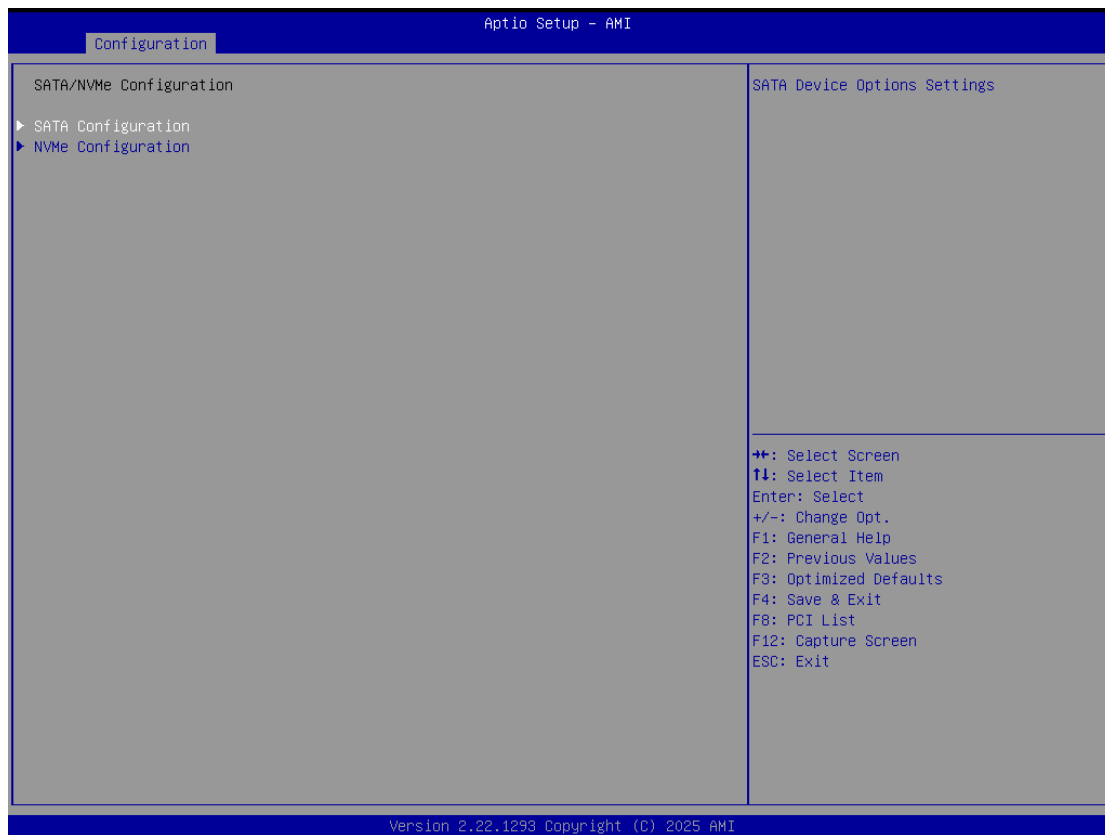
6.3.6 LAN Configuration



Feature	Description	Options
OnBoard LAN Controller #1	Enable or Disable LAN Controller.	Disabled, ★Enabled
PCI Express Root Port 9	Control the PCI Express Root Port.	Disabled, ★Enabled
OnBoard LAN Controller #2	Enable or Disable LAN Controller.	Disabled, ★Enabled
PCI Express Root Port 10	Control the PCI Express Root Port.	Disabled, ★Enabled
PCIE_WAKE (Wake On Lan)	Control the PCIE Wake# pin for Wake On Lan function.	Disabled, ★Enabled
Launch UEFI PXE ROM	Enable/Disable UEFI Network Stack	★Disabled, Enabled

Feature	Description	Options
Launch UEFI PXE ROM (Enabled)		
IPv4 PXE Support	Enable/Disable IPv4 PXE boot support. If disabled, IPv4 PXE boot support will not be available.	Disabled, ★Enabled
IPv4 HTTP Support	Enable/Disable IPv4 HTTP boot support. If disabled, IPv4 HTTP boot support will not be available.	Disabled, ★Enabled
IPv6 PXE Support	Enable/Disable IPv6 PXE boot support. If disabled, IPv6 PXE boot support will not be available.	Disabled, ★Enabled
IPv6 HTTP Support	Enable/Disable IPv6 HTTP boot support. If disabled, IPv6 HTTP boot support will not be available.	Disabled, ★Enabled
PXE boot wait time	Wait time in seconds to press ESC key to abort the PXE boot. Use either +/- or numeric keys to set the value.	★0
Media detect count	Number of times the presence of media will be checked. Use either +/- or numeric keys to set the value.	★1

6.3.7 SATA / NVMe Configuration



SATA Configuration

Configuration Aptio Setup - AMI

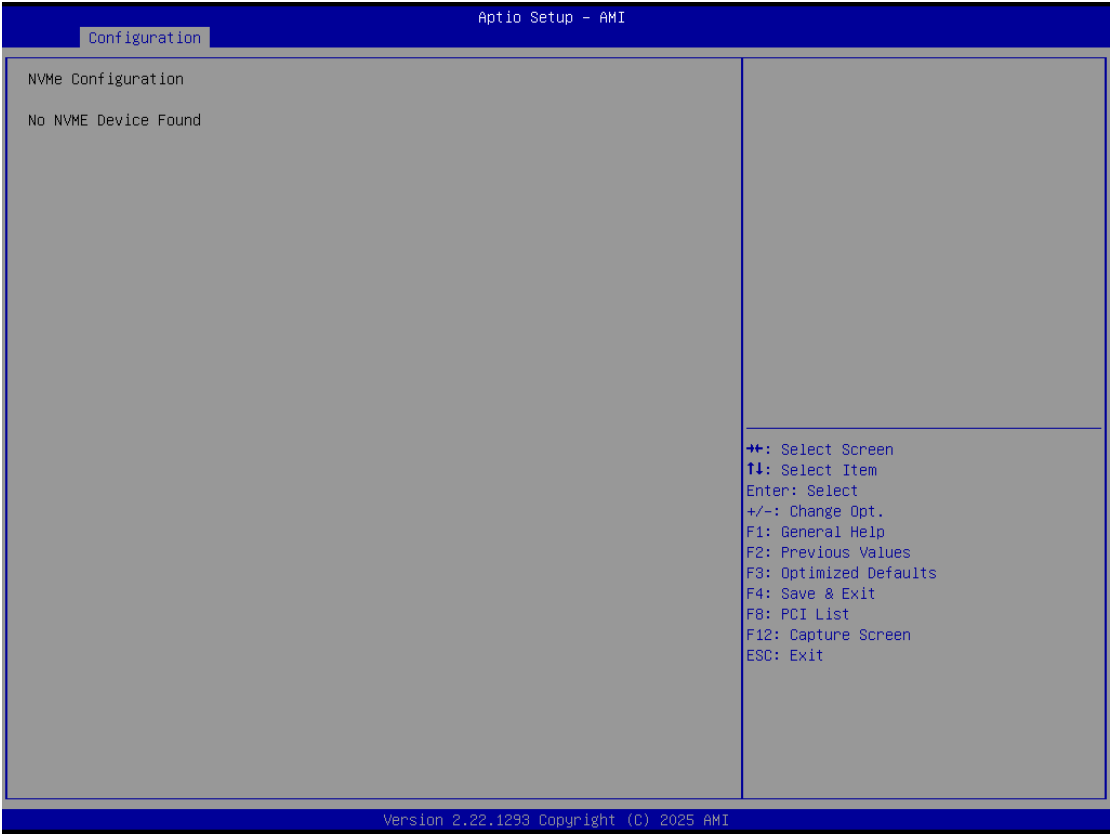
SATA Configuration		Enable/Disable SATA Device.
SATA Controller(s)	[Enabled]	
Serial ATA Port 0	Empty	
Software Preserve	Unknown	
Port 0	[Enabled]	
Hot Plug	[Disabled]	
Configured as eSATA	Hot Plug supported	
SATA Device Type	[Hard Disk Drive]	

⇐: Select Screen
 ↑↓: Select Item
 Enter: Select
 +/-: Change Opt.
 F1: General Help
 F2: Previous Values
 F3: Optimized Defaults
 F4: Save & Exit
 F8: PCI List
 F12: Capture Screen
 ESC: Exit

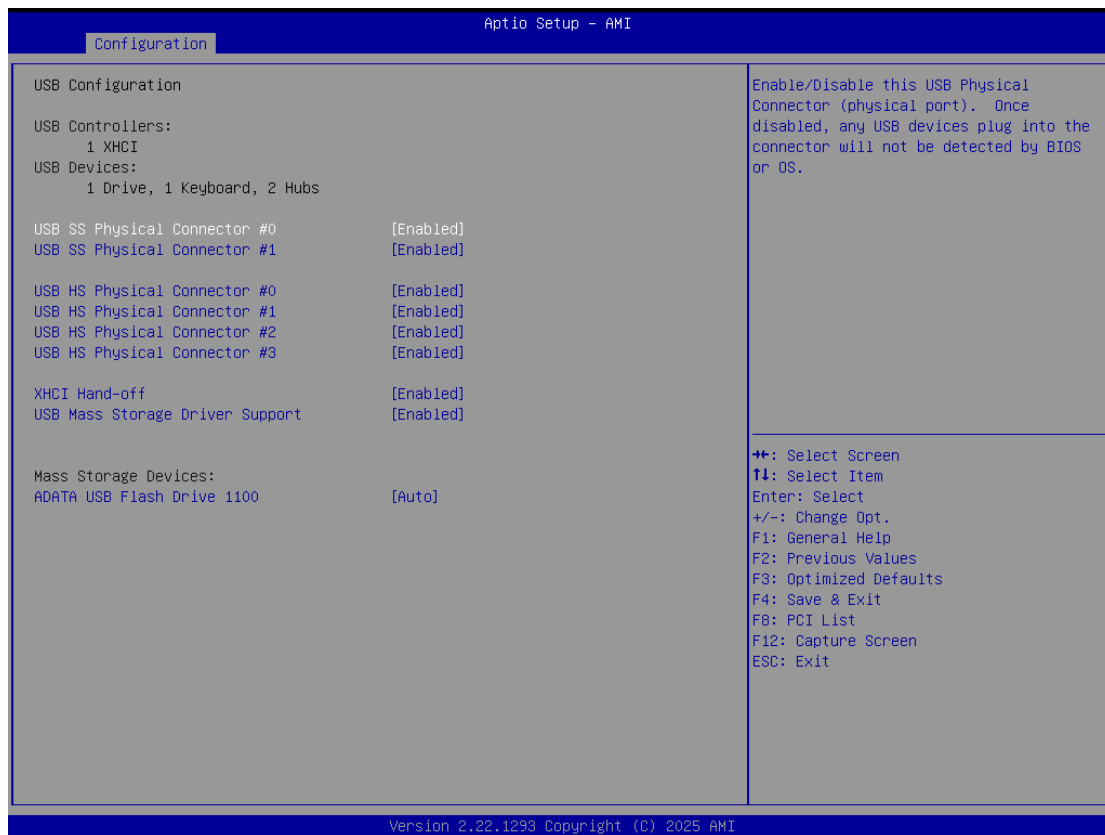
Version 2.22.1293 Copyright (C) 2025 AMI

Feature	Description	Options
SATA Controller(s)	Enable/Disable SATA Device	Disabled, ★Enabled
Serial ATA Port 0		
Port 0	Enabled or Disabled SATA Port	Disabled, ★Enabled
Hot plug	Designates this port as Hot pluggable.	★Disabled, Enabled
SATA Device Type	Identify the SATA port is connected to Solid State Drive or Hard Disk Drive.	★Hard Disk Drive, Solid State Drive

NVMe Configuration



6.3.8 USB Configuration



Feature	Description	Options
USB SS Physical Connector #0	Enabled/Disabled this USB Physical connector (physical port). Once disabled, any USB devices plug into the connector will not be detected by BIOS or OS.	Disabled, ★Enabled
USB SS Physical Connector #1	Enabled/Disabled this USB Physical connector (physical port). Once disabled, any USB devices plug into the connector will not be detected by BIOS or OS.	Disabled, ★Enabled
USB HS Physical Connector #0	Enabled/Disabled this USB Physical connector (physical port). Once disabled, any USB devices plug into the connector will not be detected by BIOS or OS.	Disabled, ★Enabled

Feature	Description	Options
USB HS Physical Connector #1	Enabled/Disabled this USB Physical connector (physical port). Once disabled, any USB devices plug into the connector will not be detected by BIOS or OS.	Disabled, ★Enabled
USB HS Physical Connector #2	Enabled/Disabled this USB Physical connector (physical port). Once disabled, any USB devices plug into the connector will not be detected by BIOS or OS.	Disabled, ★Enabled
USB HS Physical Connector #3	Enabled/Disabled this USB Physical connector (physical port). Once disabled, any USB devices plug into the connector will not be detected by BIOS or OS.	Disabled, ★Enabled
XHCI Hand-off	This is a workaround for OSes without XHCI hand-off support. The XHCI ownership change should be claimed by XHCI driver	Disabled, ★Enabled
USB Mass Storage Driver Support	Enable/Disable USB Mass Storage Driver Support	Disabled, ★Enabled
Mass storage Devices:		
ADATA USB Flash Drive 1100	Mass storage device emulation type. 'AUTO' enumerates devices according to their media format. Optical drives are emulated as 'CDROM'; drives with no media will be emulated according to a drive type.	★Auto, Floppy, Forced FDD, Hard Disk, CD-ROM

6.3.9 TPM Configuration



Feature	Description	Options
Security Device Support	Enables or Disables BIOS support for security device. O.S. will not show Security Device. TCG EFI protocol and INT1A Interface will not be available.	Disabled, ★Enabled
SHA256 PCR Bank	Enables or Disables SHA256 PCR Bank.	Disabled, ★Enabled
SHA384 PCR Bank	Enables or Disables SHA384 PCR Bank.	★Disabled, Enabled
Pending operation	Schedule an Operation for the Security Device. Note: Your Computer will reboot during restart in order to change State of Security Device.	★None, TPM Clear
Platform Hierarchy	Enables or Disables Platform Hierarchy.	Disabled, ★Enabled

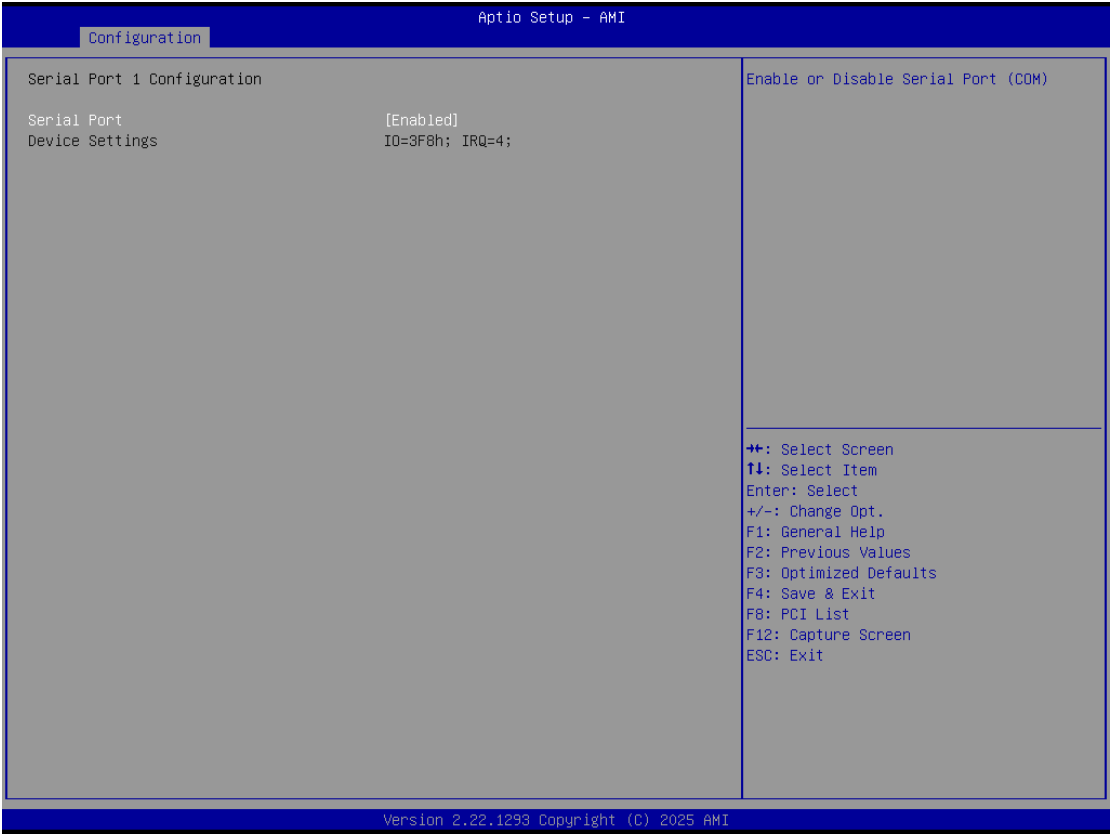
Feature	Description	Options
Storage Hierarchy	Enables or Disables Storage Hierarchy.	Disabled, ★Enabled
Endorsement Hierarchy	Enables or Disables Endorsement Hierarchy.	Disabled, ★Enabled
TPM2.0 UEFI Spec Version	Select the TCG2 Spec Version Support. CG_1_2: the Compatible mode for Win8/Win10. TCG_2: Support new TCG2 protocol and event format for Win10 or later.	TCG_1_2, ★TCG_2
Physical Presence Spec Version	Select to Tell O.S. to Support PPI Spec Version 1.2 or 1.3. Note some HCK tests might not support 1.3.	1.2, ★1.3
Device Select	TPM 1.2 will restrict support to TPM 1.2 devices, TPM 2.0 will restrict support to TPM 2.0 devices, Auto will support both with the default set to TPM 2.0 devices if not found, TPM 1.2 devices will be enumerated.	★Auto, TPM 1.2, TPM 2.0

6.3.10 Super IO Configuration



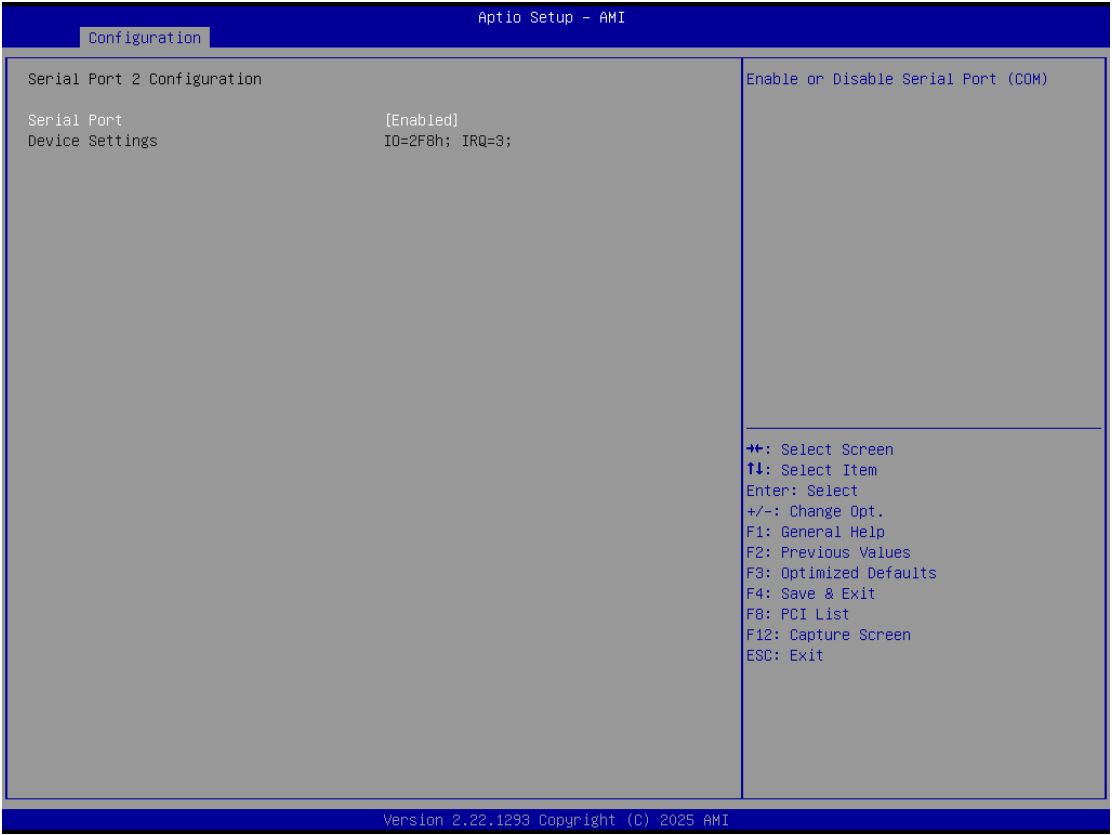
Feature	Description	Options
Serial Port 1 Configuration		
Serial Port 2 Configuration		
Watch Dog Timer	Enable/Disable Watch Dog Timer	★ Disabled, Enabled
Watch Dog Timer [Enabled]		
Timer Unit	Select Timer count unit of WDT	★ Second, Minute
Timer value	Set WDT Timer value seconds / minutes	★ 60

Serial Port 1 Configuration



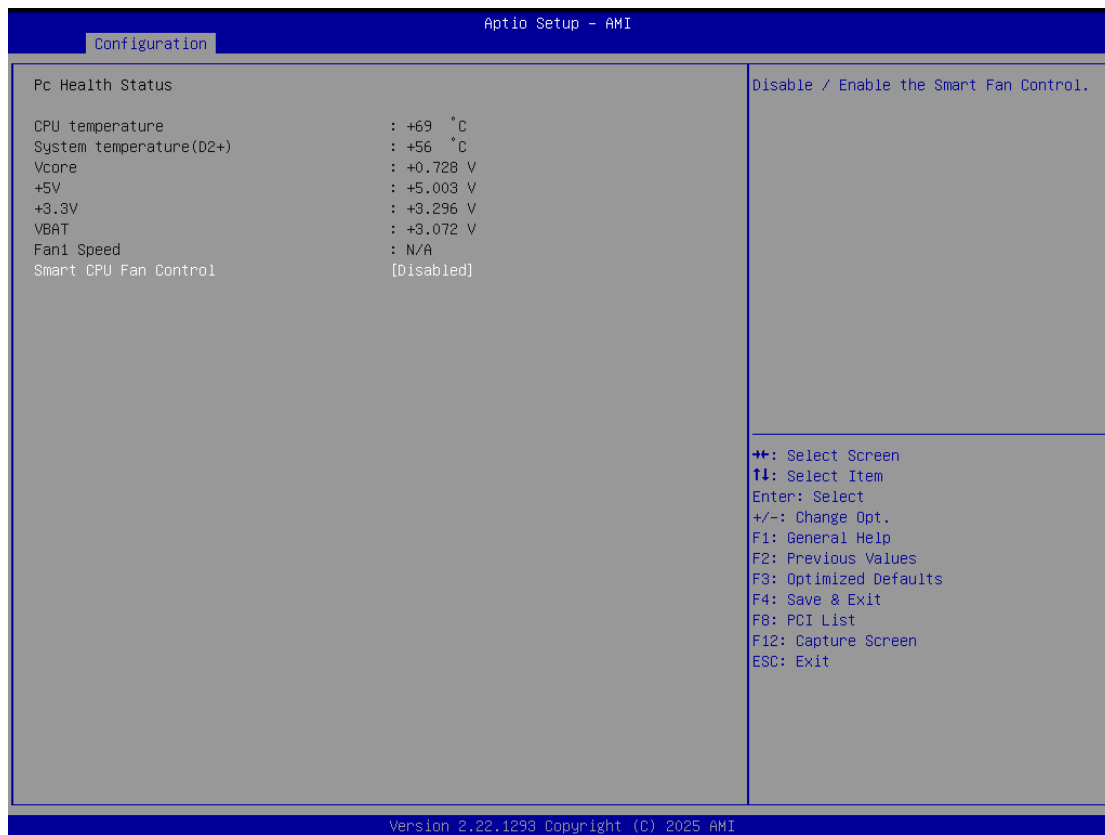
Feature	Description	Options
Serial Port	Enable or Disable Serial Port (COM)	Disabled, ★Enabled

Serial Port 2 Configuration



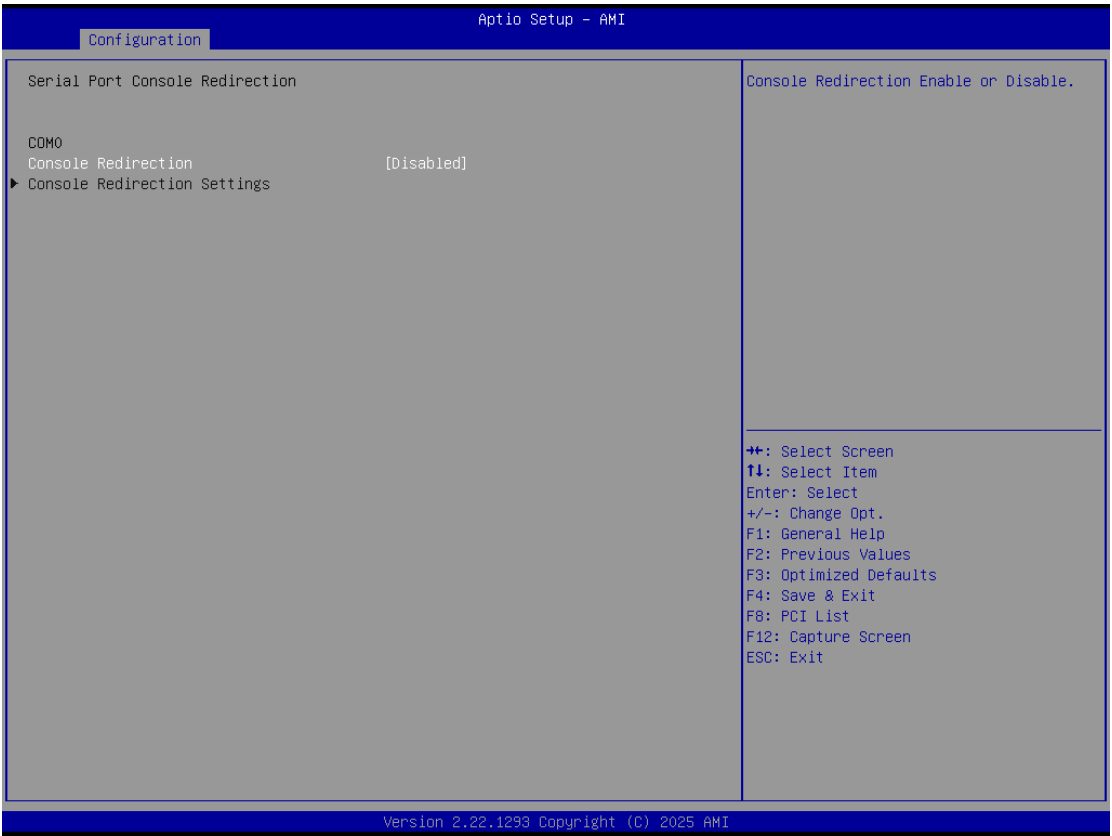
Feature	Description	Options
Serial Port	Enable or Disable Serial Port (COM)	Disabled, ★Enabled

6.3.11 HW Monitor



Feature	Description	Options
Smart CPU Fan Control	Disable / Enable the Smart Fan Control.	★ Disabled, Enabled
Smart CPU Fan Control [Enabled]		
Smart Fan Start Target Temp	Set Fan Start Target Temperature range from 20 to 80 degree.	★ 20
Smart Fan Full Target	Set Fan Full Target Temperature range from 20 to 80 degree.	★ 80
Smart Fan Low and RPM	Smart Fan Low and RPM Percentage.	★ 50

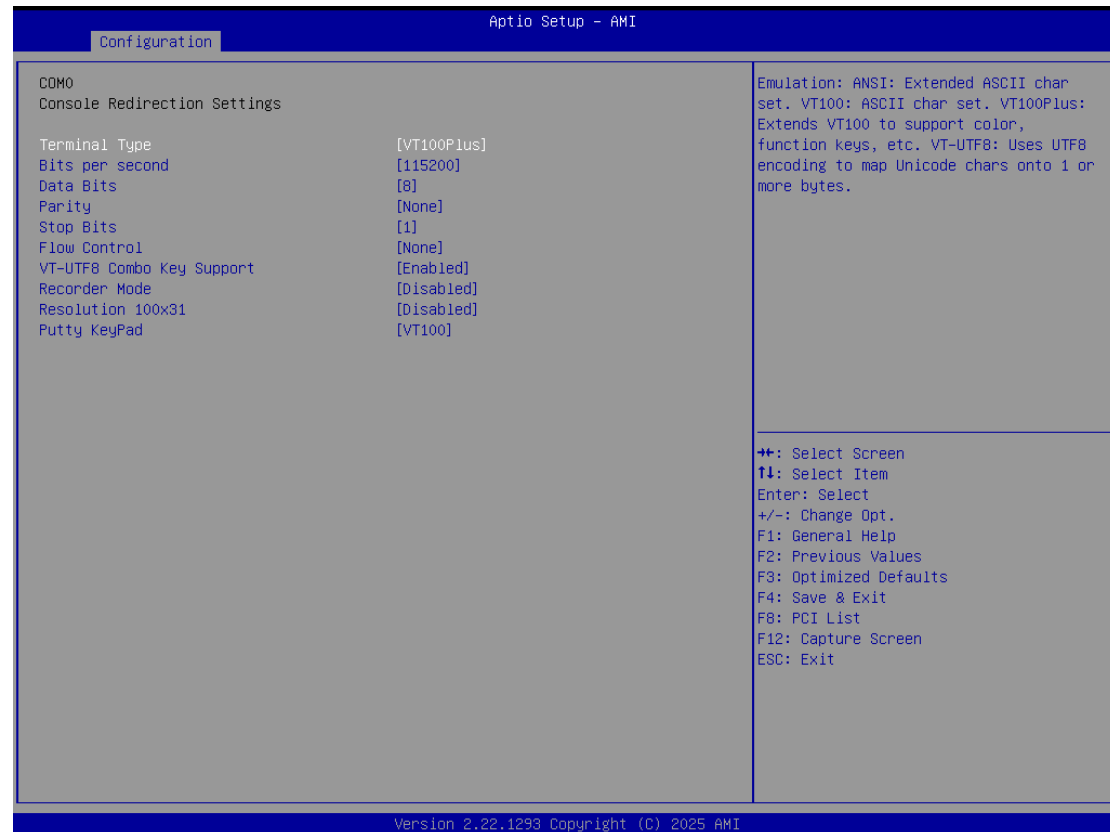
6.3.12 Serial Port Console Redirection



Feature	Description	Options
Console Redirection	Console Redirection Enable or Disable	★Disabled, Enabled

COM0 Console Redirection Settings:

The settings specify how the host computer and the remote computer (which the user is using) will exchange data. Both computers should have the same or compatible settings.



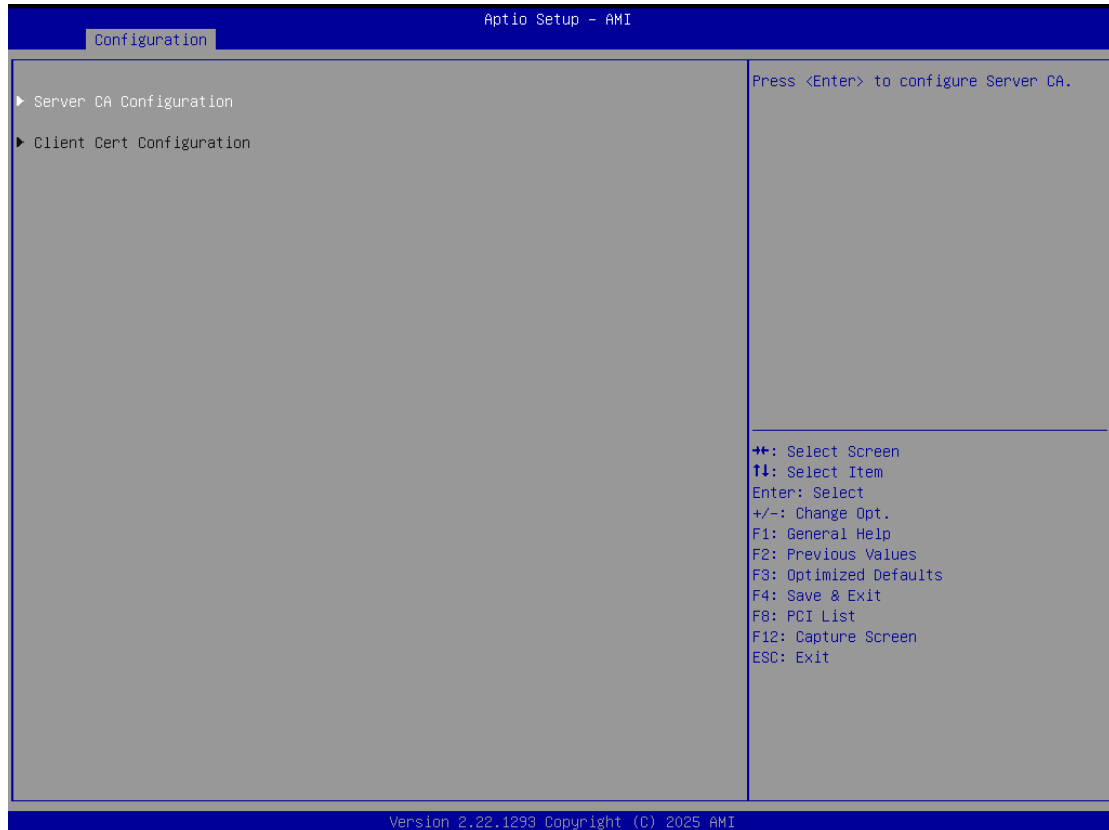
Feature	Description	Options
Terminal Type	Emulation: ANSI: Extended ASCII char set. VT100: ASCII char set. VT100Plus: Extends VT100 to support color, function keys, etc. VT-UTF8: Uses UTF8 encoding to map Unicode chars onto 1 or more bytes.	★VT100Plus, ANSI, VT100, VT-UTF8
Bits per second	Select Serial port transmission speed. The speed must be matched on other side. Long or noisy lines may require lower speeds.	★115200, 9600, 19200, 38400, 57600
Data bits	Data bits	★8, 7
Parity	A parity bit can be sent with the data bits to detect some transmission errors. Even: parity bit is 0 if the num of 1's in the data bits is even. Odd: parity bit is 0 if num of 1's in the data bits is odd. Mark: parity bit is always 1. Space parity bit is always 0. Mark and Space Parity do not allow for error detection. They can be used as an additional data bit.	★None, Even, Odd, Mark, Space

Feature	Description	Options
Stop Bits	Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may require more than 1 stop bit.	★1,2
Flow Control	Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signal.	★None, Hardware RTS/CTS
VT-UTF8 Combo Key Support	Enable VT-UTF8 Combination Key Support for ANSI/VT100 terminals	Disabled, ★Enabled
Recorder Mode	With this mode enabled only text will be sent. This is to capture Terminal data.	★Disabled, Enabled
Resolution 100x31	Enables or disables extended terminal resolution	★Disabled, Enabled
Putty KeyPad	Select FunctionKey and KeyPad on Putty	★VT100, LINUX, XTERMR6, SCO, ESCN, VT400

6.3.13 Tls Auth Configuration

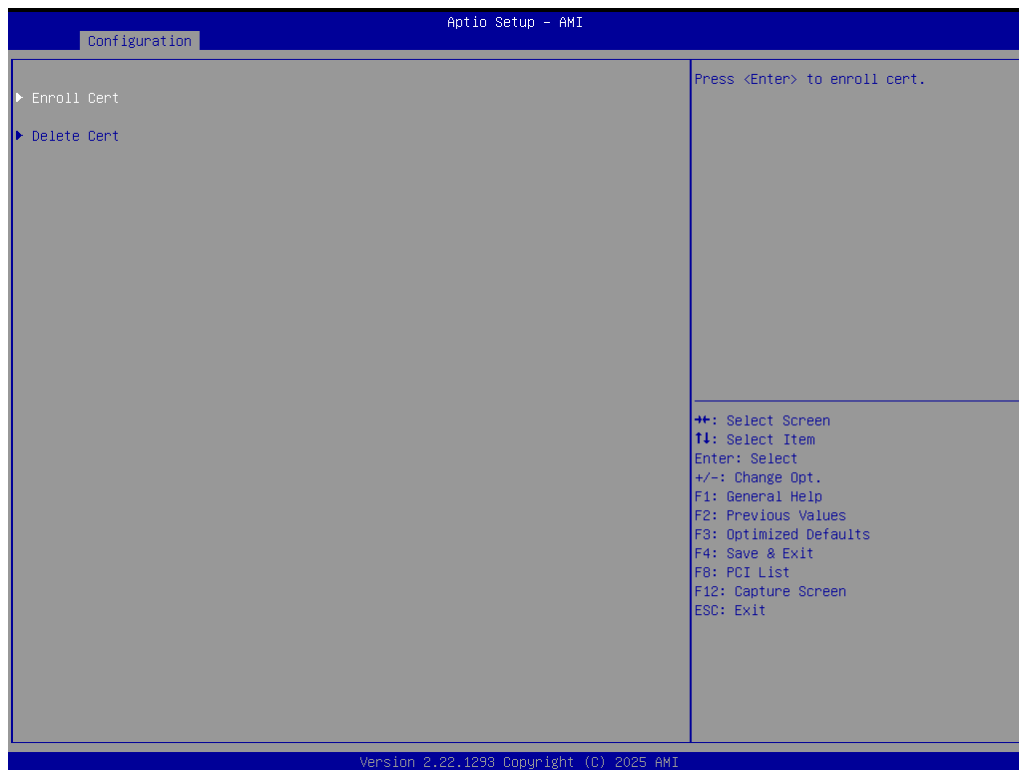
Server CA Configuration

Press <Enter> to configure Server CA.



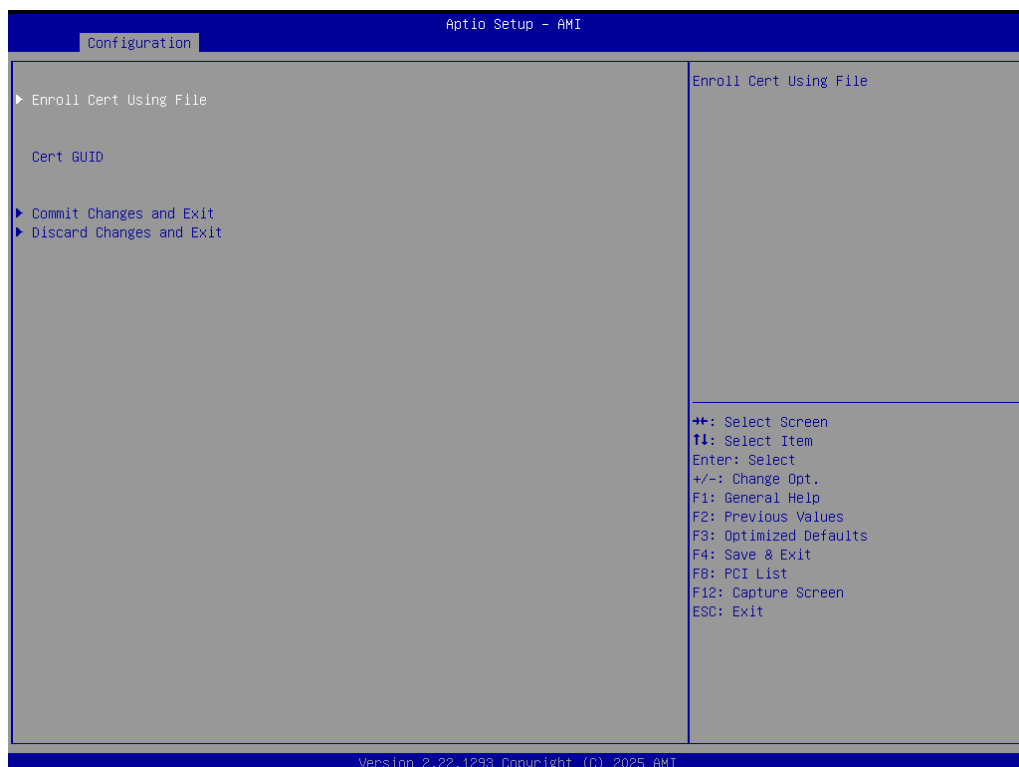
Enroll Cert

Press <Enter> to enroll cert



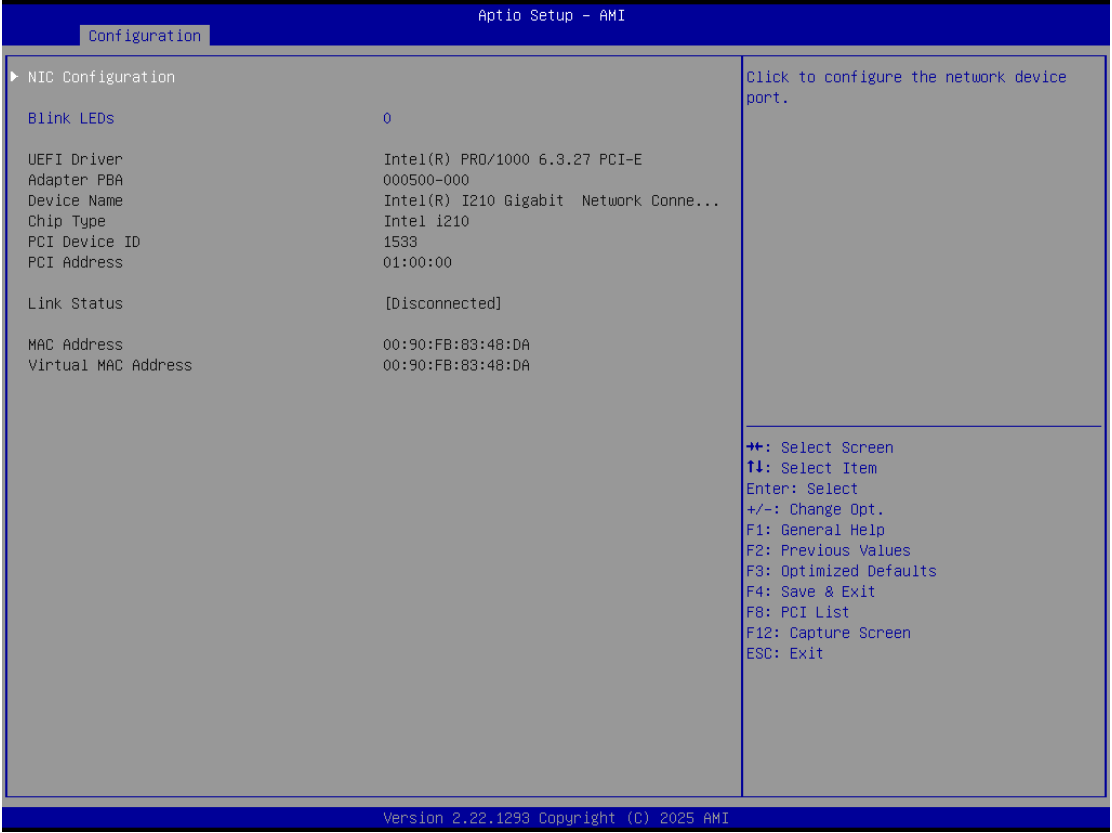
Enroll Cert Using File

Enroll Cert Using File.



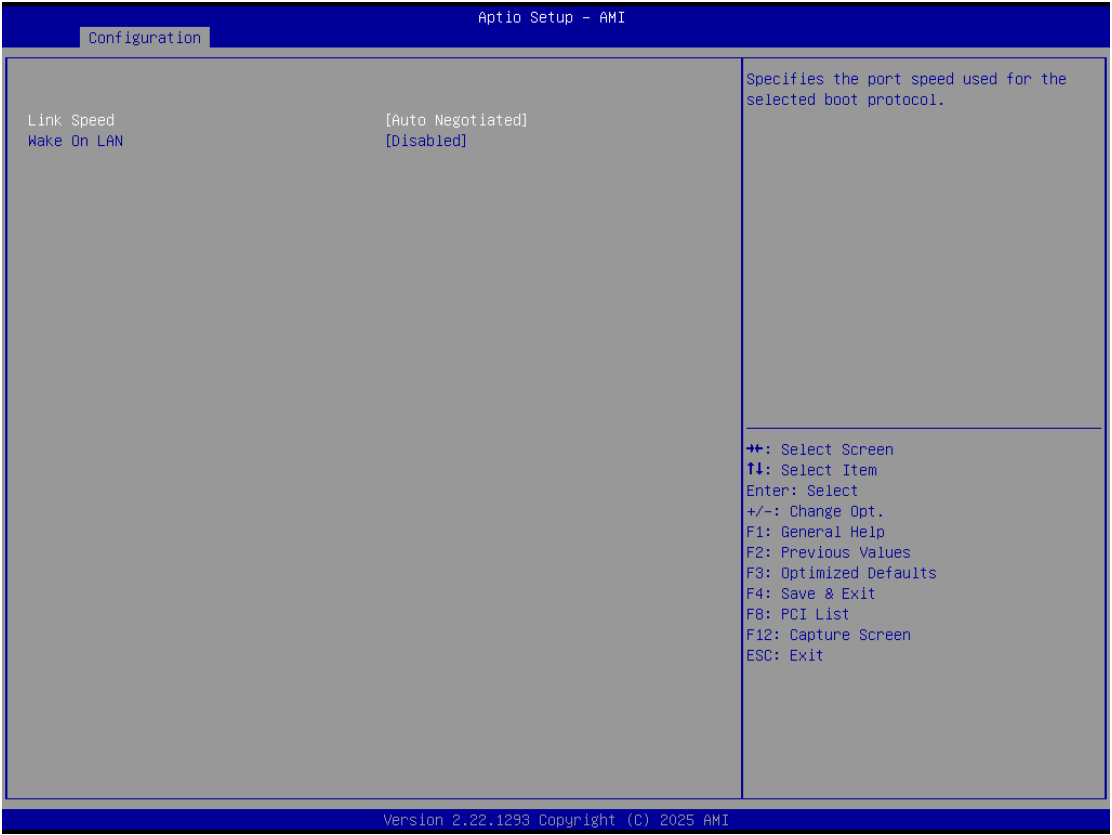
Feature	Description	Options
Enroll Cert Using File	Enroll Cert Using File.	
Cert GUID	Input digit character in 11111111-2222-3333-4444-1234567890ab format.	
Commit Changes and Exit	Commit Changes and Exit	
Discard Changes and Exit	Discard Changes and Exit	

6.3.14 Intel (R) I210 Gigabit Network Connection – 00:90:FB:83:48:DA



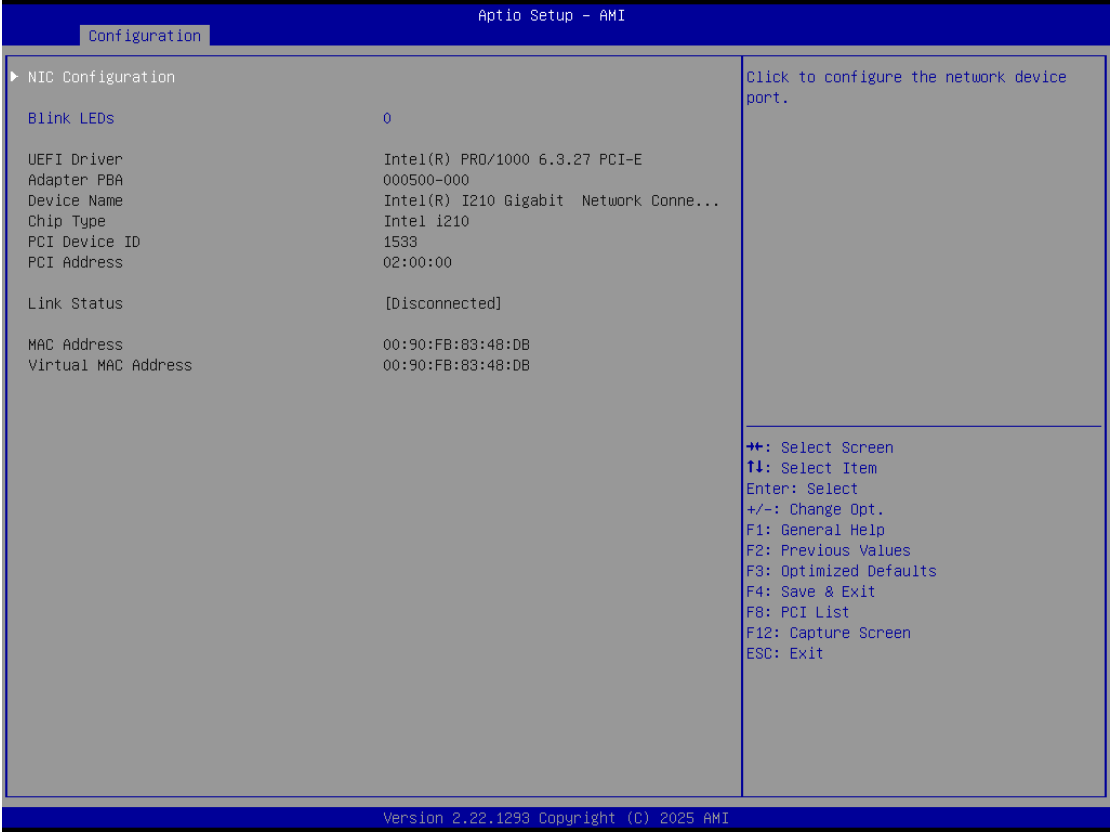
Feature	Description	Options
Blink LEDs	Identify the physical network port by blinking the associated LED.	★0

NIC Configuration



Feature	Description	Options
Link Speed	.Specifies the port speed used for the selected boot protocol.	★Auto Negotiated, 10 Mbps Half, 10 Mbps Full, 100 Mbps Half, 100 Mbps Full
Wake On Lan	Enables the server to be powered on using an in-band magic packet.	★Disabled, Enabled

6.3.15 Intel (R) I210 Gigabit Network Connection – 00:90:FB:83:48:DB



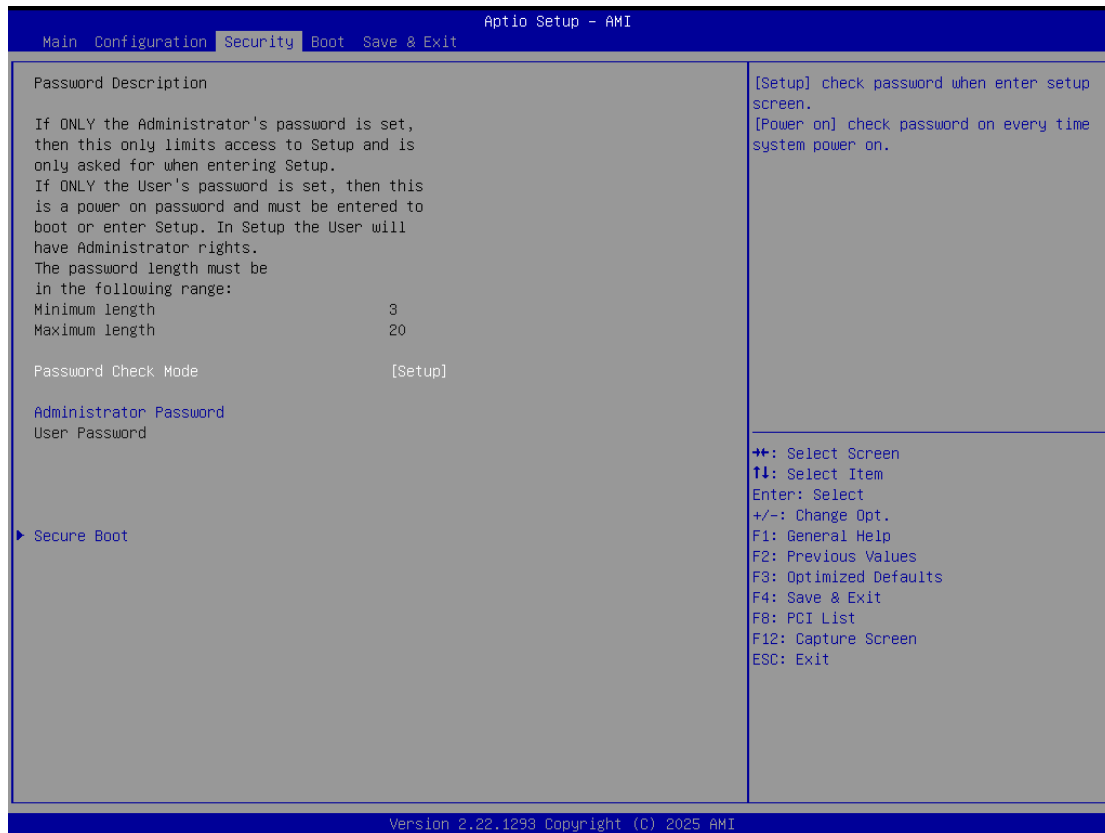
Feature	Description	Options
Blink LEDs	Identify the physical network port by blinking the associated LED.	★0

NIC Configuration



Feature	Description	Options
Link Speed	.Specifies the port speed used for the selected boot protocol.	★Auto Negotiated, 10 Mbps Half, 10 Mbps Full, 100 Mbps Half, 100 Mbps Full
Wake On Lan	Enables the server to be powered on using an in-band magic packet.	★Disabled, Enabled

6.4 Security



Feature	Description	Options
Password Check Mode	[Setup] check password when enter setup screen. [Power on] check password on every time system power on.	★ Setup, Power On
Administrator Password	Set Administrator Password	
Secure Boot	Secure Boot configuration	

Secure Boot

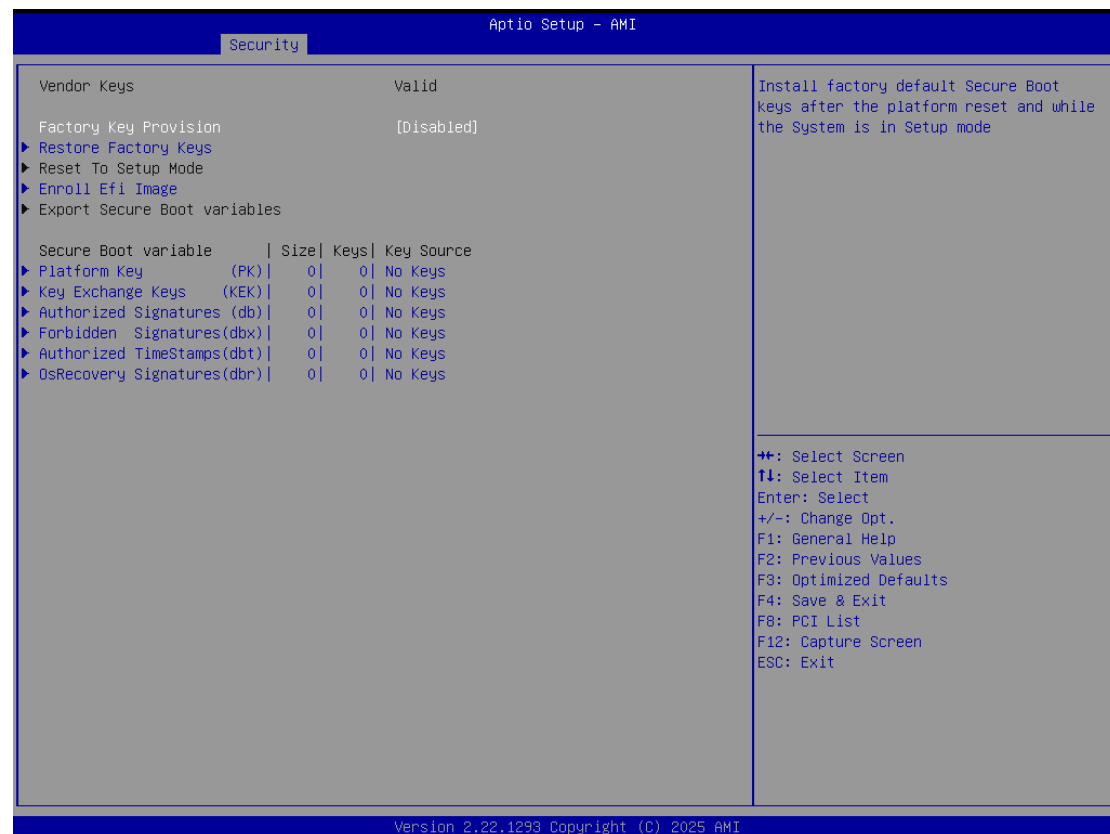
Secure Boot configuration



Feature	Description	Options
Secure Boot	Secure Boot feature is Active if Secure Boot is Enabled, Platform Key (PK) is enrolled and the System is in User mode. The mode change requires platform reset.	★Disabled, Enabled
Secure Boot Mode	Secure Boot Mode options: Standard or Custom. In Custom mode, Secure Boot Policy variables can be configured by a physically present user without full authentication	★Custom, Standard
Restore Factory keys	Force System to User Mode. Install factory default Secure Boot key databases	Yes, No
Expert Key Management	Enables expert users to modify Secure Boot Policy variables without variable authentication	

Key Management

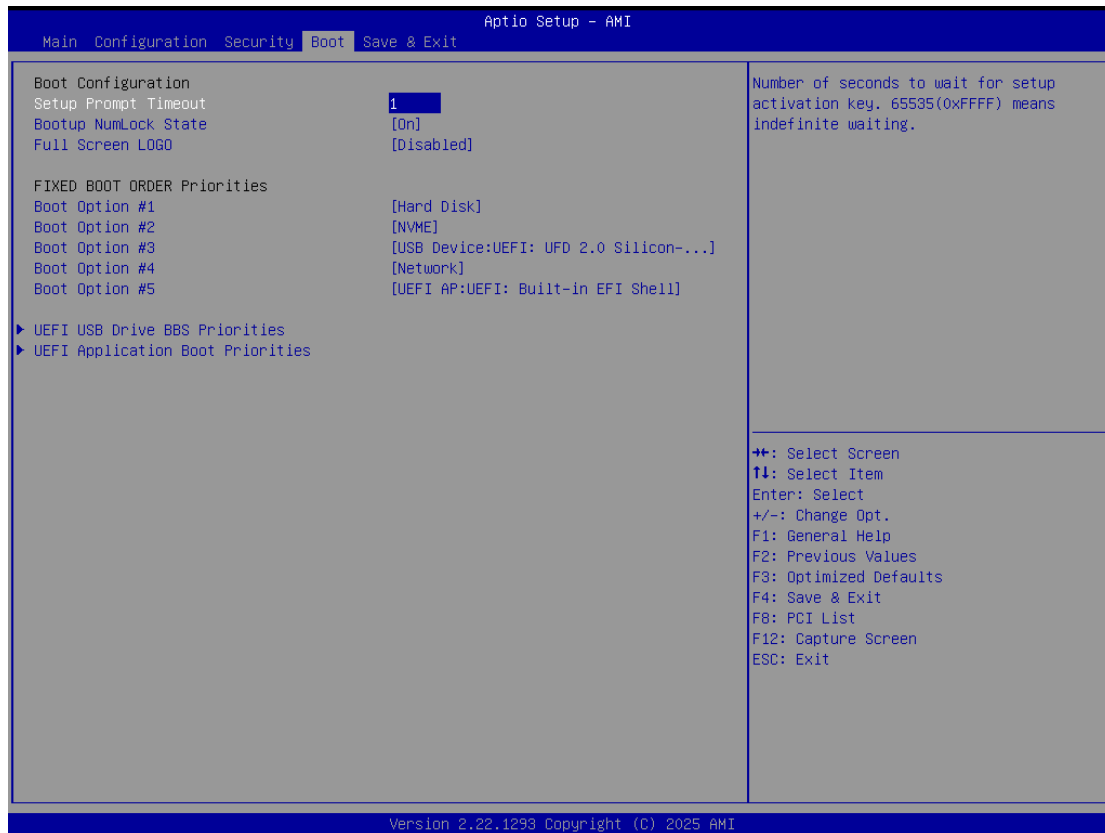
Enables expert users to modify Secure Boot Policy variables without variable authentication



Feature	Description	Options
Factory keys Provision	Install factory default Secure Boot key after the platform reset and while the System is in Setup mode.	★Disabled, Enabled
Restore Factory keys	Force System to User Mode. Install factory default Secure Boot key databases	Yes, No
Enroll Efi Image	Allow Efi image to run in Secure Boot mode. Enroll SHA256 Hash certificate of a PE image into Authorized Signature Database (db)	

Feature	Description	Key Source
Platform Key(PK)	Enroll Factory Defaults or load certificates from a file: 1.Public Key Certificate: a)EFI_SIGNATURE_LIST b) EFI_CERT_X509 (DER) c) EFI_CERT_RSA2048 (bin) d)EFI_CERT_SHAXXX 2.Authenticated UEFI Variable 3.EFI PE/COFF Image(SHA256)	Update
Key Exchange Keys(KEK)		Update, Append
Authorized Signatures (db)		Update, Append
Forbidden Signatures (dbx)		Update, Append
Authorized TimeStamps (dbt)		Update, Append
OsRecovery Signatures (dbr)		Update, Append
	Key Source: Factory, Modified, Mixed	

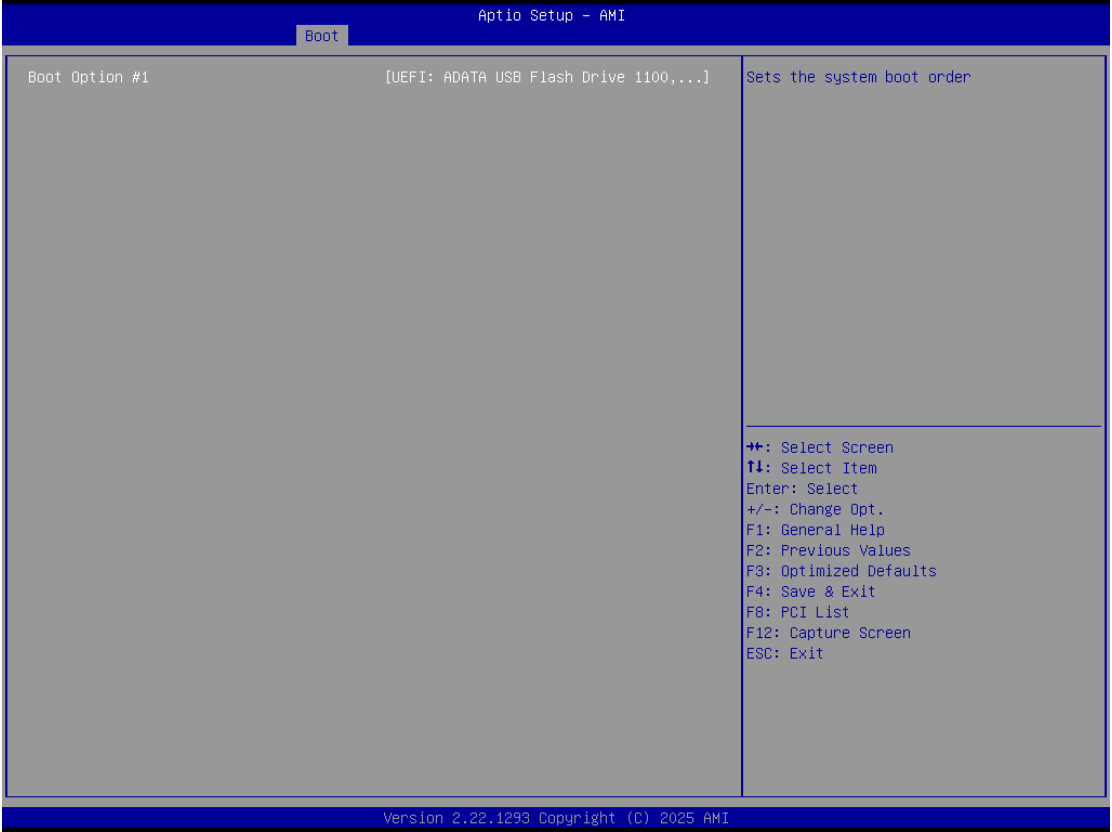
6.5 Boot



Feature	Description	Options
Setup Prompt Timeout	Number of seconds to wait for setup activation key. 65535(0xFFFF) means indefinite waiting.	★1
Bootup NumLock State	Select the keyboard NumLock state.	★On, Off
Full Screen LOGO	Enables or disables Quiet Boot option and Full screen Logo.	★Disabled, Enabled
Boot Option #1 ~ #5	Sets the system boot order	Hard Disk, NVME, USB Device, Network, UEFI AP: UEFI: Built-in EFI Shell, Disabled
UEFI USB Drive BBS Priorities	Specifies the Boot Device Priority sequence from available UEFI USB Drivers.	
UEFI Application Boot Priorities	Specifies the Boot Device Priority sequence from available UEFI Application.	

UEFI USB Drive BBS Priorities:

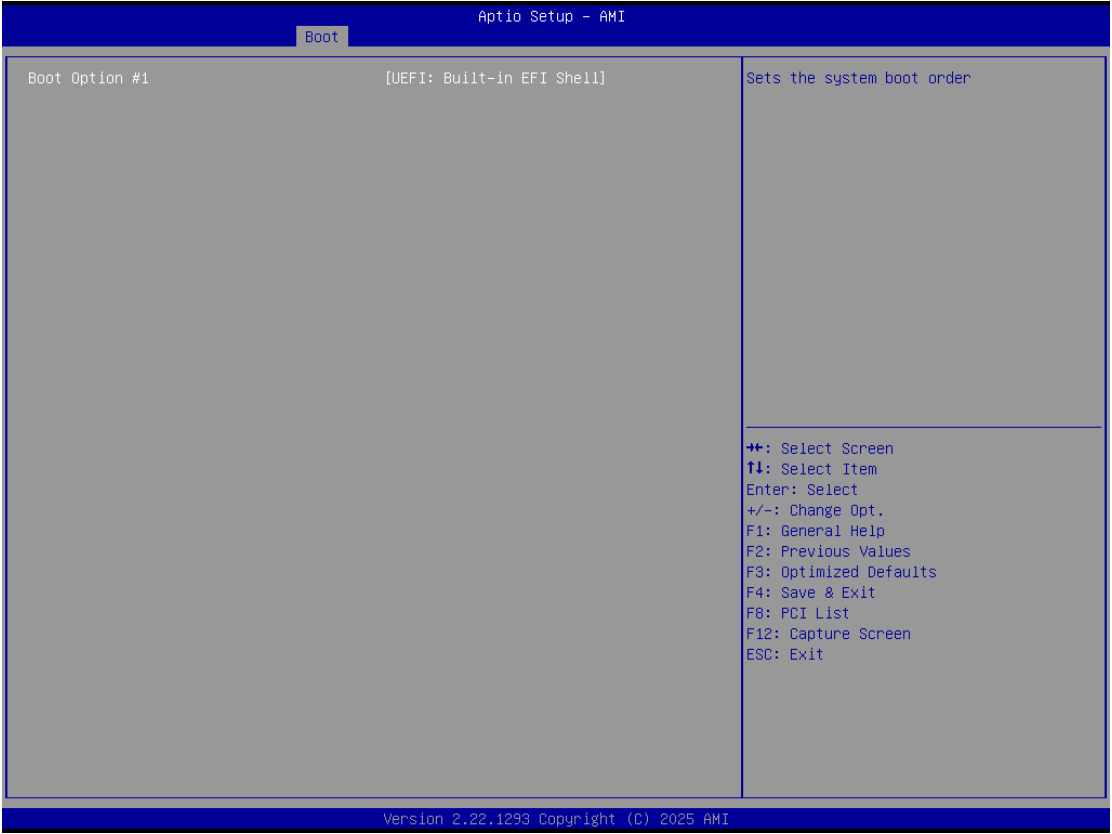
Specifies the Boot Device Priority sequence from available UEFI Hard Drive Application.



Feature	Description	Options
Boot Option #1	Sets the system boot order.	

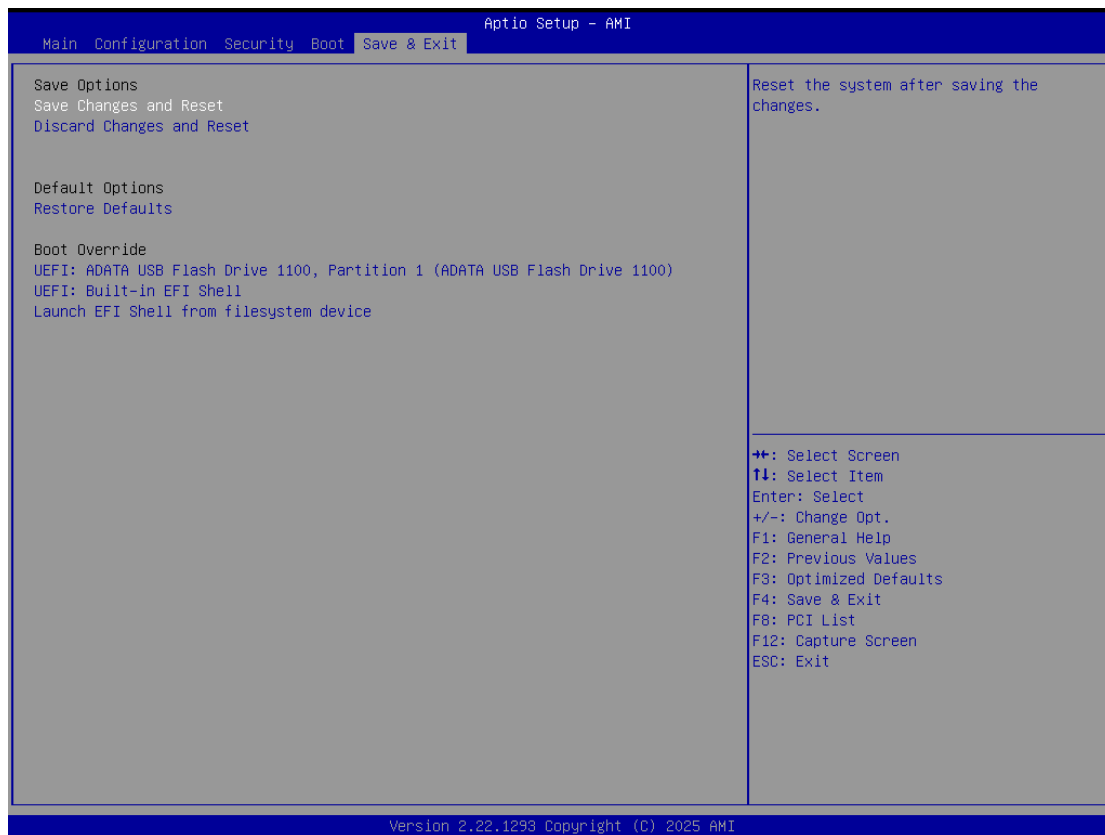
UEFI Application Boot Priorities:

Specifies the Boot Device Priority sequence from available UEFI Application.



Feature	Description	Options
Boot Option #1	Sets the system boot order.	

6.6 Save& Exit



Feature	Description	Options
Save Changes and Reset	Reset the system after saving the changes.	
Discard Changes and Reset	Reset system setup without saving any changes.	
Restore Defaults	Restore/Load Default values for all the setup options.	
UEFI: Built-in EFI Shell		
Launch EFI Shell from filesystem device	Attempts to Launch EFI Shell application (Shell.efi) from one of the available filesystem devices.	

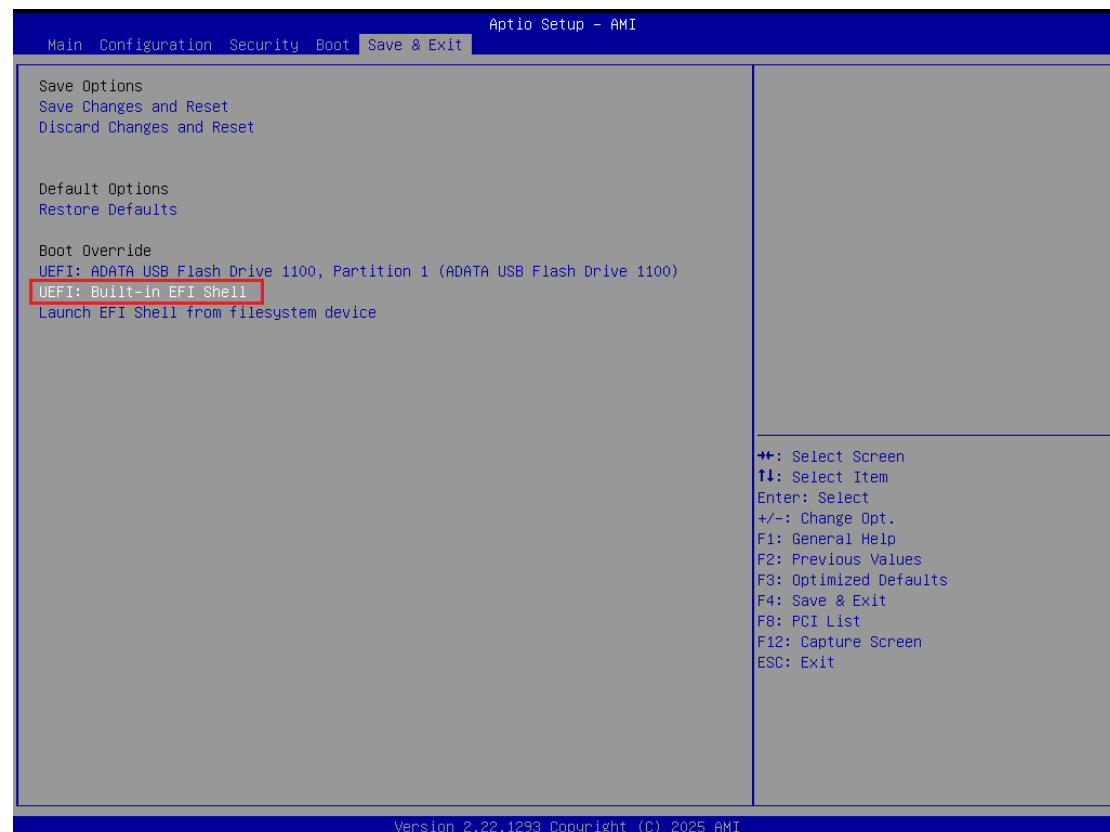
PICO-8021 BIOS UEFI Update SOP process under UEFI Shell

Step1. Prepare a USB DOK.

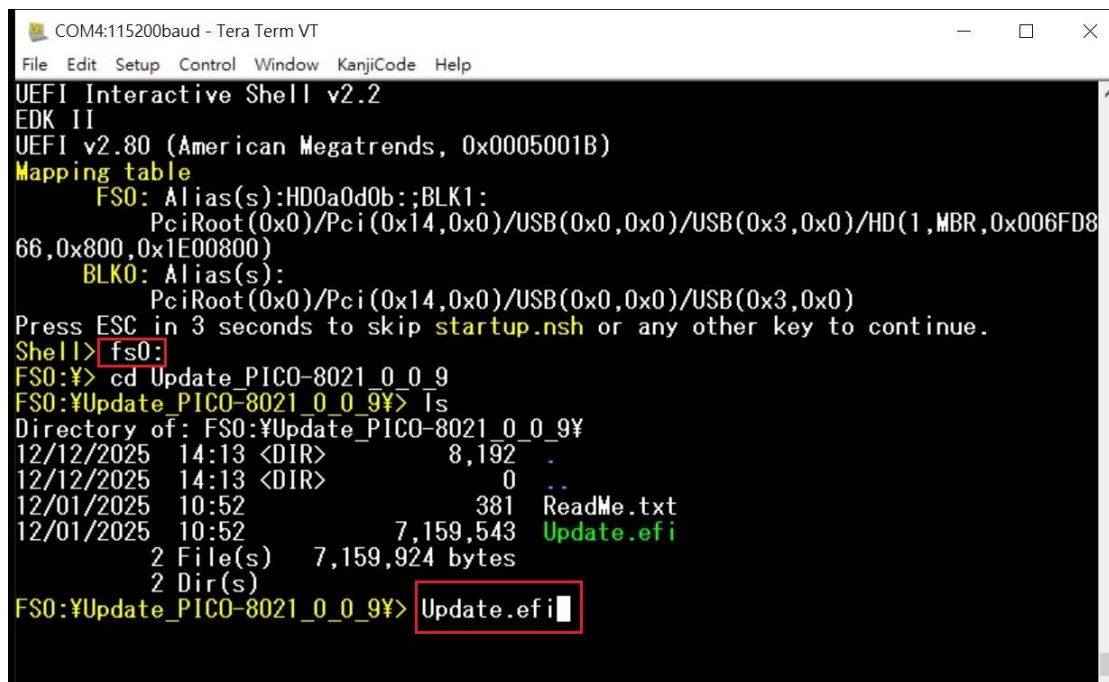
Step2. Unzip BIOS update file to the USB DOK.

Step3. Plug the USB DOK into the target system and then boot in UEFI Shell

By selecting UEFI: Built-In EFI shell in the BIOS save & Exit page.



Step4. Under the UEFI shell, direct to your USB DOK, below picture is an example using FS0. Then direct to the folder with BIOS updated file and then enter command:" Update.efi" to start updating BIOS.



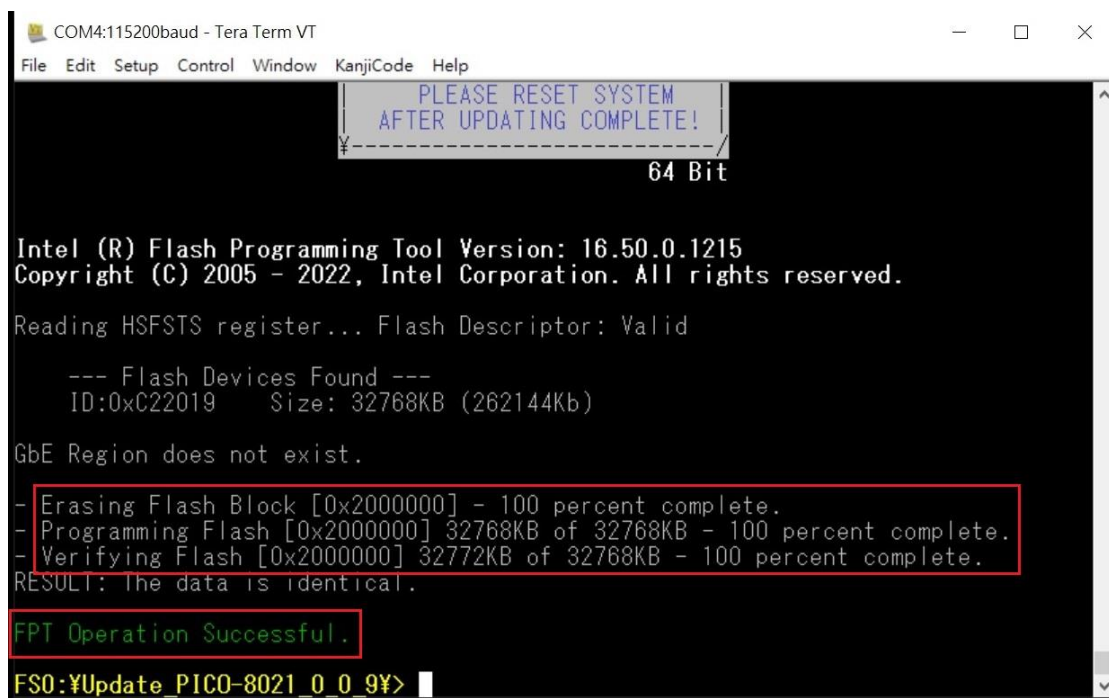
```

COM4:115200baud - Tera Term VT
File Edit Setup Control Window KanjiCode Help
UEFI Interactive Shell v2.2
EDK II
UEFI v2.80 (American Megatrends, 0x0005001B)
Mapping table
  FS0: Alias(s):HD0a0d0b:;BLK1:
        PciRoot(0x0)/Pci(0x14,0x0)/USB(0x0,0x0)/USB(0x3,0x0)/HD(1,MBR,0x006FD8
66,0x800,0x1E00800)
  BLK0: Alias(s):
        PciRoot(0x0)/Pci(0x14,0x0)/USB(0x0,0x0)/USB(0x3,0x0)
Press ESC in 3 seconds to skip startup.nsh or any other key to continue.
Shell> fs0:
FS0:¥> cd Update_PICO-8021_0_0_9
FS0:¥Update_PICO-8021_0_0_9¥> ls
Directory of: FS0:¥Update_PICO-8021_0_0_9¥
12/12/2025  14:13 <DIR>          8,192 .
12/12/2025  14:13 <DIR>          0 ..
12/01/2025  10:52              381 ReadMe.txt
12/01/2025  10:52       7,159,543 Update.efi
2 File(s)    7,159,924 bytes
2 Dir(s)
FS0:¥Update_PICO-8021_0_0_9¥> Update.efi
  
```

Step5. The updating process will start, and you can see the updating progress.

When you see the following pictures, which means the BIOS update processes finished.

Please cut the AC power off and wait for 10 seconds before powering on.



```

COM4:115200baud - Tera Term VT
File Edit Setup Control Window KanjiCode Help
PLEASE RESET SYSTEM
AFTER UPDATING COMPLETE!
64 Bit

Intel (R) Flash Programming Tool Version: 16.50.0.1215
Copyright (C) 2005 - 2022, Intel Corporation. All rights reserved.

Reading HSFSTS register... Flash Descriptor: Valid

--- Flash Devices Found ---
ID:0xC22019   Size: 32768KB (262144Kb)

GbE Region does not exist.

- Erasing Flash Block [0x20000000] - 100 percent complete.
- Programming Flash [0x20000000] 32768KB of 32768KB - 100 percent complete.
- Verifying Flash [0x20000000] 32772KB of 32768KB - 100 percent complete.
RESULT: The data is identical.

FPT Operation Successful.

FS0:¥Update_PICO-8021_0_0_9¥>
  
```

Chapter 7

System Overview

- 7 System Resources
 - 7.1 Intel Twin Lake SoC
 - 7.2 Main Memory
 - 7.3 Installing the Single Board Computer

7. System Resources

7.1 Intel® Twin Lake & Amston Lake Soc

Intel® Processor N150 (4C, 0.8GHz, 6W)

Intel® Atom x7433RE (4C, 1.5GHz, 9W)

Intel® Atom x7211RE (2C, 1.0GHz, 6W)

7.2 Main Memory

PICO-8021 supports LPDDR5. The maximum memory can be up to 16GB.

7.3 Installing the Single Board Computer

To install the PICO-8021 into a standard chassis or proprietary environment, please perform the following steps:

Step 1: Check that all jumper settings are in the proper positions.

Step 2: Install the heat spreader or heat sink in the correct position.

Step 3: Place the PICO-8021 into the designated position in the system.

Step 4: Attach cables to the existing peripheral devices and secure them.

WARNING

Please ensure that the motherboard is properly inserted and secured by the mounting mechanism.

Chapter 8

System Overview

- 8 Troubleshooting
- 8.1 Hardware Quick Installation
- 8.2 BIOS Setting
- 8.3 FAQ

8. Troubleshooting

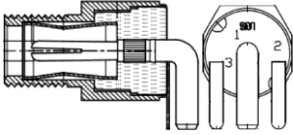
This chapter provides a few useful tips to help users quickly get the PICO-8021 up and running.

8.1 Hardware Quick Installation

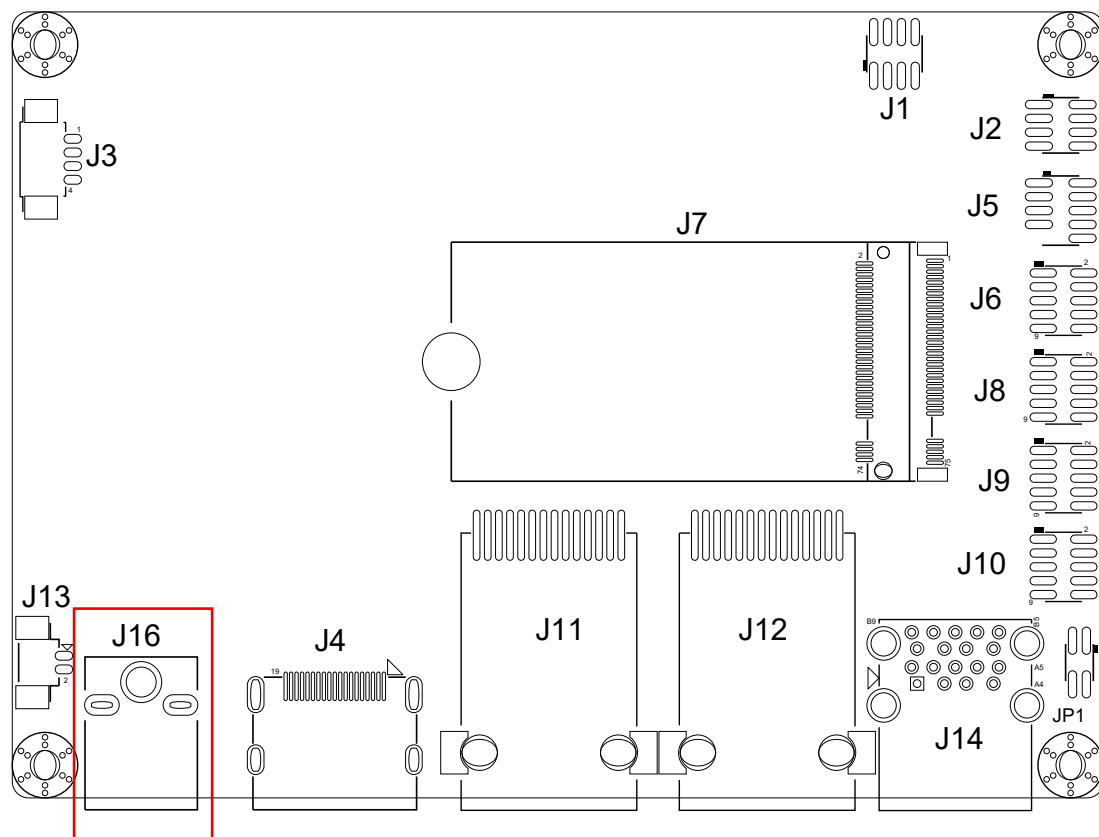
DC Jack Power

The PICO-8021 is powered via a DC jack connector, supporting an input voltage of 12V.

J16 : DC Jack

PCB Footprint	Pin No.	Signal Description	Pin No.	Signal Description
	1	Vin	3	GND
	2	GND		

Connector



8.2 BIOS Setting

It is assumed that users have correctly installed all required modules and properly connected all device cables before turning on the DC power. Keyboard, mouse, M.2 M-Key storage, HDMI connector, device power cables, and DC jack accessories are examples of items that require special attention. Without ensuring that these modules and devices are properly and correctly installed, system failures or device malfunctions may occur. To ensure a successful start-up with the PICO-8021, it is recommended that during the boot-up sequence, users press the “DEL” or “ESC” key to enter the BIOS setup menu and configure a stable BIOS environment.

Loading the default optimal settings

When prompted with the main setup menu, please scroll down to “Restore Defaults”, press “Enter”, and select “Yes” to load the default optimal BIOS settings.

This action will restore the BIOS settings to the initial factory configuration. It is recommended to perform this step to ensure that the system is running with BIOS settings officially endorsed by Portwell. In addition, users may load the default BIOS settings at any time if the system appears unstable during the boot-up sequence.

8.3 FAQ

Information & Support

● Question: Power off the system and locate the RTC battery on the PICO-8021. Remove the RTC battery and wait for 5 seconds to clear the BIOS password. Then reinstall the battery and power on the system.

● Question: How do I update the BIOS of PICO-8021?

Answer:

1. Please visit the Portwell Download Center at the following link:
<https://download.portwell.tw/>
2. Select “Search download” and enter the keyword “PICO-8021”.
3. Locate the BIOS page and download the ROM file and flashing utility.

4. Unzip the files to a bootable USB flash drive that can boot into UEFI shell mode. Then execute “update.efi” to start the BIOS update process.
5. When the message “FPT Operation Passed” appears, the BIOS update process is complete. Please power off the system and disconnect the AC power for 10 seconds before powering it on again.
6. If you require additional technical information or have requests not covered in this manual, please submit a technical support request using the following link:

<https://www.portwell.com.tw/support-center/service-request/>

We will do our best to provide appropriate suggestions or solutions.

Chapter 9

System Overview

9 Portwell Software Service

9. Portwell Software Service

1. If you have customized BIOS requirements, please contact our headquarters or local branch.
2. If you require WDT or GPIO applications, please contact our headquarters or local branch. We can provide assistance with application development.

<https://www.portwell.com.tw/portwell-worldwide/>



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