

COM Express Carrier Design Guide

Carrier Design Guideline for

PCOM-B65C

Rev. 0.1

Revision history

Rev.	Date	Note
R0.1	2026/06	First Release

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1 Introduction

The Carrier Design Guide provides the guideline of designing your own carrier board based on Portwell's COM Express Modular product PCOM-B65C. PCOM-B65C is Type 6, 95x95mm Modular board, more information is included in PCOM-B65C User's Guide and can be downloaded from Portwell download center (Or contact your Portwell sales representative for acquiring PCOM-B65C User's Guide). This carrier design guide is dedicated for the designers designing a COM Express Type 6 carrier board which will have an excellent compatibility with Portwell's PCOM-B65C modular product.

The layout guideline provided are 8 PCB layer stack up, each interface has three sections, which are detail PCOM-B65C pin out, pin name, power rail, PU/PD, AC couple capacitor etc. information are included. Second part contains PCB layout guide, impedance, maximum trace, trace width, and trace spacing etc. Third section provides the available trace length of which designers are able to optimize the high-speed signals such as PCIE, SATA, USB etc.

2 PCOM-B65C

2.1 PCOM-B65C Block Diagram

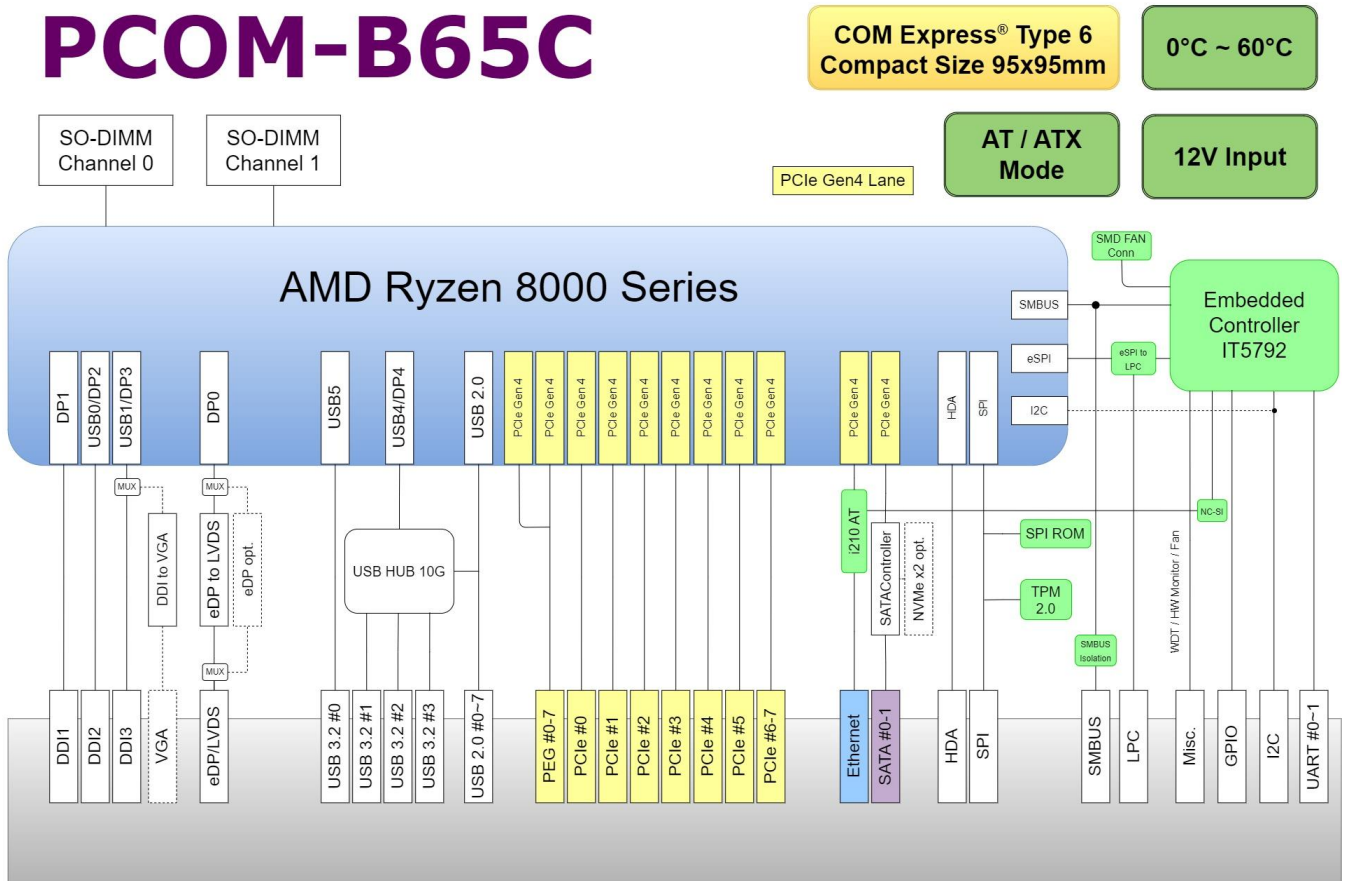


Figure 1 PCOM-B65C Block Diagram

2.2 PCOM-B65C Pin-out

A1	GND(FIXED)	B1	GND(FIXED)	C1	GND(FIXED)	D1	GND(FIXED)
A2	LAN_MDI3N	B2	LAN_LED_LNK_ACT_N	C2	GND(FIXED)	D2	GND(FIXED)
A3	LAN_MDI3P	B3	LPC_FRAME#	C3	USB3_RN1	D3	USB3_TN1
A4	LAN_LED_100_N	B4	LPC_AD0	C4	USB3_RP1	D4	USB3_TP1
A5	LAN_LED_1000_N	B5	LPC_AD1	C5	GND(FIXED)	D5	GND(FIXED)
A6	LAN_MDI2N	B6	LPC_AD2	C6	USB3_RN2	D6	USB3_TN2
A7	LAN_MDI2P	B7	LPC_AD3	C7	USB3_RP2	D7	USB3_TP2
A8	LAN_LED_LINK_N	B8	N/A	C8	GND(FIXED)	D8	GND(FIXED)
A9	LAN_MDI1N	B9	N/A	C9	USB3_RN3	D9	USB3_TN3
A10	LAN_MDI1P	B10	CLK_LPC	C10	USB3_RP3	D10	USB3_TP3
A11	GND	B11	GND(FIXED)	C11	GND(FIXED)	D11	GND(FIXED)
A12	LAN_MDI0N	B12	PWRBTN#_D	C12	USB3_RN4	D12	USB3_TN4
A13	LAN_MDI0P	B13	SMB_CLK	C13	USB3_RP4	D13	USB3_TP4
A14	N/C	B14	SMB_DATA	C14	GND(FIXED)	D14	GND(FIXED)
A15	KBC_SLP_S3#	B15	SMBALERT	C15	N/C	D15	DPB_CTRLCLK_AUX_P
A16	SATA_TXP0	B16	SATA_TXP1	C16	N/C	D16	DPB_CTRLDATA_AUX_N
A17	SATA_TXN0	B17	SATA_TXN1	C17	N/C	D17	N/C
A18	KBC_SLP_S4#	B18	ICH_SUS_STAT	C18	N/C	D18	N/C
A19	SATA_RXP0	B19	SATA_RXP1	C19	PCIE_RXP6	D19	PCIE_TXP6
A20	SATA_RXN0	B20	SATA_RXN1	C20	PCIE_RXN6	D20	PCIE_TXN6
A21	GND(FIXED)	B21	GND(FIXED)	C21	GND(FIXED)	D21	GND(FIXED)
A22	N/C	B22	N/C	C22	PCIE_RXP7	D22	PCIE_TXP7
A23	N/C	B23	N/C	C23	PCIE_RXN7	D23	PCIE_TXN7
A24	KBC_SLP_S5#	B24	CB_PWROK	C24	DDPB_HPD	D24	N/C
A25	N/C	B25	N/C	C25	N/C	D25	N/C
A26	N/C	B26	N/C	C26	N/C	D26	DPB_TXP0
A27	BATLOW_N	B27	WDTO#	C27	N/C	D27	DPB_TXN0
A28	SATA_LED#	B28	HDA_SDI2	C28	N/C	D28	N/C
A29	HDA_SYNC	B29	HDA_SDI1	C29	N/C	D29	DPB_TXP1
A30	HDA_RST#	B30	HDA_SDI0	C30	N/C	D30	DPB_TXN1

A31	GND(FIXED)	B31	GND(FIXED)	C31	GND(FIXED)	D31	GND(FIXED)
A32	HDA_BIT_CLK	B32	SPKR	C32	DPC_CTRLCLK_AUX_P	D32	DPB_TXP2
A33	HDA_SDO	B33	KBC_SCL1	C33	DPC_CTRLDATA_AUX_N	D33	DPB_TXN2
A34	BIOS_DIS0#	B34	KBC_SDA1	C34	DPC_AUX_SEL	D34	DPB_AUX_SEL
A35	THERMTRIP#_3V_C	B35	THRM#	C35	N/C	D35	N/C
A36	USB_PN6	B36	USB_PN7	C36	DPD_CTRLCLK_AUX_P	D36	DPB_TXP3
A37	USB_PP6	B37	USB_PP7	C37	DPD_CTRLDATA_AUX_N	D37	DPB_TXN3
A38	USB_OC#_6_7	B38	USB_OC#_4_5	C38	DPD_AUX_SEL	D38	N/C
A39	USB_PN4	B39	USB_PN5	C39	DPD_TXP0	D39	DPC_TXP0
A40	USB_PP4	B40	USB_PP5	C40	DPD_TXN0	D40	DPC_TXN0
A41	GND	B41	GND(FIXED)	C41	GND(FIXED)	D41	GND(FIXED)
A42	USB_PN2	B42	USB_PN3	C42	DPD_TXP1	D42	DPC_TXP1
A43	USB_PP2	B43	USB_PP3	C43	DPD_TXN1	D43	DPC_TXN1
A44	USB_OC#_2_3	B44	USB_OC#_0_1	C44	DDPD_HPD	D44	DDPC_HPD (DDI2_HPD)
A45	USB_PN0	B45	USB_PN1	C45	N/C	D45	N/C
A46	USB_PP0	B46	USB_PP1	C46	DPD_TXP2	D46	DPC_TXP2
A47	VCC3P3_RTC	B47	N/C	C47	DPD_TXN2	D47	DPC_TXN2
A48	N/C	B48	N/C	C48	N/C	D48	N/C
A49	GBE0_SDP	B49	RSTBTN_N	C49	DPD_TXP3	D49	DPC_TXP3
A50	LPC_SERIRQ	B50	BUF_PLT_RST#	C50	DPD_TXN3	D50	DPC_TXN3
A51	GND(FIXED)	B51	GND(FIXED)	C51	GND(FIXED)	D51	GND(FIXED)
A52	PCIE_TXP5	B52	PCIE_RXP5	C52	PEG0_RX_DP	D52	PEG0_TX_DP
A53	PCIE_TXN5	B53	PCIE_RXN5	C53	PEG0_RX_DN	D53	PEG0_TX_DN
A54	GPIO	B54	GPO1	C54	TYPE0	D54	N/C
A55	PCIE_TXP4	B55	PCIE_RXP4	C55	PEG1_RX_DP	D55	PEG1_TX_DP
A56	PCIE_TXN4	B56	PCIE_RXN4	C56	PEG1_RX_DN	D56	PEG1_TX_DN
A57	GND	B57	GPO2	C57	TYPE1	D57	TYPE2
A58	PCIE_TXP3	B58	PCIE_RXP3	C58	PEG2_RX_DP	D58	PEG2_TX_DP
A59	PCIE_TXN3	B59	PCIE_RXN3	C59	PEG2_RX_DN	D59	PEG2_TX_DN
A60	GND(FIXED)	B60	GND(FIXED)	C60	GND(FIXED)	D60	GND(FIXED)

A61	PCIE_TXP2	B61	PCIE_RXP2	C61	PEG3_RX_DP	D61	PEG3_TX_DP
A62	PCIE_TXN2	B62	PCIE_RXN2	C62	PEG3_RX_DN	D62	PEG3_TX_DN
A63	GP11	B63	GPO3	C63	N/C	D63	N/C
A64	PCIE_TXP1	B64	PCIE_RXP1	C64	N/C	D64	N/C
A65	PCIE_TXN1	B65	PCIE_RXN1	C65	PEG4_RX_DP	D65	PEG4_TX_DP
A66	GND	B66	PCIE_WAKE#	C66	PEG4_RX_DN	D66	PEG4_TX_DN
A67	GP12	B67	WAKE1#	C67	RAPID_SUTDN	D67	GND(FIXED)
A68	PCIE_TXP0	B68	PCIE_RXP0	C68	PEG5_RX_DP	D68	PEG5_TX_DP
A69	PCIE_TXN0	B69	PCIE_RXN0	C69	PEG5_RX_DN	D69	PEG5_TX_DN
A70	GND(FIXED)	B70	GND(FIXED)	C70	GND(FIXED)	D70	GND(FIXED)
A71	LVDS0_EDP2_P (EDP_TXP2_CN)	B71	LVDS_B0+	C71	PEG6_RX_DP	D71	PEG6_TX_DP
A72	LVDS0_EDP2_N (EDP_TXN2_CN)	B72	LVDS_B0-	C72	PEG6_RX_DN	D72	PEG6_TX_DN
A73	LVDS1_EDP1_P (EDP_TXP1_CN)	B73	LVDS_B1+	C73	GND(FIXED)	D73	GND(FIXED)
A74	LVDS1_EDP1_N (EDP_TXN1_CN)	B74	LVDS_B1-	C74	PEG7_RX_DP	D74	PEG7_TX_DP
A75	LVDS2_EDP0_P (EDP_TXP0_CN)	B75	LVDS_B2+	C75	PEG7_RX_DN	D75	PEG7_TX_DN
A76	LVDS2_EDP0_N (EDP_TXN0_CN)	B76	LVDS_B2-	C76	GND(FIXED)	D76	GND(FIXED)
A77	VDDEN (EDP_VDD_EN)	B77	LVDS_B3+	C77	N/C	D77	N/C
A78	LVDS3_P	B78	LVDS_B3-	C78	N/C	D78	N/C
A79	LVDS3_N	B79	LVDS_BKLT_EN (EDP_BKLT_EN)	C79	N/C	D79	N/C
A80	GND(FIXED)	B80	GND(FIXED)	C80	GND(FIXED)	D80	GND(FIXED)
A81	LVDSCK_DP3_P (EDP_TXP3_CN)	B81	LVDS_B_CK+	C81	N/C	D81	N/C
A82	LVDSCK_DP3_N (EDP_TXN3_CN)	B82	LVDS_B_CK-	C82	N/C	D82	N/C
A83	LVSDCK_EDPAUX_P (EDP_AUX_P_CN)	B83	LVDS_BKLT_CTRL (EDP_BKLTCTRL)	C83	N/C	D83	N/C
A84	LVSDDA_EDPAUX_N (EDP_AUX_N_CN)	B84	5VSB	C84	GND(FIXED)	D84	GND(FIXED)
A85	GP13	B85	5VSB	C85	N/C	D85	N/C
A86	N/C	B86	5VSB	C86	N/C	D86	N/C
A87	EPD_HPD_CN (eDP_HDP)	B87	5VSB	C87	GND(FIXED)	D87	GND(FIXED)
A88	CK_PCIE_SLOT_P	B88	BIOS_DIS1#	C88	N/C	D88	N/C
A89	CK_PCIE_SLOT_N	B89	CRT_RED	C89	N/C	D89	N/C
A90	GND	B90	GND(FIXED)	C90	GND(FIXED)	D90	GND(FIXED)

A91	VCC3M_SPI	B91	CRT_GREEN	C91	N/C	D91	N/C
A92	SPI_SO	B92	CRT_BLUE	C92	N/C	D92	N/C
A93	GPO0	B93	CRT_HSYNC	C93	GND(FIXED)	D93	GND(FIXED)
A94	SPI_CLK	B94	CRT_VSYNC	C94	N/C	D94	N/C
A95	SPI_SI	B95	CRT_DDC_CLK	C95	N/C	D95	N/C
A96	N/C	B96	CRT_DDC_DATA	C96	GND(FIXED)	D96	GND(FIXED)
A97	N/C	B97	SPI_CS#0	C97	N/C	D97	N/C
A98	TXDA#	B98	N/C	C98	N/C	D98	N/C
A99	RXDA#	B99	N/C	C99	N/C	D99	N/C
A100	GND(FIXED)	B100	GND(FIXED)	C100	GND(FIXED)	D100	GND(FIXED)
A101	TXDB#	B101	FAN_PWMOUT_R	C101	N/C	D101	N/C
A102	RXDB#	B102	FAN_TACHIN_R	C102	N/C	D102	N/C
A103	LID#_R	B103	SLEEP#_R	C103	GND(FIXED)	D103	GND(FIXED)
A104	VIN_12V	B104	VIN_12V	C104	VIN_12V	D104	VIN_12V
A105	VIN_12V	B105	VIN_12V	C105	VIN_12V	D105	VIN_12V
A106	VIN_12V	B106	VIN_12V	C106	VIN_12V	D106	VIN_12V
A107	VIN_12V	B107	VIN_12V	C107	VIN_12V	D107	VIN_12V
A108	VIN_12V	B108	VIN_12V	C108	VIN_12V	D108	VIN_12V
A109	VIN_12V	B109	VIN_12V	C109	VIN_12V	D109	VIN_12V
A110	GND(FIXED)	B110	GND(FIXED)	C110	GND(FIXED)	D110	GND(FIXED)

Table 1 PCOM-B65C Pin-Out

3 COM Express Interface

3.1 PCIe

PCOM-B65C PCIe#0~#7 /PEG#0~#7 Tx signal

Pin#	Pin Name	COM e 3.0/3.1 Specification (Signals Requiring Module Termination)	Pin Typ	B65C Module	Pwr Rail /Tolerance(Volt)	
A68	PCIE_TX0+	AC coupled on the Module	O PCIE	0.22uF AC coupled on the Module(Gen3/4).	AC coupled on Module	
A69	PCIE_TX0-					
A64	PCIE_TX1+					
A65	PCIE_TX1-					
A61	PCIE_TX2+					
A62	PCIE_TX2-					
A58	PCIE_TX3+					
A59	PCIE_TX3-					
A55	PCIE_TX4+					
A56	PCIE_TX4-					
A52	PCIE_TX5+					
A53	PCIE_TX5-					
D19	PCIE_TX6+					
D20	PCIE_TX6-					
D22	PCIE_TX7+					
D23	PCIE_TX7-					
D52	PEG_TX0+					
D53	PEG_TX0-					
D55	PEG_TX1+					
D56	PEG_TX1-					
D58	PEG_TX2+					
D59	PEG_TX2-					
D61	PEG_TX3+					
D62	PEG_TX3-					
D65	PEG_TX4+					
D66	PEG_TX4-					
D68	PEG_TX5+					
D69	PEG_TX5-					
D71	PEG_TX6+					
D72	PEG_TX6-					
D74	PEG_TX7+					
D75	PEG_TX7-					

Table 2 PCOM-B65C PCIe/PEG TX

PCOM-B65C PCIe #0~#7 / PEG#0~#7 Rx signal

Pin#	Pin Name	COMe 3.0/3.1 Specification (Signals Requiring Module Termination)	Pin Typ	Module	Pwr Rail / Tolerance(Volt)
B68	PCIe RX0+	AC coupled off the Module.	I PCIe	AC coupled off Module	AC coupled off Module
B69	PCIe RX0-				
B64	PCIe RX1+				
B65	PCIe RX1-				
B61	PCIe RX2+				
B62	PCIe RX2-				
B58	PCIe RX3+				
B59	PCIe RX3-				
B55	PCIe RX4+				
B56	PCIe RX4-				
B52	PCIe RX5+				
B53	PCIe RX5-				
C19	PCIe RX6+				
C20	PCIe RX6-				
C22	PCIe RX7+				
C23	PCIe RX7-				
C52	PEG RX0+				
C53	PEG RX0-				
C55	PEG RX1+				
C56	PEG RX1-				
C58	PEG RX2+				
C59	PEG RX2-				
C61	PEG RX3+				
C62	PEG RX3-				
C65	PEG RX4+				
C66	PEG RX4-				
C68	PEG RX5+				
C69	PEG RX5-				
C71	PEG RX6+				
C72	PEG RX6-				
C74	PEG RX7+				
C75	PEG RX7-				
A88	PCIe CLK REF+	Reference clock output for all PCI Express and PCI Express Graphics lanes.	O PCIe	-	PCIe
A89	PCIe CLK REF-				

Table 3 PCOM-B65C PCIe/PEG RX

3.1.1 AC Coupling Capacitor

PCIE / PEG AC Coupling : Device Down

While PCIE devices are designed on COM Express Carrier Board, the AC coupling Capacitor should be added on the carrier, please refer to below diagram.

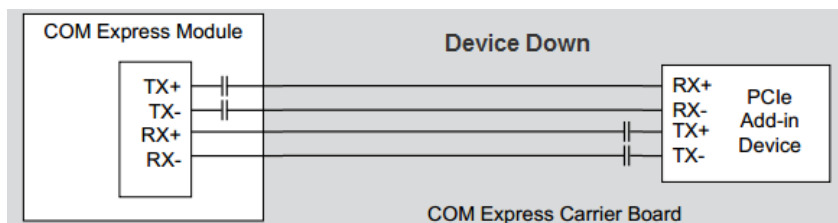


Figure 2 PCIE AC Coupling Capacitor - Device Down
(From PICMG COM Express Carrier Board Design Guide)

PCIE / PEG AC Coupling : Add-In Card

While PCIE devices are designed as Add In Card, the AC coupling Capacitor should be on PCle Add-In Card, rather than on the COM Express Carrier Board, please refer to below diagram.

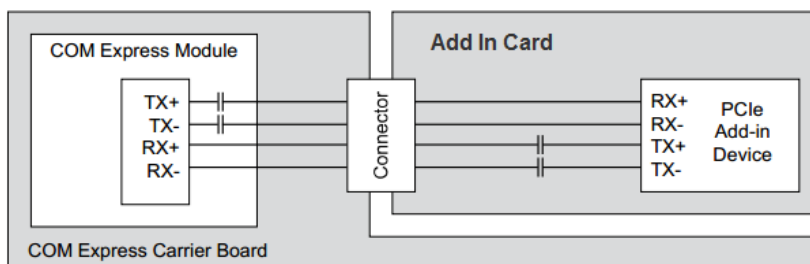


Figure 3 PCIE AC Coupling Capacitor - Add In Card
(From PICMG COM Express Carrier Board Design Guide)

3.1.2 PCB layout guideline - PCIe/PEG

Parameter	PCIe Gen2 / Gen3	PCIe Gen4
Bandwidth	5G / 8G	16 G
Maximum signal line length (coupled traces) TX and RX	10/12 inch (Add In Card/ Device Down)	8/11 inch (Add In Card/ Device Down)
Differential impedance	85 Ω +/-10%	85 Ω +/-10%
Single-ended Impedance	50 Ω +/-10%	50 Ω +/-10%
Trace width (W)	4.5 mil PCB stack-up dependent	4.5 mil PCB stack-up dependent
Spacing between differential pairs (intra-pair) (S)	4.5 mil PCB stack-up dependent	4.5 mil PCB stack-up dependent
Spacing between RX and TX pairs (inter-pair) (s)	Microstrip > 7H Stripline > 5H	Microstrip > 9H Stripline > 5H
Length matching between differential pairs (intra-pair)	Max. 5mils	Max. 5mils
Reference plane	GND referenced preferred	GND referenced preferred
Spacing from edge of plane	Min. 10*W mils (W=trace width)	Min. 10*W mils (W=trace width)
Via Usage	Max. 1 vias/ Max. 2 vias (Add In Card/ Device Down)	Max. 1 vias/ Max. 2 vias (Add In Card/ Device Down)

Table 4 PCIE/PEG Layout information

3.1.3 Passive Devices

AC Cap value (Gen2)	Min = 75nf Max = 200nf	PCOM-B65C AC Cap value 220nF
AC Cap value (Gen3/Gen4)	Min = 176nf Max = 265nf	

Table 5 PCIE/PEG AC coupling capacitor value

3.1.4 Reference schematic - PCOM-C60B R1

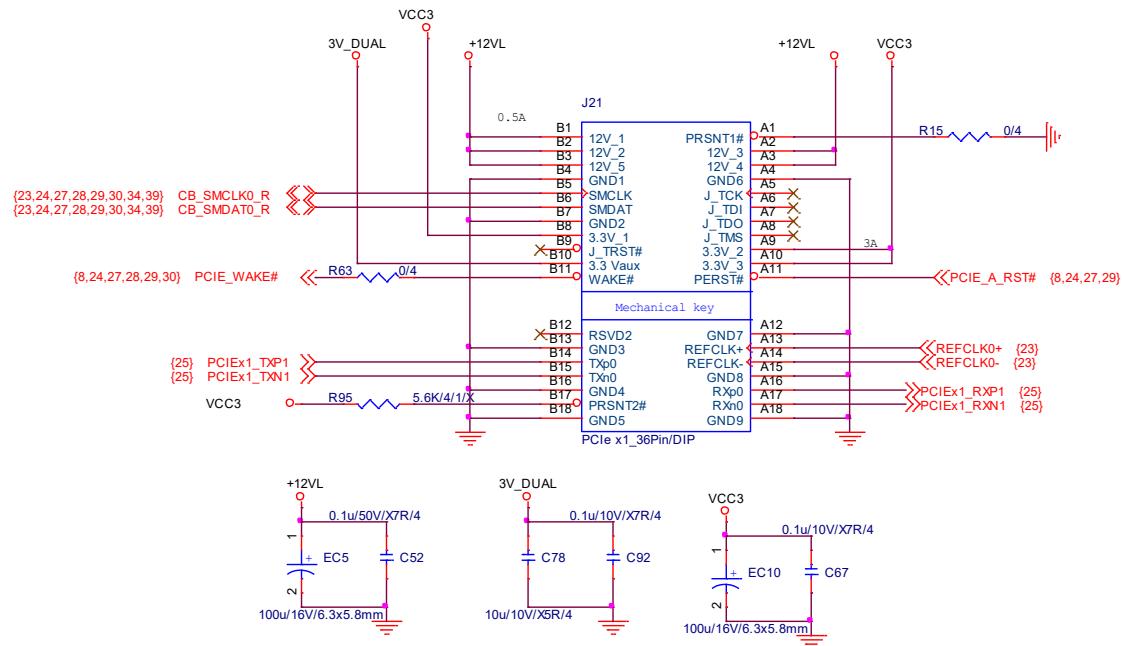


Figure 4 PCIe x1 reference schematic-1

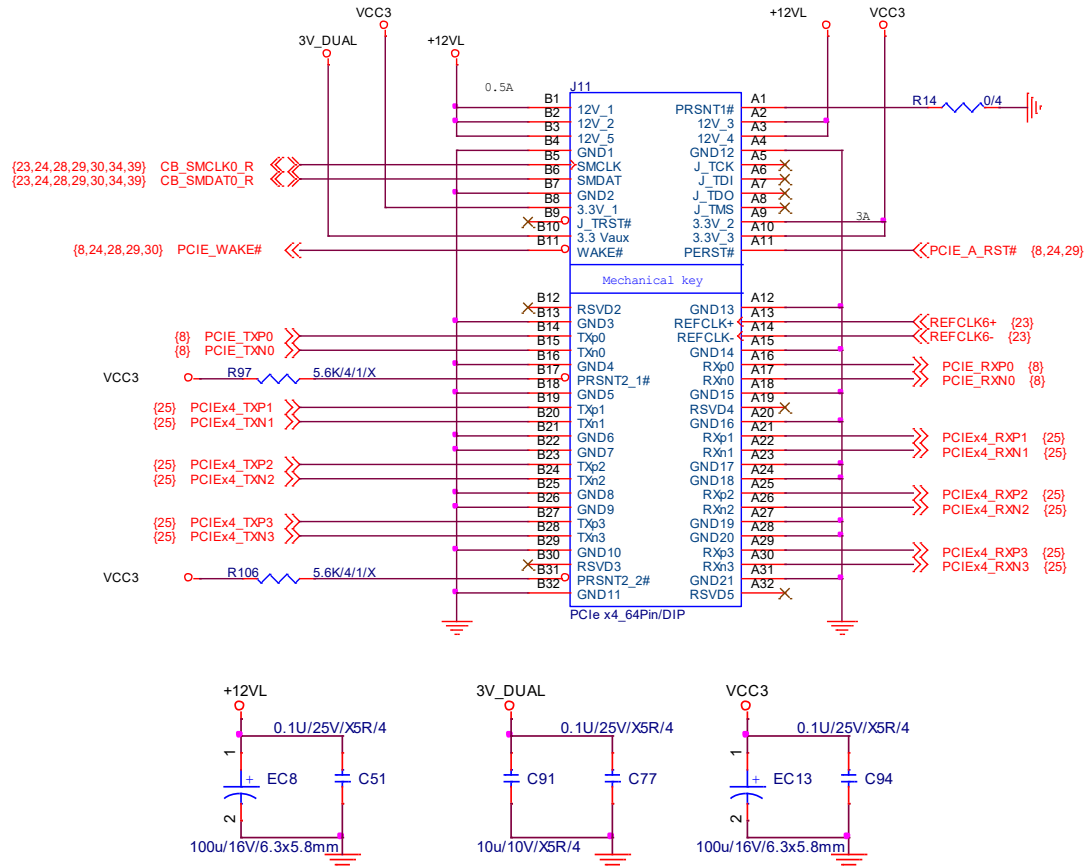


Figure 5 PCIe x4 reference schematic-2

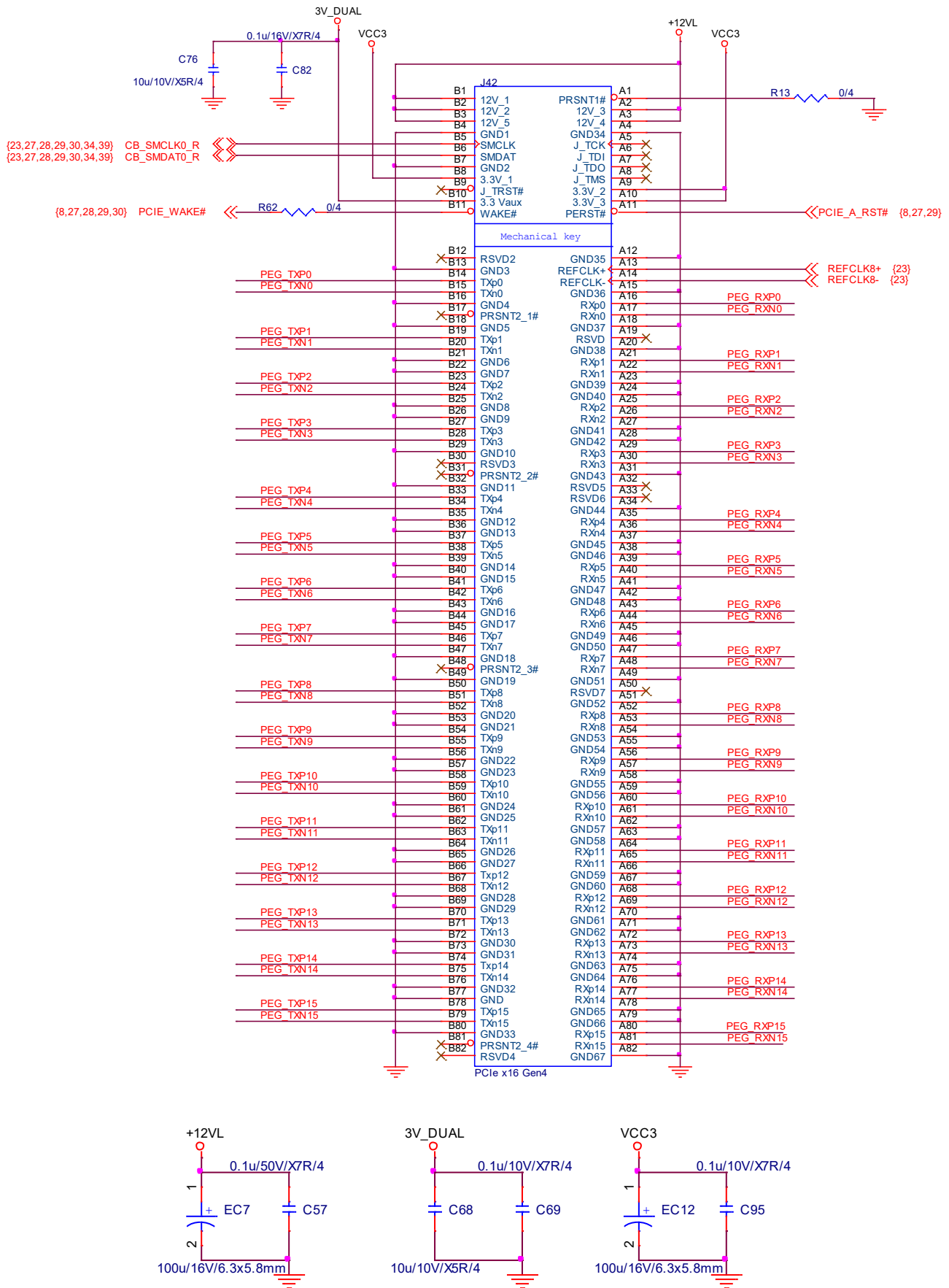


Figure 6 PCIe x16 reference schematic-3

3.1.5 Max trace length and available carrier trace length - PCIe (Device Down)

PCIe Device Down Topology

PIN	Name	Module Length	Max Length	Available Carrier length (Device Down Topology)
A68	PCIE_TX0+	2915.27	11000	8084.73
A69	PCIE_TX0-	2919.20	11000	8080.80
A64	PCIE_TX1+	2818.18	11000	8181.82
A65	PCIE_TX1-	2820.79	11000	8179.21
A61	PCIE_TX2+	2666.45	11000	8333.55
A62	PCIE_TX2-	2668.01	11000	8331.99
A58	PCIE_TX3+	2569.22	11000	8430.78
A59	PCIE_TX3-	2565.46	11000	8434.54
A55	PCIE_TX4+	2779.85	11000	8220.15
A56	PCIE_TX4-	2776.11	11000	8223.89
A52	PCIE_TX5+	2884.37	11000	8115.63
A53	PCIE_TX5-	2879.48	11000	8120.52
D19	PCIE_TX6+	1065.44	11000	9934.56
D20	PCIE_TX6-	1061.51	11000	9938.49
D22	PCIE_TX7+	1122.71	11000	9877.29
D23	PCIE_TX7-	1120.61	11000	9879.39
D52	PEG_TX0+	1072.38	11000	9927.62
D53	PEG_TX0-	1070.45	11000	9929.55
D55	PEG_TX1+	1079.06	11000	9920.94
D56	PEG_TX1-	1076.93	11000	9923.07
D58	PEG_TX2+	1069.41	11000	9930.59
D59	PEG_TX2-	1064.65	11000	9935.35
D61	PEG_TX3+	1095.05	11000	9904.95
D62	PEG_TX3-	1091.96	11000	9908.04
D65	PEG_TX4+	1077.44	11000	9922.56
D66	PEG_TX4-	1075.23	11000	9924.77
D68	PEG_TX5+	1110.73	11000	9889.27
D69	PEG_TX5-	1111.22	11000	9888.78
D71	PEG_TX6+	1100.40	11000	9899.60
D72	PEG_TX6-	1102.25	11000	9897.75
D74	PEG_TX7+	1102.34	11000	9897.66
D75	PEG_TX7-	1099.67	11000	9900.33

B68	PCIE_RX0+	2134.11	11000	8865.89
B69	PCIE_RX0-	2130.77	11000	8869.23
B64	PCIE_RX1+	1696.42	11000	9303.58
B65	PCIE_RX1-	1698.25	11000	9301.75
B61	PCIE_RX2+	1370.92	11000	9629.08
B62	PCIE_RX2-	1368.47	11000	9631.53
B58	PCIE_RX3+	1375.2	11000	9624.80
B59	PCIE_RX3-	1378.22	11000	9621.78
B55	PCIE_RX4+	1909.5	11000	9090.50
B56	PCIE_RX4-	1904.67	11000	9095.33
B52	PCIE_RX5+	1438.91	11000	9561.09
B53	PCIE_RX5-	1440.6	11000	9559.40
C19	PCIE_RX6+	1084.86	11000	9915.14
C20	PCIE_RX6-	1086.74	11000	9913.26
C22	PCIE_RX7+	1138.62	11000	9861.38
C23	PCIE_RX7-	1135.17	11000	9864.83
C52	PEG_RX0+	1371.68	11000	9628.32
C53	PEG_RX0-	1376.06	11000	9623.94
C55	PEG_RX1+	1432.39	11000	9567.61
C56	PEG_RX1-	1436.03	11000	9563.97
C58	PEG_RX2+	1553.48	11000	9446.52
C59	PEG_RX2-	1555	11000	9445.00
C61	PEG_RX3+	1513.96	11000	9486.04
C62	PEG_RX3-	1512.92	11000	9487.08
C65	PEG_RX4+	1497.89	11000	9502.11
C66	PEG_RX4-	1500.58	11000	9499.42
C68	PEG_RX5+	1526.79	11000	9473.21
C69	PEG_RX5-	1526	11000	9474.00
C71	PEG_RX6+	1505.73	11000	9494.27
C72	PEG_RX6-	1505.23	11000	9494.77
C74	PEG_RX7+	1519.26	11000	9480.74
C75	PEG_RX7-	1521.68	11000	9478.32
A88	PCIE_CLK_REF+	1808.65	11000	9191.35
A89	PCIE_CLK_REF-	1807.74	11000	9192.26

Table 6 PCIe carrier available traces - Device Down

3.1.6 Max trace length and available carrier trace length - PCIe (Add In Card)

PCIe Add In Card topology

PIN	Name	Module Length	Max Length	Available Carrier length ((AIC Topology))
A68	PCIE_TX0+	2915.27	8000	5084.73
A69	PCIE_TX0-	2919.20	8000	5080.80
A64	PCIE_TX1+	2818.18	8000	5181.82
A65	PCIE_TX1-	2820.79	8000	5179.21
A61	PCIE_TX2+	2666.45	8000	5333.55
A62	PCIE_TX2-	2668.01	8000	5331.99
A58	PCIE_TX3+	2569.22	8000	5430.78
A59	PCIE_TX3-	2565.46	8000	5434.54
A55	PCIE_TX4+	2779.85	8000	5220.15
A56	PCIE_TX4-	2776.11	8000	5223.89
A52	PCIE_TX5+	2884.37	8000	5115.63
A53	PCIE_TX5-	2879.48	8000	5120.52
D19	PCIE_TX6+	1065.44	8000	6934.56
D20	PCIE_TX6-	1061.51	8000	6938.49
D22	PCIE_TX7+	1122.71	8000	6877.29
D23	PCIE_TX7-	1120.61	8000	6879.39
D52	PEG_TX0+	1072.38	8000	6927.62
D53	PEG_TX0-	1070.45	8000	6929.55
D55	PEG_TX1+	1079.06	8000	6920.94
D56	PEG_TX1-	1076.93	8000	6923.07
D58	PEG_TX2+	1069.41	8000	6930.59
D59	PEG_TX2-	1064.65	8000	6935.35
D61	PEG_TX3+	1095.05	8000	6904.95
D62	PEG_TX3-	1091.96	8000	6908.04
D65	PEG_TX4+	1077.44	8000	6922.56
D66	PEG_TX4-	1075.23	8000	6924.77
D68	PEG_TX5+	1110.73	8000	6889.27
D69	PEG_TX5-	1111.22	8000	6888.78
D71	PEG_TX6-	1100.40	8000	6899.60
D72	PEG_TX6+	1102.25	8000	6897.75
D74	PEG_TX7-	1102.34	8000	6897.66
D75	PEG_TX7+	1099.67	8000	6900.33

B68	PCIE_RX0+	2190.68	8000	5865.89
B69	PCIE_RX0-	2186.77	8000	5869.23
B64	PCIE_RX1+	2310.45	8000	6303.58
B65	PCIE_RX1-	2306.61	8000	6301.75
B61	PCIE_RX2+	2247.03	8000	6629.08
B62	PCIE_RX2-	2248.92	8000	6631.53
B58	PCIE_RX3+	2295.32	8000	6624.80
B59	PCIE_RX3-	2290.97	8000	6621.78
B55	PCIE_RX4+	2389.89	8000	6090.50
B56	PCIE_RX4-	2385.53	8000	6095.33
B52	PCIE_RX5+	2641.51	8000	6561.09
B53	PCIE_RX5-	2643.16	8000	6559.40
C19	PCIE_RX6+	2775.38	8000	6915.14
C20	PCIE_RX6-	2773.26	8000	6913.26
C22	PCIE_RX7+	2720.6	8000	6861.38
C23	PCIE_RX7-	2716.64	8000	6283.36
C52	PEG_RX0+	2775.38	8000	6628.32
C53	PEG_RX0-	2773.26	8000	6623.94
C55	PEG_RX1+	2720.6	8000	6567.61
C56	PEG_RX1-	2716.64	8000	6563.97
C58	PEG_RX2+	2723.86	8000	6446.52
C59	PEG_RX2-	2725.05	8000	6445.00
C61	PEG_RX3+	2603.47	8000	6486.04
C62	PEG_RX3-	2600.87	8000	6487.08
C65	PEG_RX4+	2540.48	8000	6502.11
C66	PEG_RX4-	2535.8	8000	6499.42
C68	PEG_RX5+	2519.16	8000	6473.21
C69	PEG_RX5-	2522.26	8000	6474.00
C71	PEG_RX6+	2539.99	8000	6494.27
C72	PEG_RX6-	2539.75	8000	6494.77
C74	PEG_RX7+	2377.17	8000	6480.74
C75	PEG_RX7-	2373.81	8000	6478.32
A88	PCIE_CLK_REF+	3318.07	11000	9191.35
A89	PCIE_CLK_REF-	3320.29	11000	9192.26

Table 7 PCIE carrier available traces - Add In Card

3.2 USB 2.0/3.0

PCOM- B65C USB2.0

Pin#	Pin Name	COM e 3.0/3.1 Specification (Signals Requiring Module Termination)	Pin Typ	B65C Module	Pwr Rail /Tolerance(Volt)
A45	USB0-	No termination is required on USB pairs.	I/O USB	SoC to Com Express Row connector.	3.3V Suspend/3.3V
A46	USB0+				
B45	USB1-				
B46	USB1+				
A42	USB2-				
A43	USB2+				
B42	USB3-				
B43	USB3+				
A39	USB4-				
A40	USB4+				
B39	USB5-				
B40	USB5+				
A36	USB6-				
A37	USB6+				
B36	USB7-				
B37	USB7+				
B44	USB 0 1 OC#	Pulled up to 3.3V standby on module with a 10K Ω resistor	I CMOS	PU 10k ohm	3.3V Suspend/3.3V
A44	USB 2 3 OC#				
B38	USB 4 5 OC#				
A38	USB 6 7 OC#				

Table 8 B65C USB 2.0

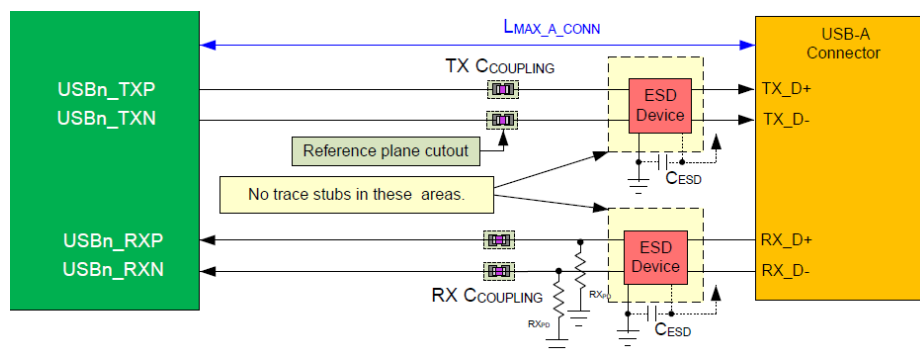
PCOM- B65C USB3.0

Pin#	Pin Name	COM e 3.0/3.1 Specification (Signals Requiring Module Termination)	Pin Typ	Module	Pwr Rail /Tolerance(Volt)
C3	USB SSRX0-	AC coupled off Module.	I PCIE	0.33uF AC coupled on the Module for AMD	AC coupled off Module.
C4	USB SSRX0+				
C6	USB SSRX1-				
C7	USB SSRX1+				
C9	USB SSRX2-				
C10	USB SSRX2+				
C12	USB SSRX3-	AC coupled on Module.	O PCIE	0.22uF AC coupled on the Module	AC coupled on Module
C13	USB SSRX3+				
D3	USB SSTX0-				
D4	USB SSTX0+				
D6	USB SSTX1-				
D7	USB SSTX1+				
D9	USB SSTX2-				
D10	USB SSTX2+				
D12	USB SSTX3-				
D13	USB SSTX3+				

Table 9 B65C USB 3.0

Note

RX_{PD}: pull-down resistor to VSS, it is recommended to reserve



3.2.1 PCB layout guideline - USB2.0/3.0

Parameter	Trace Routing	Trace Routing
Transfer rate / Port	480 Mbit/s	5/10 Gbit/s
Maximum signal line length (coupled traces)	Max. 12.0 inches / 9 inches	Max. 5 inches
Differential Impedance	85 Ω +/-10%	85 Ω +/-10%
Single-ended Impedance	50 Ω +/-10%	50 Ω +/-10%
Trace width (W)	4.5 mil PCB stack-up dependent	4.5 mil PCB stack-up dependent
Spacing between differential pairs (intra-pair) (S)	4.5 mil PCB stack-up dependent	4.5 mil PCB stack-up dependent
Spacing between RX and TX, RX and RX pairs (inter-pair) (s)	Microstrip > 7H Stripline > 7H	Microstrip > 10H Stripline > 8H
Spacing between TX and TX pairs (inter-pair) (s)	Microstrip > 7H Stripline > 7H	Microstrip > 7H Stripline > 6H
Length matching between differential pairs (intra-pair)	5 mils	3 mils
Reference plane	GND referenced preferred	GND referenced preferred
Spacing from edge of plane	Min. 10*W mils (W=trace width)	Min. 10*W mils (W=trace width)
Via Usage	Max. 1 vias	Max. 1 vias

Table 10 USB 2.0 / 3.0 Layout information

3.2.2 Reference schematic - PCOM-C60B

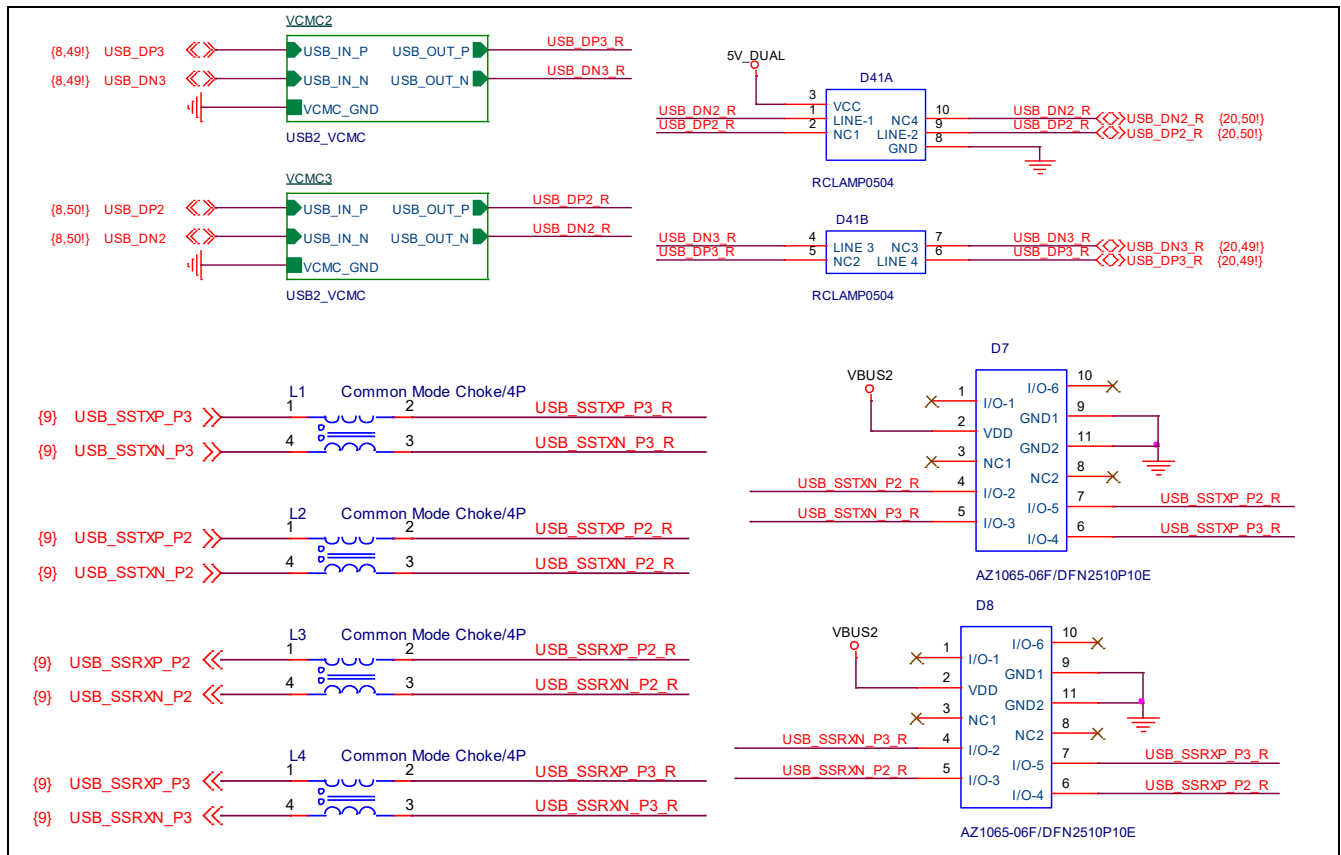


Figure 7 USB 2.0 / 3.0 Reference schematic 1

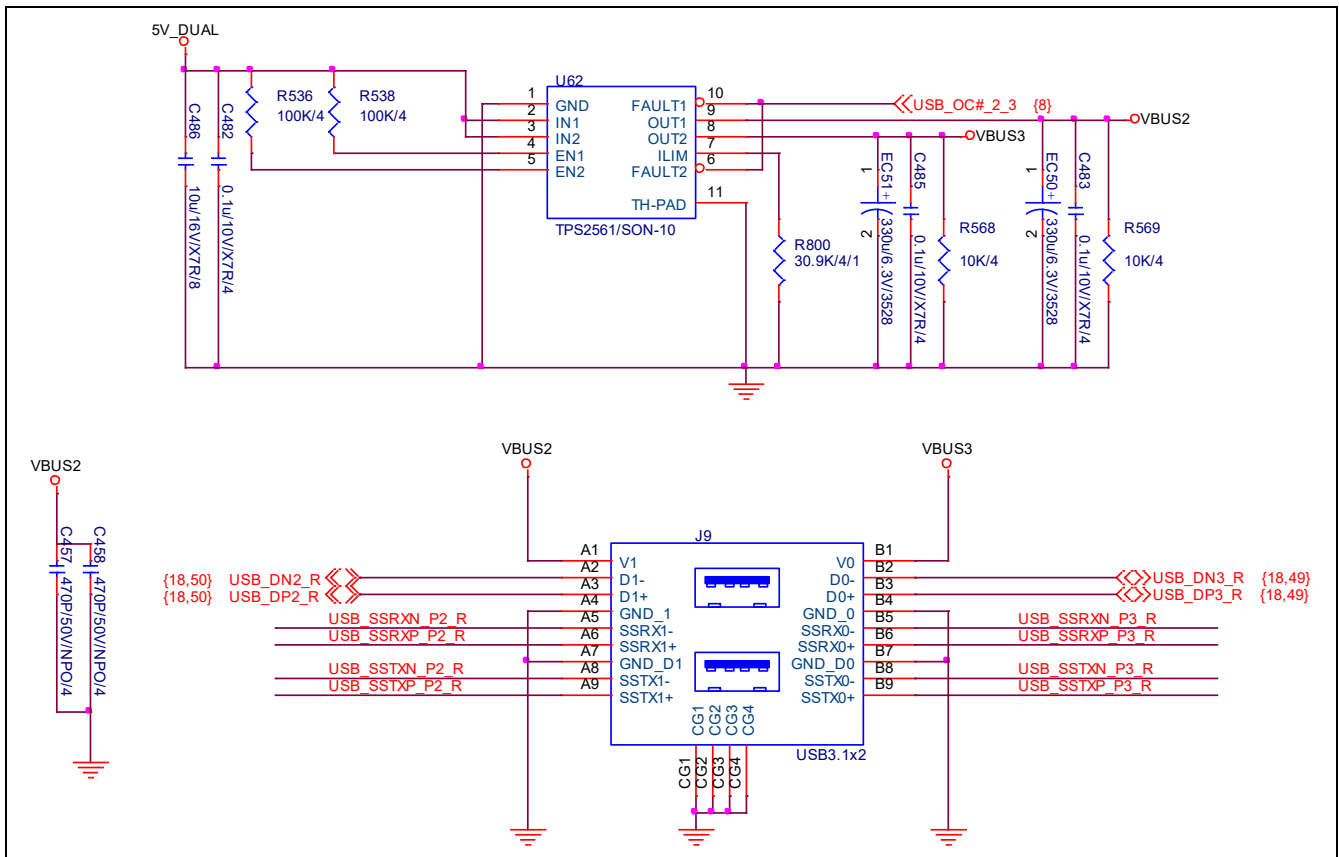


Figure 8 USB 2.0 / 3.0 Reference schematic 2

3.2.3 Max trace length and available carrier trace length - USB 2.0 / 3.0

PIN	Name	Module Length	Max Length	Available Carrier length
A45	USB0-	2135.66	12000	9864.34
A46	USB0+	2137.56	12000	9862.44
B45	USB1-	1142.12	9000	7857.88
B46	USB1+	1145.2	9000	7854.8
A42	USB2-	682.52	9000	8317.48
A43	USB2+	686.07	9000	8313.93
B42	USB3-	604.16	9000	8395.84
B43	USB3+	604.69	9000	8395.31
A39	USB4-	2665.28	12000	9334.72
A40	USB4+	2663.47	12000	9336.53
B39	USB5-	1494.53	12000	10505.47
B40	USB5+	1493.98	12000	10506.02

A36	USB6-	2403.95	12000	9596.05
A37	USB6+	2402.19	12000	9597.81
B37	USB7-	1724.09	12000	10275.91
B38	USB7+	1726.65	12000	10273.35
C3	USB_SSRX0-	1709.21	5000	3290.79
C4	USB_SSRX0+	1706.45	5000	3293.55
C6	USB_SSRX1-	646.06	5000	4353.94
C7	USB_SSRX1+	646.02	5000	4353.98
C9	USB_SSRX2-	722.01	5000	4277.99
C10	USB_SSRX2+	722.7	5000	4277.3
C12	USB_SSRX3-	280.17	5000	4719.83
C13	USB_SSRX3+	282.45	5000	4717.55
D3	USB_SSTX0-	1017.51	5000	3982.49
D4	USB_SSTX0+	1021.16	5000	3978.84
D6	USB_SSTX1-	1154.62	5000	3845.38
D7	USB_SSTX1+	1157.92	5000	3842.08
D9	USB_SSTX2-	1136.85	5000	3863.15
D10	USB_SSTX2+	1137.11	5000	3862.89
D12	USB_SSTX3-	875.79	5000	4124.21
D13	USB_SSTX3+	872.94	5000	4127.06

Table 11 Carrier available traces - USB 2.0 / 3.0

3.3 GbE LAN

PCOM-B65C LAN

Pin#	Pin Name	COM e 3.0/3.1 Specification (Signals Requiring Module Termination)	Pin Typ	B65C Module	Pwr Rail /Tolerance(Volt)
A12	GBE0 MDI0-	-	I/O Analog	Media Dependent Interface signal. I210 chip on Module.	3.3V max Suspend
A13	GBE0 MDI0+				
A9	GBE0 MDI1-				
A10	GBE0 MDI1+				
A6	GBE0 MDI2-				
A7	GBE0 MDI2+				
A2	GBE0 MDI3-				
A3	GBE0 MDI3+				
A8	GBE0_LINK#	-	OD CMOS	Gigabit Ethernet Controller 0 link indicator, active low.	3.3V Suspend/ 3.3V
A4	GBE0_LINK100#	-	OD CMOS	Gigabit Ethernet Controller 0 100 Mbit / sec link indicator, active low.	3.3V Suspend/ 3.3V
A5	GBE0_LINK1000#	-	OD CMOS	Gigabit Ethernet Controller 0 1000 Mbit / sec link indicator, active low.	3.3V Suspend/ 3.3V
A14	GBE0_CTREF	-	REF	Reserved resistor NP (Reference voltage for Carrier Board Ethernet channel 0 magnetics center	GND min 3.3V max
B2	GBE0_ACT#	-	OD CMOS	I210 chip to Com Express Row connector.	3.3V Suspend/ 3.3V

Table 12 B65C LAN

3.3.1 PCB layout guideline - LAN

Parameter	Trace Routing
Differential Impedance	100 Ω +/-10%
Single-ended Impedance	50 Ω +/-10%
Trace width (W)	3.5 mil PCB stack-up dependent
Spacing between differential pairs (intra-pair) (S)	6.5 mil PCB stack-up dependent
Spacing between RX and TX pairs (inter-pair) (s)	Microstrip > 7H Stripline > 6H
Length matching between RX and TX pairs (inter-pair)	Max. 5mils
Spacing from edge of plane	Min. 10*W mils (W=trace width)

Table 13 LAN Layout information

3.3.2 Reference schematic - PCOM-C60B R1

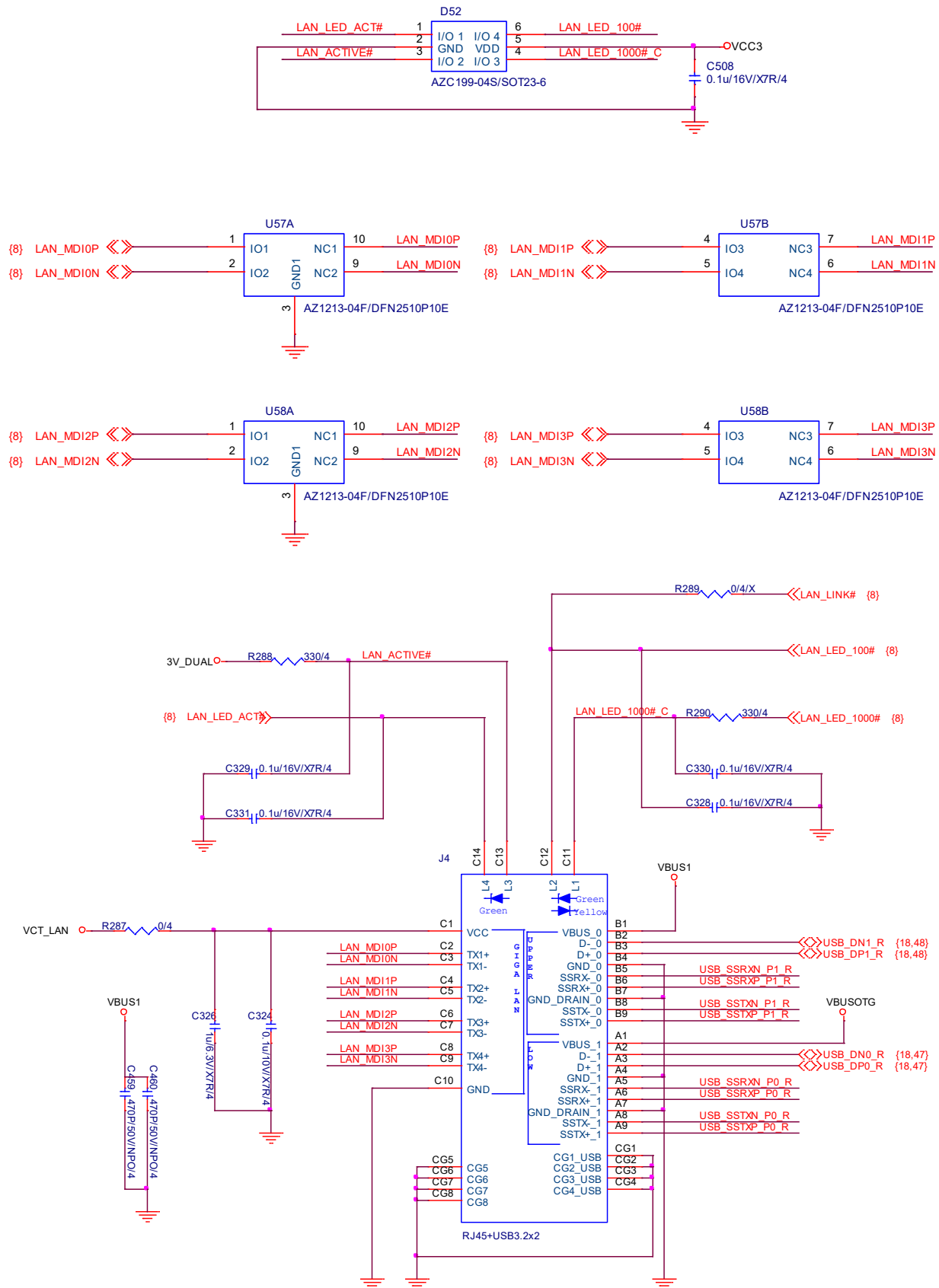


Figure 9 Reference schematic – LAN

3.3.3 Max trace length and available carrier trace length - LAN

PIN	Name	Module Length	Max Length	Available Carrier length
A13	GBE0_MDI0+	790	4000	3210
A12	GBE0_MDI0-	788.19	4000	3211.81
A10	GBE0_MDI1+	683.18	4000	3316.82
A9	GBE0_MDI1-	680.95	4000	3319.05
A7	GBE0_MDI2+	807.87	4000	3192.13
A6	GBE0_MDI2-	808.3	4000	3191.7
A3	GBE0_MDI3+	680.71	4000	3319.29
A2	GBE0_MDI3-	680.29	4000	3319.71

Table 14 Carrier available traces - LAN

3.4 SATA

PCOM-B65C SATA

Pin#	Pin Name	COM e 2.0/2.1 Specification (Signals Requiring Module Termination)	Pin Typ	Module	Pwr Rail /Tolerance(Volt)
A16	SATA0 TX+	AC coupled on the Module	O SATA	0.01uF AC coupled on the Module(Gen3).	AC coupled on Module
A17	SATA0 TX-		I SATA		
A19	SATA0 RX+		O SATA		
A20	SATA0 RX-		I SATA		
B16	SATA1 TX+		O SATA		
B17	SATA1 TX-		I SATA		
B19	SATA1 RX+		O SATA		
B20	SATA1 RX-		I SATA		
A28	(S)ATA_ACT#		O/D(I/O) CMOS	PU 10k ohm	3.3V / 3.3V
B18	SUS_STAT#	Indicates imminent suspend operation; used to notify LPC devices	O CMOS	-	3.3VSuspend/ 3.3V

Table 15 B65C SATA

3.4.1 PCB layout guideline -SATA

Parameter	Trace Routing
Transfer Rate	Up to 6.0 Gbit/s
Maximum signal line length (coupled traces)	5 inches
Differential Impedance	85 Ω +/-10%
Single-ended Impedance	50 Ω +/-10%
Trace width (W)	4.5 mil PCB stack-up dependent
Spacing between differential pairs (intra-pair) (S)	4.5mil PCB stack-up dependent
Spacing between RX and TX,pairs (inter-pair) (s)	Microstrip > 7H Stripline > 7H
Spacing between TX and TX pairs (inter-pair) (s)	Microstrip > 5H Stripline > 5H
Length matching between differential pairs (intra-pair)	Max. 5mils
Spacing from edge of plane	Min. 10*W mils (W=trace width)
Via Usage	A maximum of 1 vias is recommended.
AC Coupling capacitors	10nF

Table 16 SATA layout information

3.4.2 Reference schematic - PCOM-C60B R1

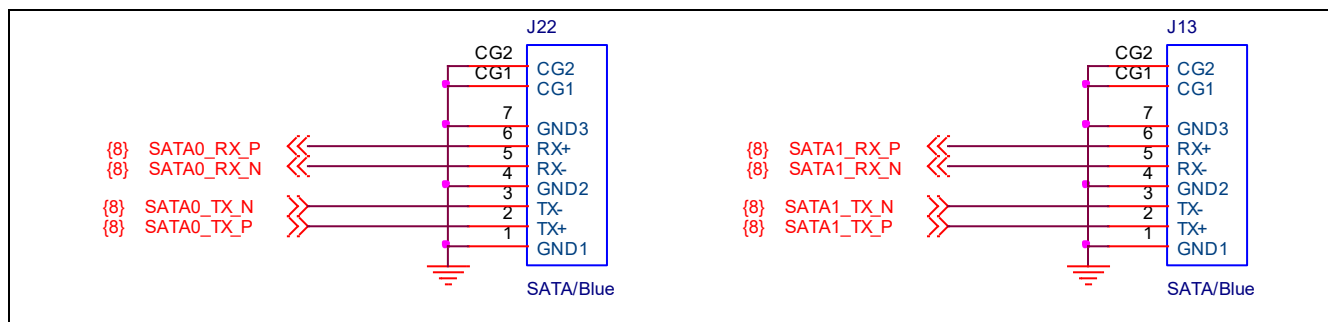


Figure 10 Reference schematic –SATA

3.4.3 Max trace length and available carrier trace length - SATA

PIN	Name	Module Length	Max Length	Available Carrier length
A16	SATA0_TX+	875.01	5000	4124.99
A17	SATA0_TX-	877.05	5000	4122.95
A19	SATA0_RX+	854.78	5000	4145.22
A20	SATA0_RX-	850.94	5000	4149.06
B16	SATA1_TX+	836.90	5000	4163.1
B17	SATA1_TX-	836.42	5000	4163.58
B19	SATA1_RX+	796.17	5000	4203.83
B20	SATA1_RX-	795.18	5000	4204.82

Table 17 Carrier available traces - SATA

3.5 DDI

PCOM-B65C DDI

Pin#	Pin Name	COM e 3.0/3.1 Specification (Signals Requiring Module Termination)	Pin Type	B65C Module
D26	DDI1 PAIR0+	AC coupled off Module.	O PCIE	AC coupled off Module.
D27	DDI1 PAIR0-			
D29	DDI1 PAIR1+			
D30	DDI1 PAIR1-			
D32	DDI1 PAIR2+			
D33	DDI1 PAIR2-			
D36	DDI1 PAIR3+			
D37	DDI1 PAIR3-			
D15	DDI1_CTRLCLK_AUX+		I/O PCIE	1.Module flow COM Express Spec Figure 4- 1: Dual-Mode COM Express Module Implementation
			I/O OD CMOS	
D16	DDI1_CTRLDATA_AUX-		I/O(I/O) PCIE	
			I/O OD CMOS	
D34	DDI1_DDC_AUX_SEL	1M pull-down to logic ground on the Module	I CMOS	1M pull-down to GND on the Module
C24	DDI1_HPD		I CMOS	Follow INTEL SKL PDG : PD 100k ohm to GND
D39	DDI2 PAIR0+	AC coupled off Module.	O PCIE	AC coupled off Module.
D40	DDI2 PAIR0-			
D42	DDI2 PAIR1+			
D43	DDI2 PAIR1-			
D46	DDI2 PAIR2+			
D47	DDI2 PAIR2-			
D49	DDI2 PAIR3+			
D50	DDI2 PAIR3-			
C32	DDI2_CTRLCLK_AUX+		I/O PCIE	1.Module flow COM Express Spec Figure 4- 1: Dual-Mode COM Express Module Implementation
			I/O OD CMOS	
C33	DDI2_CTRLDATA_AUX-		I/O PCIE	
			I/O OD CMOS	
C34	DDI2_DDC_AUX_SEL	1M pull-down to logic ground on the Module	I CMOS	1M pull-down to GND on the Module.
D44	DDI2_HPD		I CMOS	Follow INTEL SKL PDG : PD 100k ohm to GND
C39	DDI3 PAIR0+	AC coupled off Module.	O PCIE	DP/DP to VGA co-lay DDI signal. 1.DP AC coupled off Module. 2.DP to VGA on board AC coupled on Module.
C40	DDI3 PAIR0-			
C42	DDI3 PAIR1+			AC coupled off Module.
C43	DDI3 PAIR1-			
C46	DDI3 PAIR2+			
C47	DDI3 PAIR2-			
C49	DDI3 PAIR3+			
C50	DDI3 PAIR3-			
C36	DDI3_CTRLCLK_AUX+		I/O PCIE	1.Module flow COM Express Spec Figure 4- 1: Dual-Mode COM Express Module Implementation
			I/O OD CMOS	
C37	DDI3_CTRLDATA_AUX-		I/O PCIE	
			I/O OD CMOS	
C38	DDI3_DDC_AUX_SEL	1M pull-down to logic ground on the Module	I CMOS	1M pull-down to GND on the Module.
C44	DDI3_HPD			Follow INTEL SKL PDG : PD 100k ohm to GND

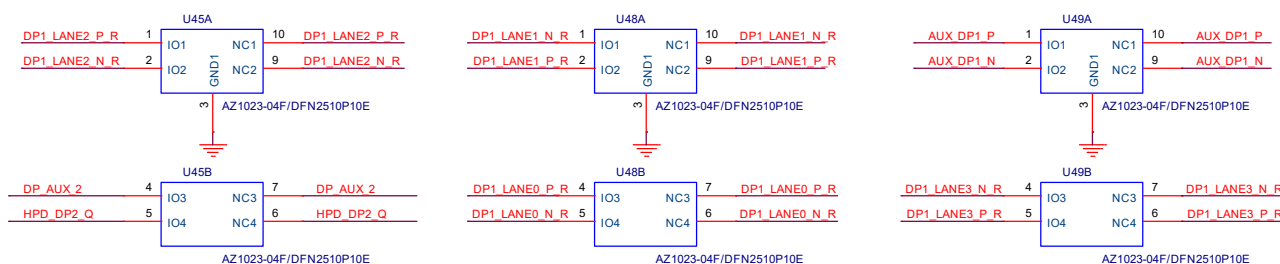
Table 18 B65C DDI (DP)

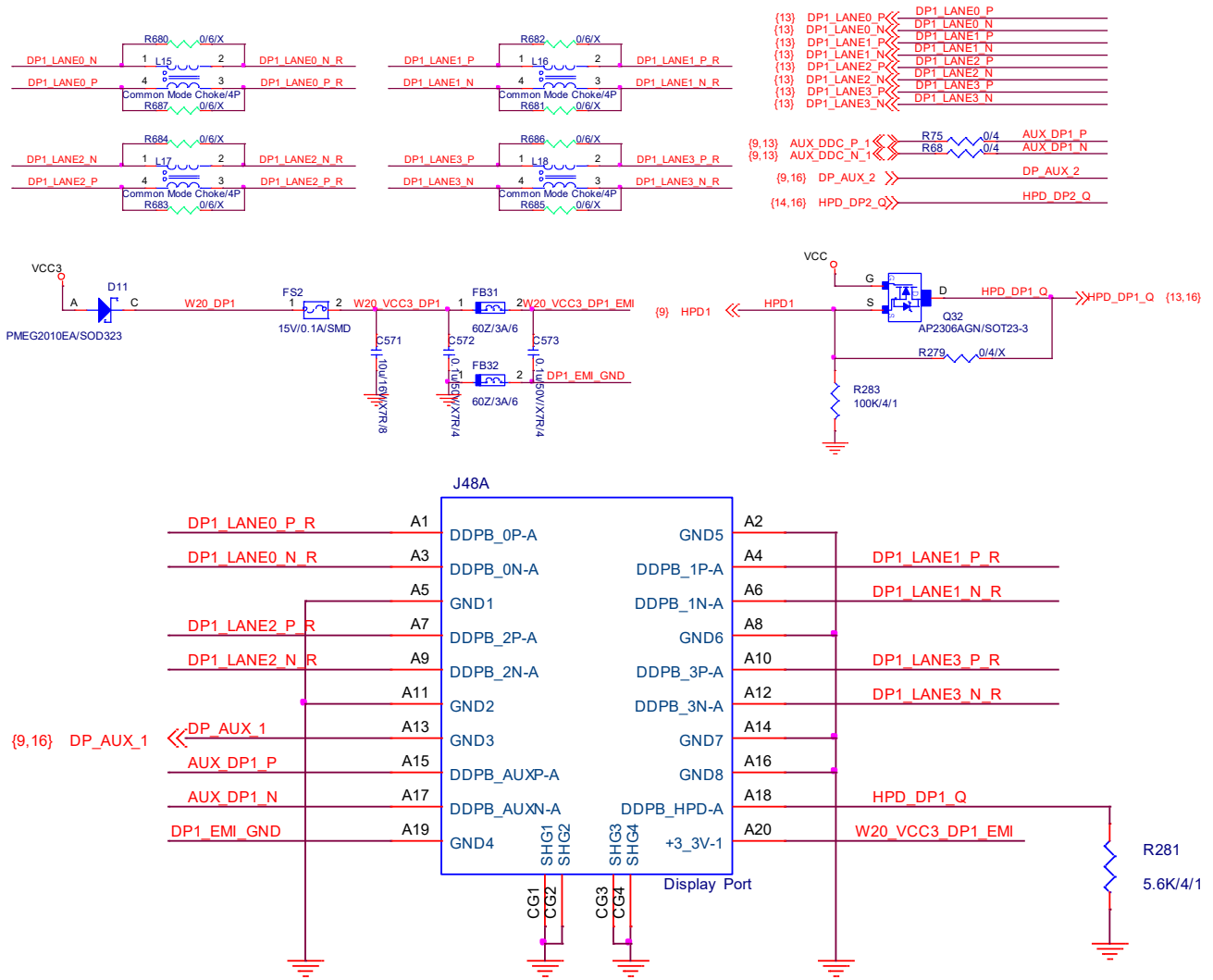
3.5.1 PCB layout guideline –DDI (DP)

Parameter	Trace Routing
Transfer Rate	Max. 5.4 Gbit/s
Maximum signal line length (coupled traces)	6 inches
Differential Impedance	85 Ω +/-10%
Single-ended Impedance	50 Ω +/-10%
Trace width (W)	4.5 mil PCB stack-up dependent
Spacing between differential pairs (intra-pair) (S)	4.5 mil PCB stack-up dependent
Spacing to other signals (Tx to Rx)	Microstrip > 9H Stripline > 5H PCB stack-up dependent
Length matching between differential pairs (intra-pair)	Max. 5mils
Spacing from edge of plane	Min. 10*W mils (W=trace width)
Via Usage	Max. 1
AC coupling capacitors	100nF

Table 19 DDI layout information

3.5.2 Reference schematic – PCOM-C60B R1





3.5.3 Max trace length and available carrier trace length – DDI (DP)

PIN	Name	Module Length	Max Length	Available Carrier length
D26	DDI1_PAIR0+	1443.75	6000	4556.25
D27	DDI1_PAIR0-	1444.38	6000	4555.62
D29	DDI1_PAIR1+	1410.4	6000	4589.6
D30	DDI1_PAIR1-	1407.46	6000	4592.54
D32	DDI1_PAIR2+	1356.9	6000	4643.1
D33	DDI1_PAIR2-	1358.8	6000	4641.2
D36	DDI1_PAIR3+	1408.05	6000	4591.95
D37	DDI1_PAIR3-	1409.45	6000	4590.55
D39	DDI2_PAIR0+	1402.34	6000	4597.66
D40	DDI2_PAIR0-	1400.08	6000	4599.92
D42	DDI2_PAIR1+	1253.81	6000	4746.19
D43	DDI2_PAIR1-	1257.13	6000	4742.87
D46	DDI2_PAIR2+	1319.34	6000	4680.66
D47	DDI2_PAIR2-	1319.93	6000	4680.07
D49	DDI2_PAIR3+	1631	6000	4369
D50	DDI2_PAIR3-	1632.05	6000	4367.95
C39	DDI3_PAIR0+	1991.9	6000	4008.1
C40	DDI3_PAIR0-	1988.33	6000	4011.67
C42	DDI3_PAIR1+	1429.17	6000	4570.83
C43	DDI3_PAIR1-	1430.24	6000	4569.76
C46	DDI3_PAIR2+	1805.97	6000	4194.03
C47	DDI3_PAIR2-	1807.36	6000	4192.64
C49	DDI3_PAIR3+	1991.82	6000	4008.18
C50	DDI3_PAIR3-	1988.92	6000	4011.08

Table 20 Carrier available traces – DDI (DP)

3.6 LVDS

PCOM-B65C DDI (DP)

Pin#	Pin Name	COM e 3.0/3.1 Specification (Signals Requiring Module Termination)	Pin Typ	B65C Module	Power Rail /Tolerance(Volt)
A71	LVDS A0+		O LVDS	According to COM Express Spec 2.1 Table 4.37 LVDS/eDP Pin Assignment definition Co-layer,default module PTN3460 to LVDS Com Express Row connector.	LVDS
A72	LVDS A0-				
A73	LVDS A1+				
A74	LVDS A1-				
A75	LVDS A2+				
A76	LVDS A2-				
A78	LVDS A3+				
A79	LVDS A3-				
A81	LVDS A CK+				
A82	LVDS A CK-				
B71	LVDS B0+				
B72	LVDS B0-				
B73	LVDS B1+				
B74	LVDS B1-				
B75	LVDS B2+				
B76	LVDS B2-				
B77	LVDS B3+				
B78	LVDS B3-				
B81	LVDS B CK+				
B82	LVDS B CK-				
B83	LVDS_BKLT_CTRL		O CMOS	LVDS_BKLT_CTRL	3.3V/ 3.3V
A77	LVDS VDD EN			LVDS panel power enable	
B79	LVDS BKLT EN			According to COM Express Spec 2.1 Table 4.37 LVDS/eDP Pin Assignment definition Co-layer,default module PTN3460 to LVDS DDC signal to Com Express Row connector.	
A83	LVDS_I2C_CK				
A84	LVDS_I2C_DAT		I/O OD CMOS		

Table 21 B65C LVDS

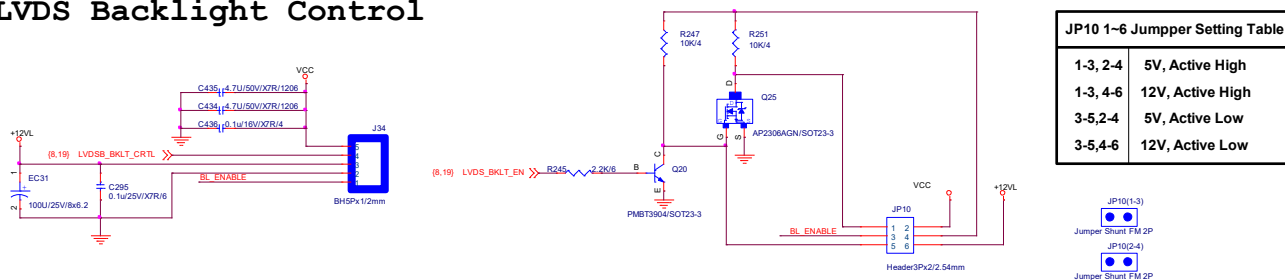
3.6.1 PCB layout guideline – LVDS

Parameter	Trace Routing
Maximum signal line length to the LVDS connector (coupled traces)	10 inches
Differential Impedance	85 Ω +/-15%
Single-ended Impedance	50 Ω +/-15%
Trace width (W)	PCB stack-up dependent
Spacing between differential pairs (intra-pair) (S)	30 mil PCB stack-up dependent

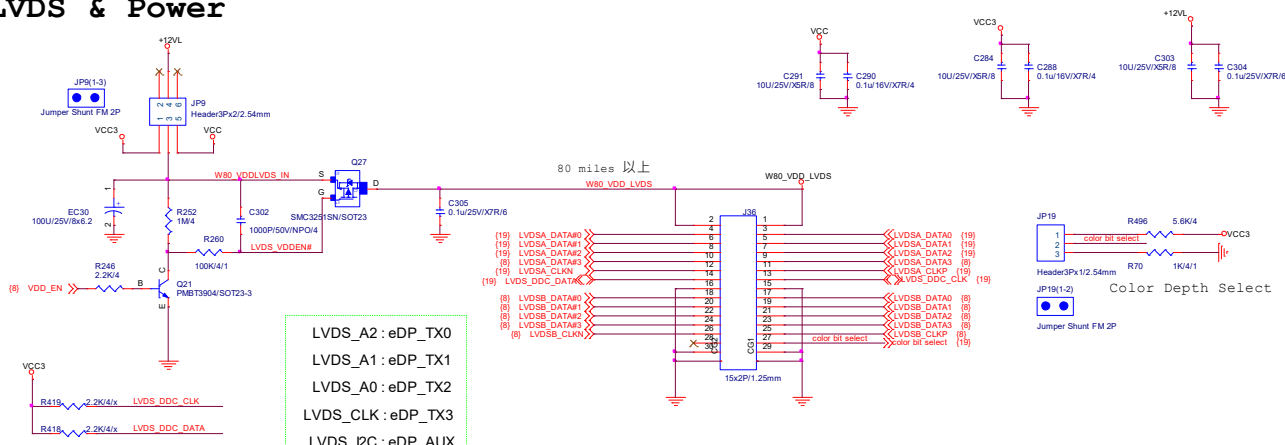
Table 22 LVDS Layout information

3.6.2 Reference schematic – PCOM-C60B R1

LVDS Backlight Control



LVDS & Power



3.6.3 Max trace length and available carrier trace length - LVDS

PIN	Name	Module Length	Max Length	Available Carrier length
A71	LVDS_A0+	999.32	10000	9000.68
A72	LVDS_A0-	1000.97	10000	8999.03
A73	LVDS_A1+	810.56	10000	9189.44
A74	LVDS_A1-	815.26	10000	9184.74
A75	LVDS_A2+	768.62	10000	9231.38
A76	LVDS_A2-	764.03	10000	9235.97
A78	LVDS_A3+	785.71	10000	9214.29
A79	LVDS_A3-	784.88	10000	9215.12
A81	VDS_A_CK+	780.05	10000	9219.95
A82	VDS_A_CK-	782.38	10000	9217.62
A83	LVDS_I2CCLK	1539.65	10000	8460.35
A84	LVDS_I2CDAT	1637.38	10000	8362.62

Table 23 Carrier available traces – LVDS Channel A

PIN	Name	Module Length	Max Length	Available Carrier length
B71	LVDS_B0+	815.56	10000	9184.44
B72	LVDS_B0-	816.04	10000	9183.96
B73	LVDS_B1+	728.69	10000	9271.31
B74	LVDS_B1-	726.34	10000	9273.66
B75	LVDS_B2+	713.3	10000	9286.7
B76	LVDS_B2-	710.49	10000	9289.51
B77	LVDS_B3+	770.16	10000	9229.84
B78	LVDS_B3-	768.64	10000	9231.36
B81	LVDS_B_CK+	611.04	10000	9388.96
B82	LVDS_B_CK-	607.96	10000	9392.04

Table 24 Carrier available traces – LVDS Channel B

Table 4.39: LVDS / eDP Pin Assignment

Pin Name	Type 6/10 Pin Number	eDP
LVDS_A0+	A71	eDP_TX2+
LVDS_A0-	A72	eDP_TX2-
LVDS_A1+	A73	eDP_TX1+
LVDS_A1-	A74	eDP_TX1-
LVDS_A2+	A75	eDP_TX0+
LVDS_A2-	A76	eDP_TX0-
LVDS_A_CK+	A81	eDP_TX3+
LVDS_A_CK-	A82	eDP_TX3-
LVDS_VDD_EN	A77	eDP_VDD_EN
LVDS_BKLT_EN	B79	eDP_BKLT_EN
LVDS_I2C_CK	A83	eDP_AUX+
LVDS_I2C_DAT	A84	eDP_AUX-
LVDS_BKLT_CTRL	B83	eDP_BKLT_CTRL
RSVD	A87	eDP_HPD

3.7 UART

PCOM- B65C UART

Pin#	Pin Name	Description	Pin Typ	B65C Module	Pwr Rail /Tolerance(Volt)
A98	SER0_TX	General purpose serial port transmitter	O CMOS	Series connection Schottky diode	3.3V / 12V
A99	SER0_RX	General purpose serial port receiver	I CMOS		
A101	SER1_TX	General purpose serial port transmitter / CAN_TX	O CMOS		
A102	SER1_RX	General purpose serial port receiver / CAN_RX	I CMOS		

Table 25 B65C UART

3.7.1 Reference schematic - PCOM-C60B R1

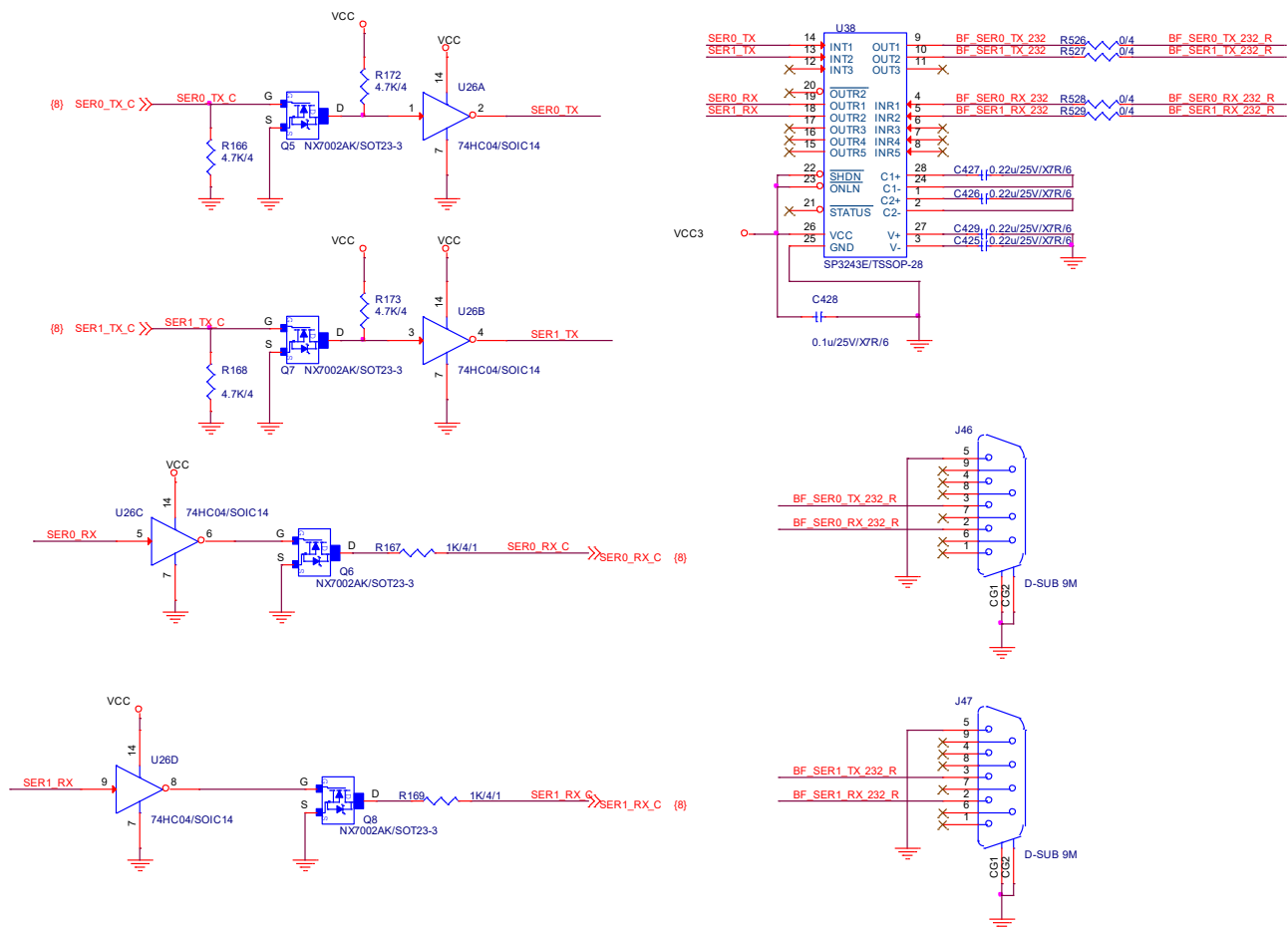


Figure 12 Reference schematic –UART

3.8 I2C

PCOM-B65C I2C

Pin#	Pin Name	Description	Pin Typ	B65C Module	Pwr Rail /Tolerance(Volt)
B33	I2C_CLK	General purpose I2C port clock output	I/O OD CMOS	PU 2.2k ohm to +3V_Dual.	3.3V Suspend/ 3.3V
B34	I2C_DAT	General purpose I2C port data I/O line			

Table 26 B65C I2C

3.9 SMBus

PCOM- B65C SMBus

Pin#	Pin Name	Description	Pin Typ	B65C Module	Pwr Rail /Tolerance(Volt)
B13	SMB_CK	System Management Bus bidirectional clock line	I/O OD CMOS	PU 2.2K ohm to +3V_Dual.	3.3V Suspend/ 3.3V
B14	SMB_DAT	System Management Bus bidirectional data line			
B15	SMB_ALERT#	System Management Bus Alert – active low input can be used to generate an SMI# (System Management Interrupt) or to wake the system	I CMOS	PU 10K ohm to +3V_Dual	

Table 27 B65C SMBus

3.10 GPIO

PCOM- B65C GPIO

Pin#	Pin Name	Description	Pin Typ	B65C Module	Pwr Rail /Tolerance(Volt)
A54	GPIO	General purpose input pins. Pulled high internally on the Module.	I CMOS	PU 5.6k ohm to +3.3V.	3.3V/ 3.3V
A63	GPI1				
A67	GPI2				
A85	GPI3				
A93	GPO0	-	O CMOS	EC to Com Express Row connector.	3.3V/ 3.3V
B54	GPO1				
B57	GPO2				
B63	GPO3				

Table 28 B65C GPIO

3.11 LPC

Parameter	Trace Routing
Maximum signal line length	10 inches
Single-ended Impedance	50 Ω +/-10%
Trace width (W)	PCB stack-up dependent
Trace-to-trace space	PCB stack-up dependent 3h

Pin#	Pin Name	Description	Pin Typ	B65C Module	Pwr Rail /Tolerance(Volt)
A50	LPC_SERIRQ	LPC Mode: LPC serial interrupt	I/O CMOS	PU 4.7k ohm to +3.3V	3.3V/ 3.3V
B3	LPC_FRAME#	LPC frame indicates the start of an LPC cycle	O CMOS	Bridge to Com Express Row connector	
B4	LPC AD0	LPC Mode: LPC multiplexed address, command and data bus	I/O CMOS		
B5	LPC AD1				
B6	LPC AD2				
B7	LPC AD3				
B8	LPC DRO0#	LPC Mode: LPC serial DMA request	I CMOS	NC	
B9	LPC DRO1#				
B10	LPC_CLK	LPC clock output	O CMOS	Bridge to Com Express Row connector	

Table 29 B65C LPC

PIN	Name	Module Length	Max Length	Available Carrier length
A50	LPC_SERIRQ	4134.00	10000	5866
B3	LPC_FRAME#	4298.58	10000	5701.42
B4	LPC_AD0	4093.20	10000	5906.8
B5	LPC_AD1	4100.18	10000	5899.82
B6	LPC_AD2	4097.40	10000	5902.6
B7	LPC_AD3	4110.37	10000	5889.63
B10	LPC_CLK	4213.87	10000	5786.13

3.11.1 Reference schematic - PCOM-C60B R1

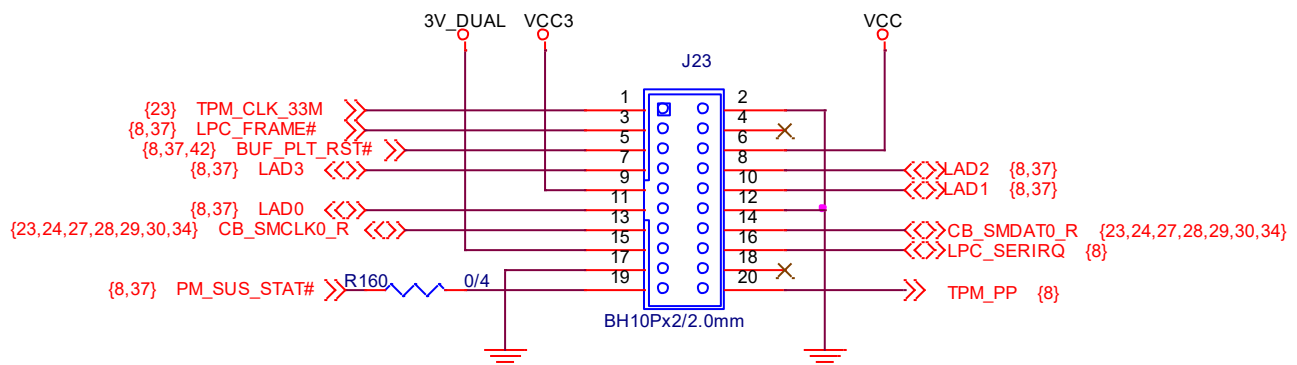


Figure 13 Reference schematic –LPC

3.12 SPI

An external SPI BIOS is designed on the Carrier board, which allows the Module boot from the Carrier SPI BIOS. To achieve this function, the BIOS_DIS0# and BIOS_DIS1# must be designed as a selectable method on the Carrier.

PCOM-B65C SPI

Pin#	Pin Name	Description	Pin Typ	B65C Module	Pwr Rail /Tolerance(Volt)
A34	BIOS_DIS0#	Selection strap to determine the BIOS boot device. The Carrier should only float these or pull them low	I CMOS	PU 10k ohm to +3V_Dual	NA
B88	BIOS_DIS1#				
A91	SPI_POWER	Power supply for Carrier Board SPI – sourced from Module – nominally 3.3V. The Module shall provide a minimum of 100mA on SPI_POWER	O	+3V_Dual	3.3V Suspend/ 3.3V
A92	SPI_MISO	Data in to Module from Carrier SPI	I CMOS	Level Translator to Com Express Row connector	
A95	SPI_MOSI	Data out from Module to Carrier SPI	O CMOS		
A94	SPI_CLK	Clock from Module to Carrier SPI			
B97	SPI_CS#	-	O CMOS		

Table 30 PCOM-B65C SPI

3.12.1 Reference schematic - PCOM-C60B R1

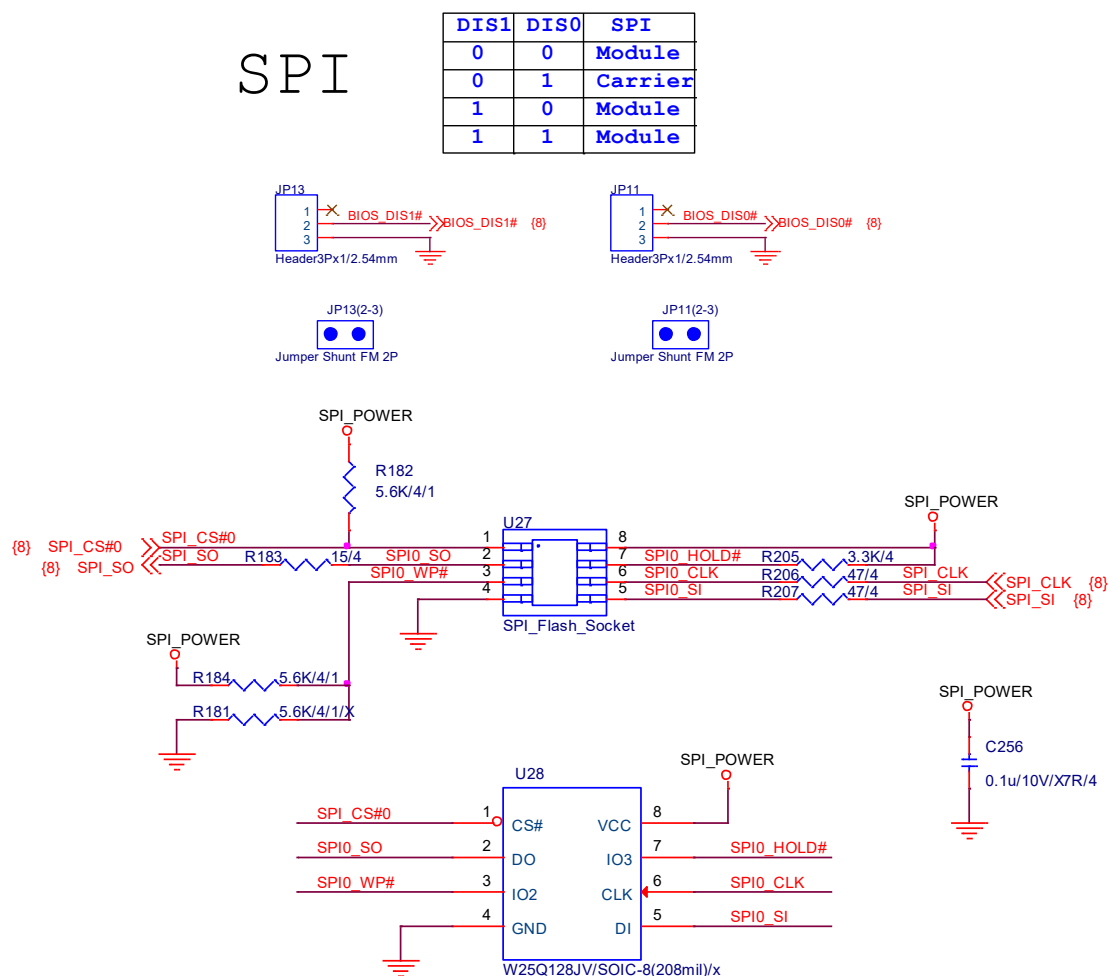


Figure 14 Reference schematic –SPI

4 Power

PCOM-B65C is designed for both AT and ATX power mode, which depends on the power mode design on carrier board. The following ATX and AT mode power sequences are provided for the carrier design guideline.

4.1 Power sequence

The AT power sequence is based on PCOM-B65C with evaluation carrier PCOM-C60B R1

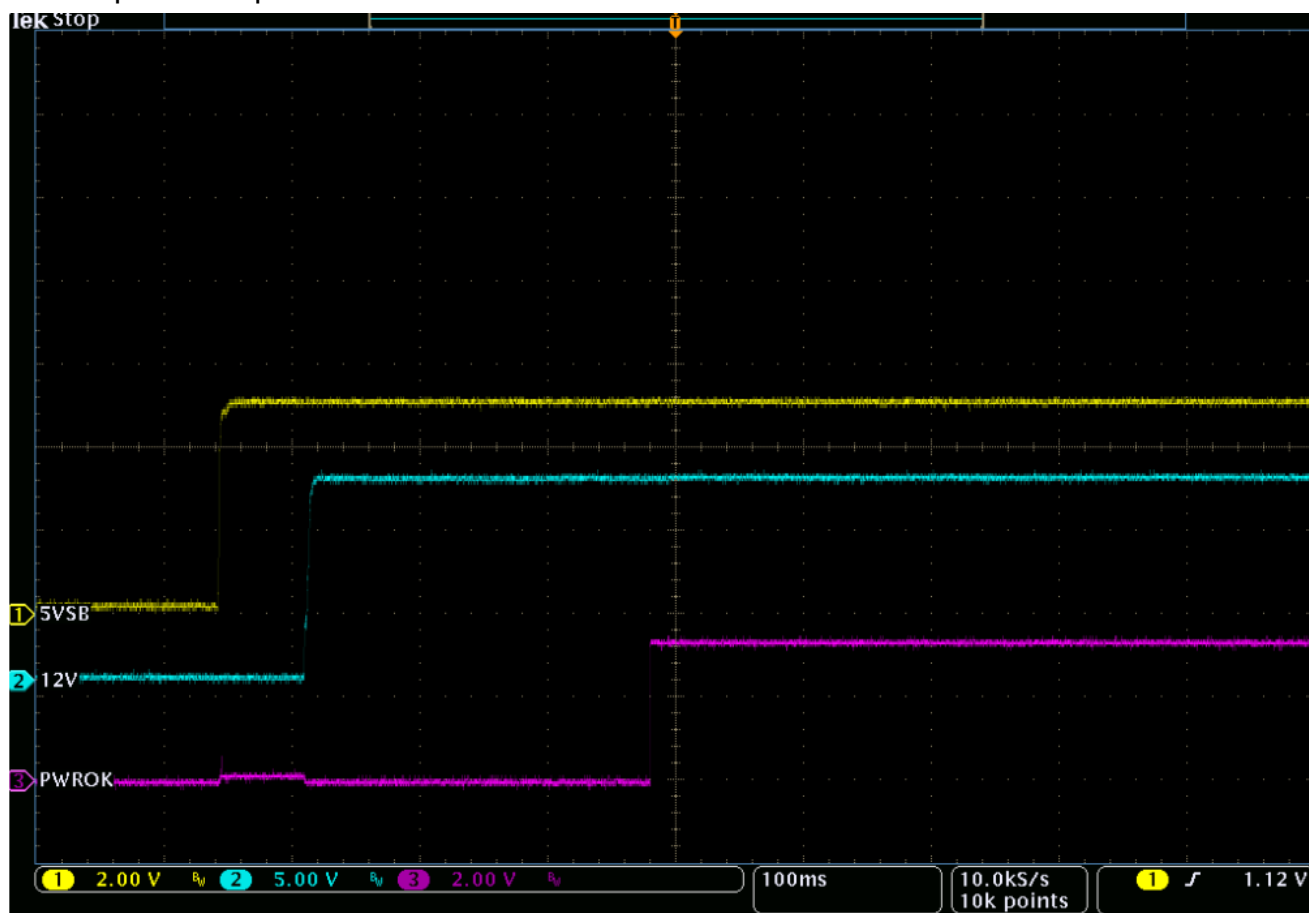


Figure 15 Power Sequence under AT Mode

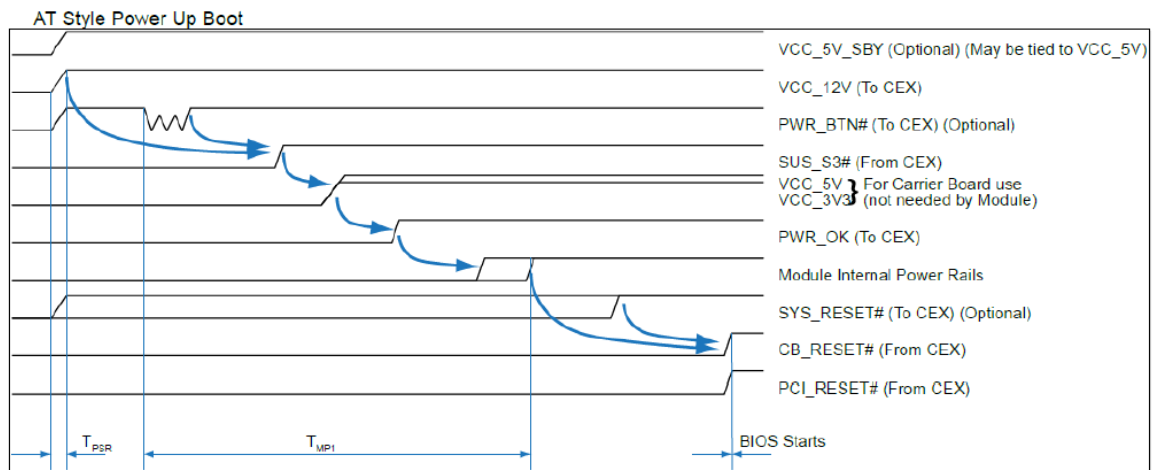


Figure 16 Carrier Power Sequence under AT Mode

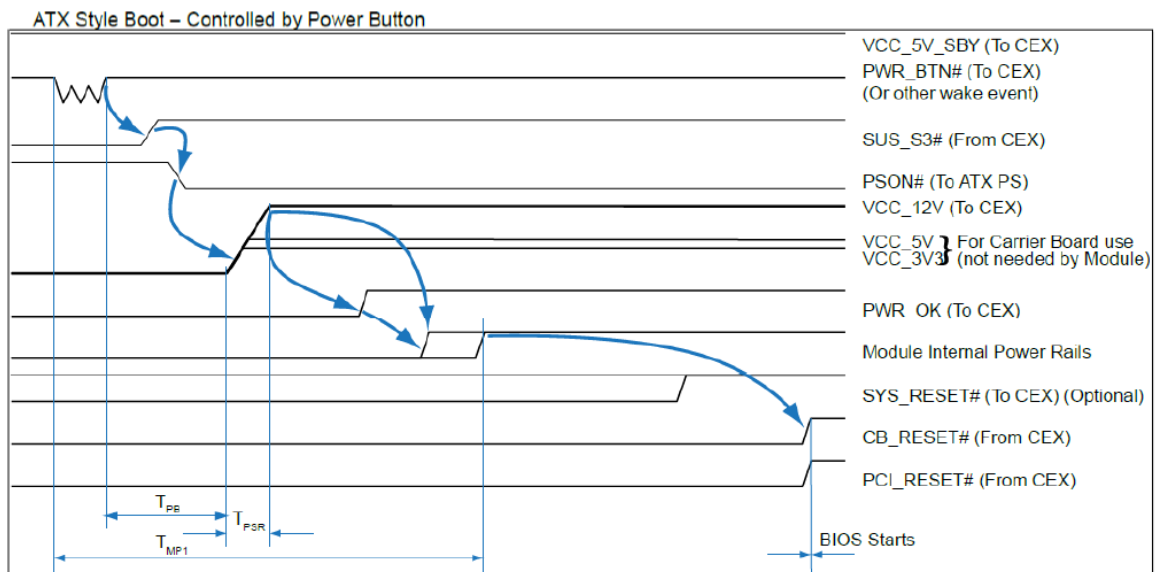
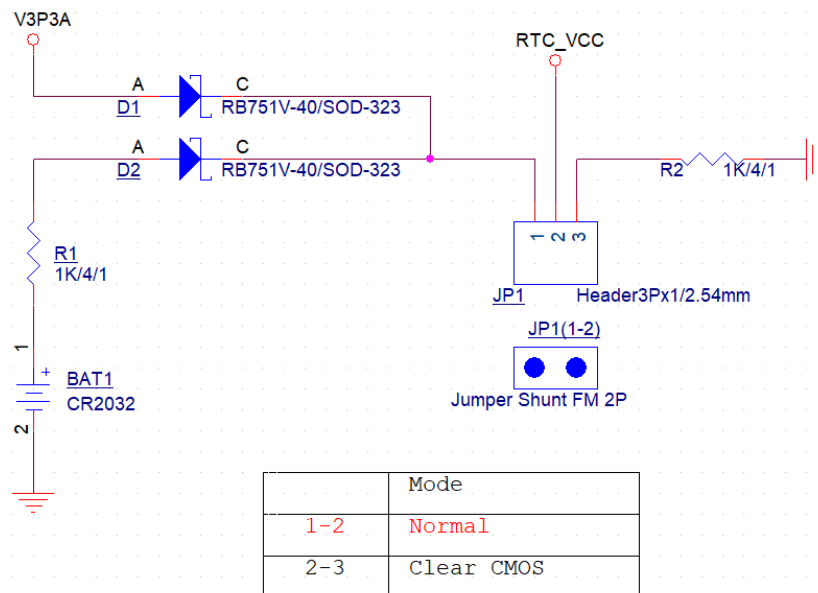


Figure 17 Carrier Power Sequence under ATX Mode

4.2 RTC_VCC

To implement the RTC Battery according to the Underwriters Laboratories IncR (UL) guidelines, battery cells must be protected against a reverse current going to the cell. This can be done by either a series low-leakage diode and/or a series resistor. Revision 1.0 of this specification did not specify the location of this diode and the location was vendor implementation specific. For revision 2.0 Carrier Boards, a protection diode or a series resistor shall be placed on the Carrier Board. For backwards compatibility, a revision 2.0 Module may also implement the protection diode.

Note: If a Schottky diode is used, the leakage current must not exceed the UL requirement of the battery, especially at the temperature limits.



5 Mechanical

5.1 PCOM-B65C Dimension

PCOM-B65C top side view dimension

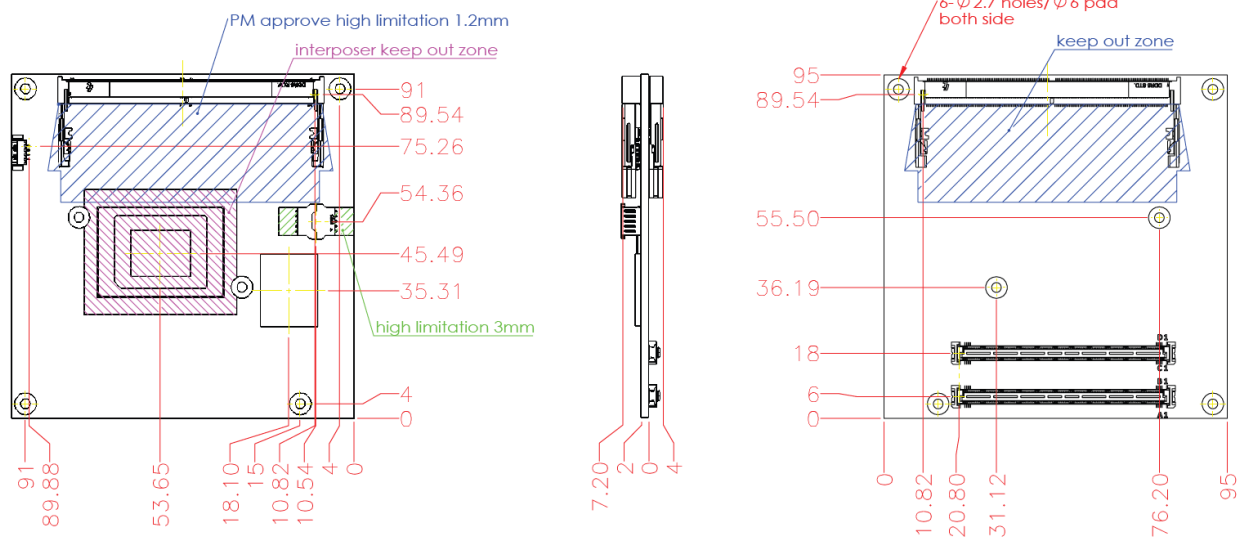


Figure 18 PCOM-B65C Dimension – TOP & Bottom

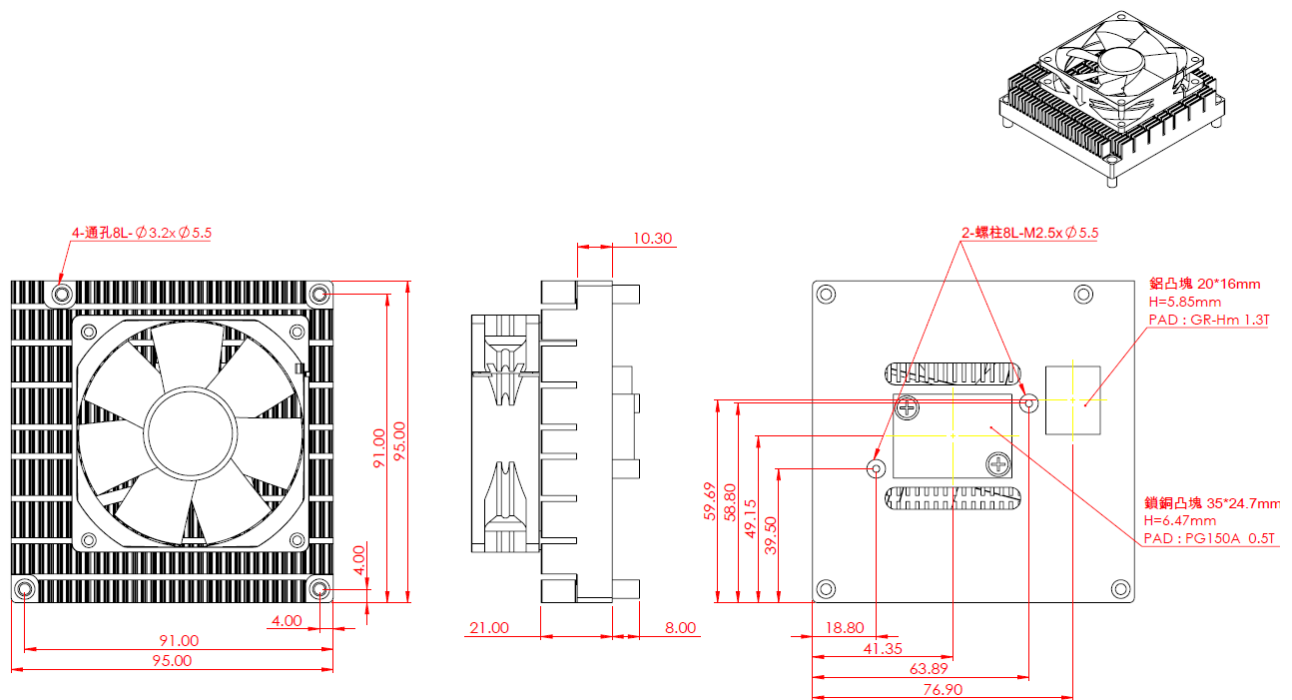


Figure 19 PCOM-B65C side view dimension, along with a heat sink / cooler.

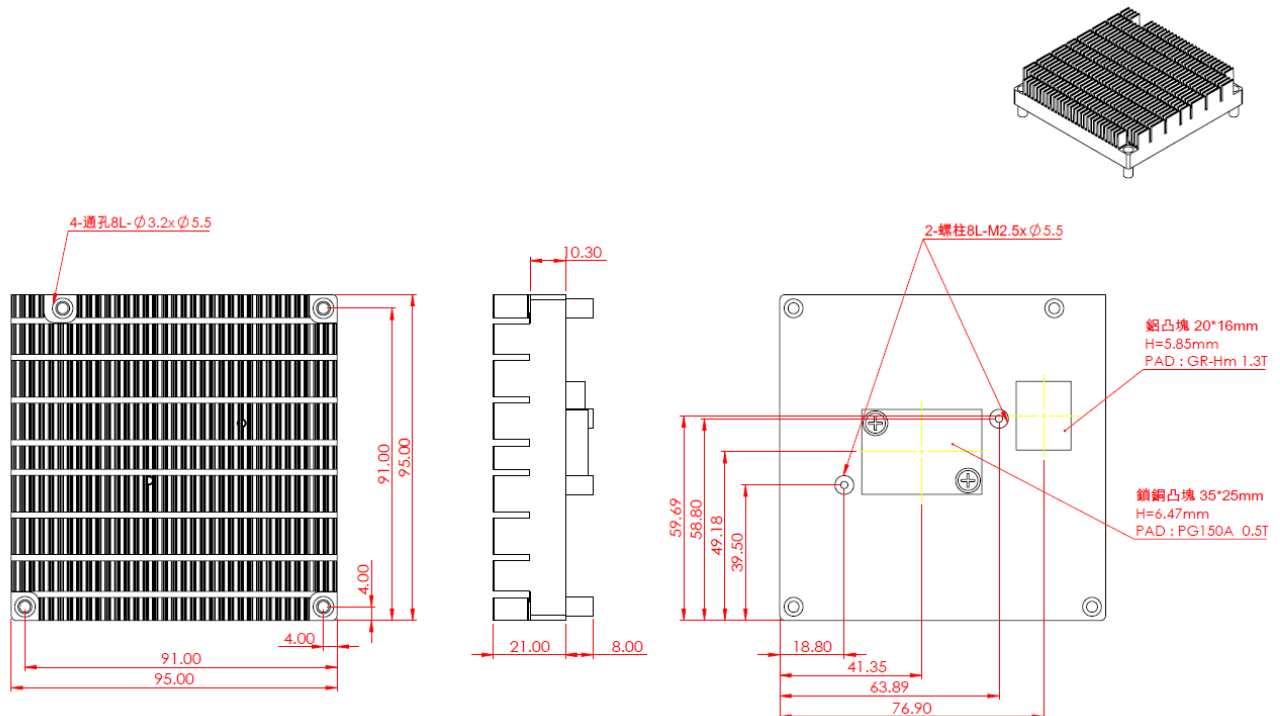


Figure 20 PCOM-B65C side view dimension, along with a heat sink.

6 COM Express Module and Carrier protection design

6.1 Module protection

PCOM-B65C Type 6, Schottky diode protection has been design on the COM Express module for Serial Port, FAN(PWMOUT & TACHIN), LID and SLEEP. Please refer to Fig.21 Module circuit protection schematic.

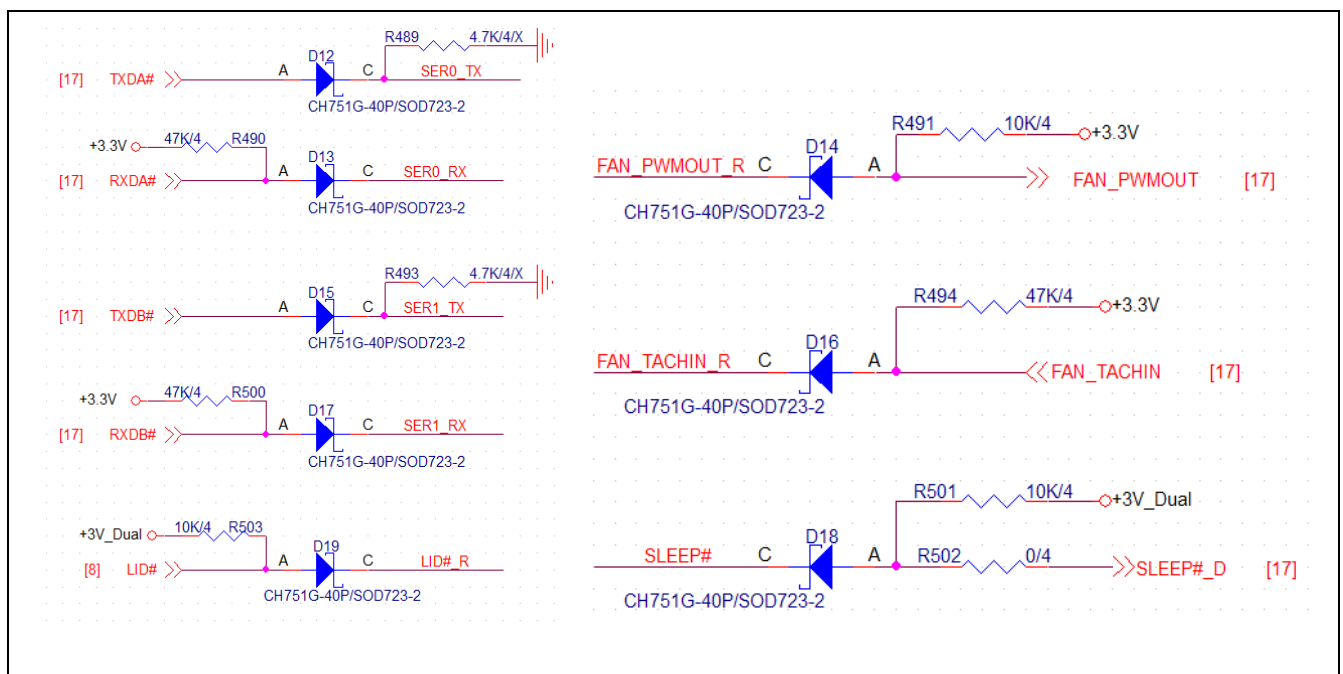


Figure 21 Circuit protection on Module

6.2 Carrier protection

Avoiding Carrier accidentally exposure to VCC_12V pool, a circuit protection design should be implemented on the Carrier, please refer to Fig.22 Carrier circuit protection schematic.

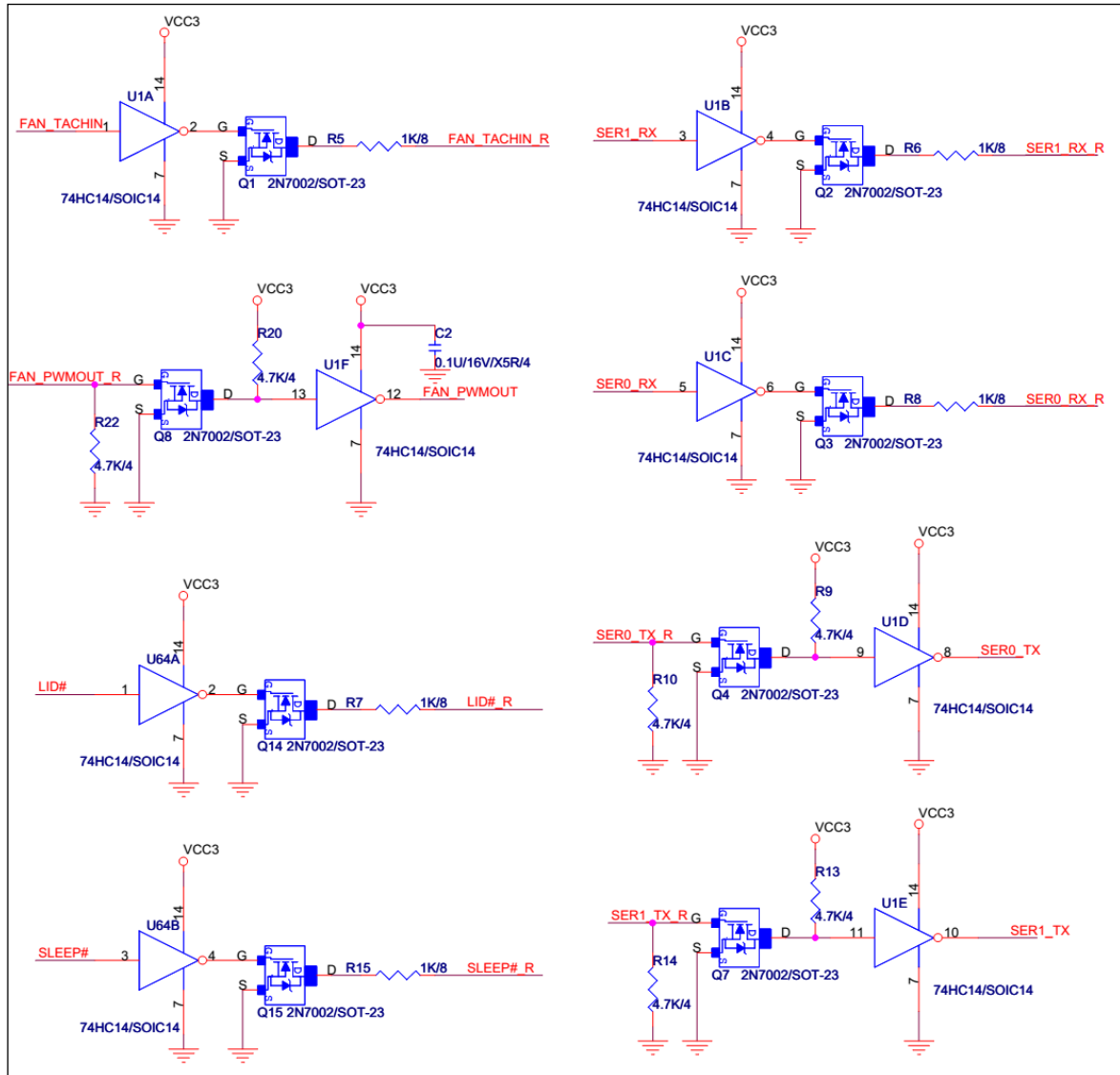


Figure 22 Circuit protection on Carrier

7 Industry Specifications

Low Pin Count Interface Specification, Revision 1.0 (LPC)

<http://www.intel.com/design/chipsets/industry/lpc.htm>

Universal Serial Bus (USB) Specification, Revision 2.0 <http://www.usb.org/home>

Serial ATA Specification, Revision 3.0 <http://www.serialata.org/>

PCI Express Base Specification, Revision 2.0 <https://www.pcisig.com/specifications>

PICMG® COM Express Module™ Base Specification <http://www.picmg.org/>

PICMG®COM Express Carrier Board Design Guide <http://www.picmg.org/>